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Power supplies

Page 3

USB 2.0 interface, LPC4370 USB, reset, crystal, jtag/swd

Page 4

Boot mode, LPC4370 IOs, external spi flash

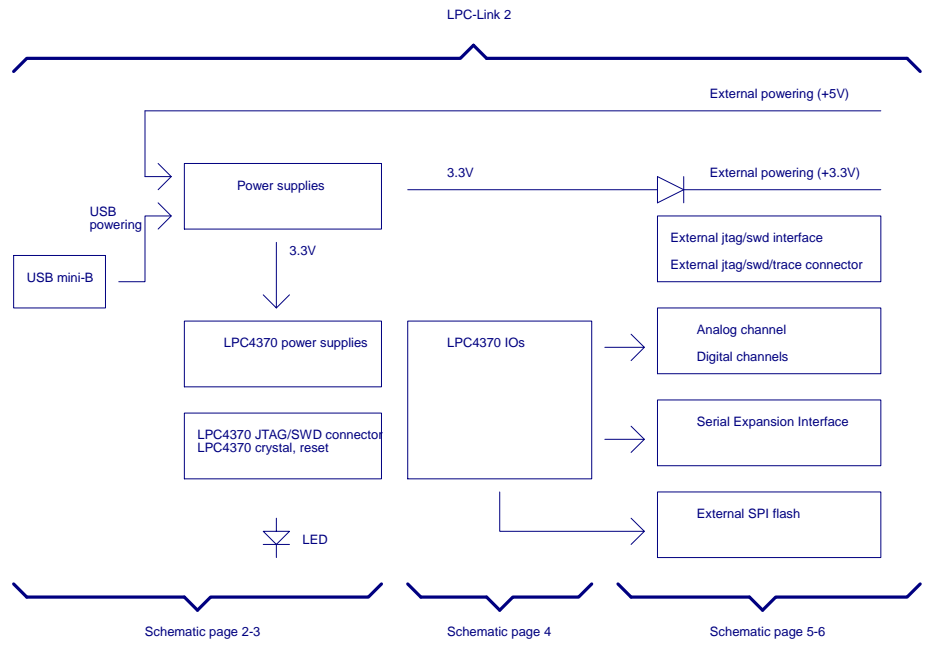
Page 5

External JTAG/Cortex debug interface

Page 6

Analog channel, digital channels, jtag/swd/trace interface

Design Overview



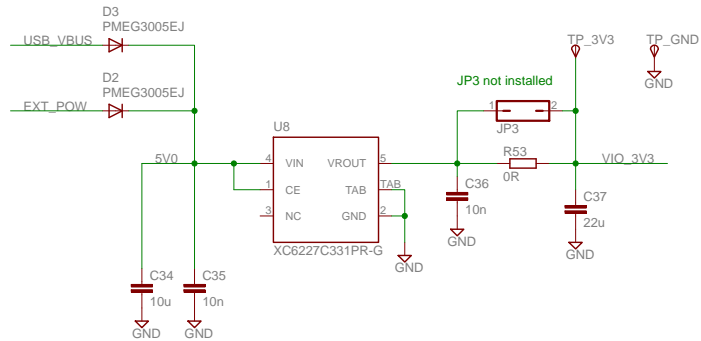
UL = UnLoaded = normally not mounted component.

Default jumper settings are indicated in the schematic. However, always check jumper positions on actual boards since there is no guarantee that all jumpers are in default place.

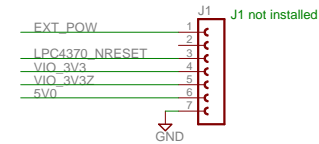
NXP Semiconductors

TITLE: LPC-Link2_v3_RevB	
Document Number:	REV:
Date: 4/27/2015 8:39:07 AM	Sheet: 1/6

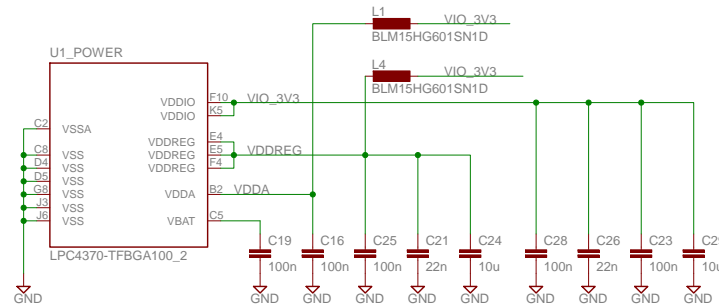
Power supply



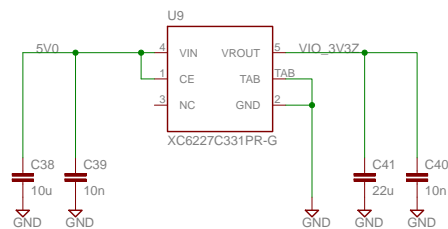
Power Supply Access connector



LPC4370 power supplies



Target Power supply

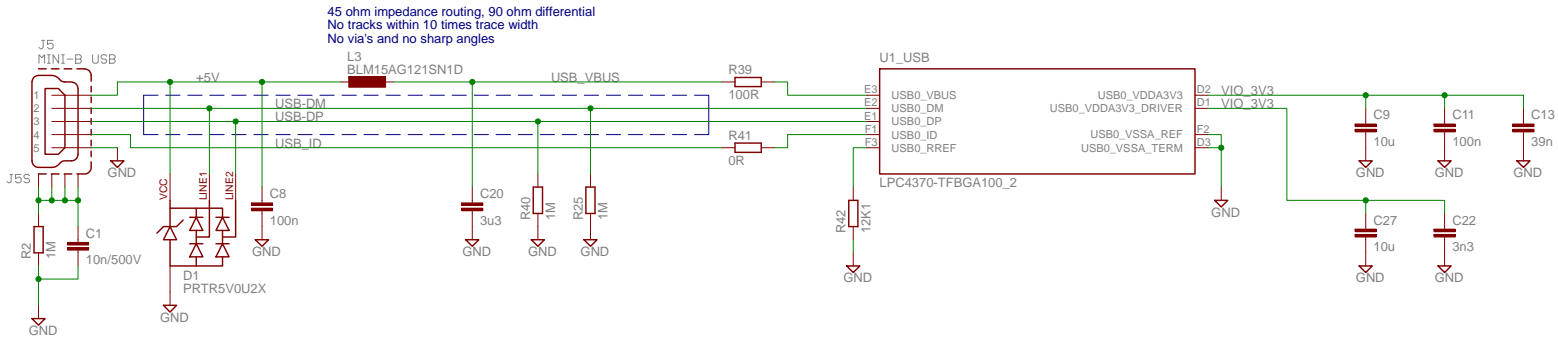


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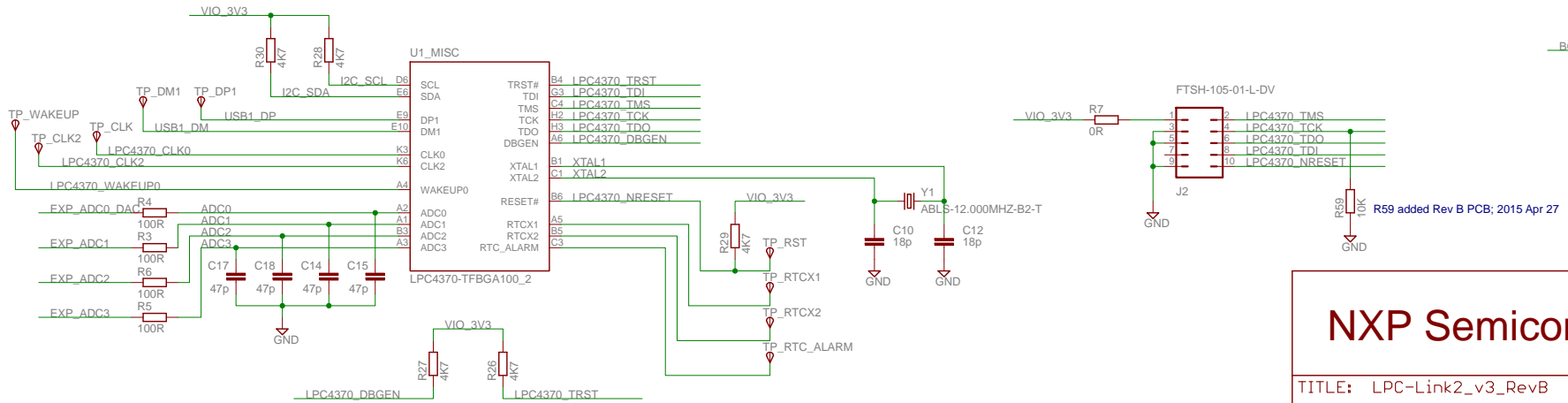
USB 2.0 OTG Interface

LPC4370 USB



LPC4370 reset, crystal, JTAG/SWD

LED



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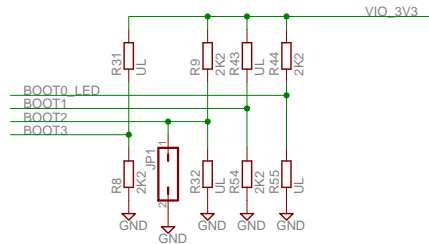
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REV:

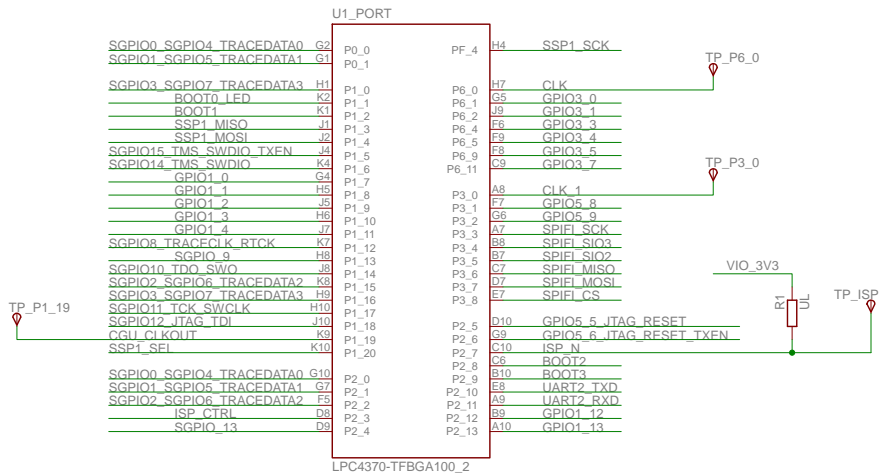
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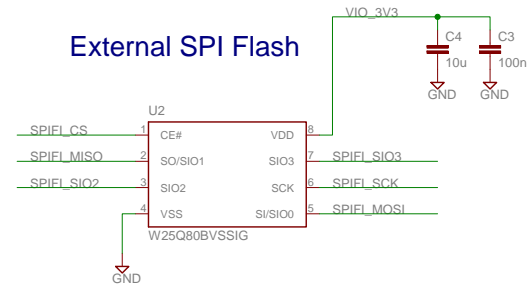
Boot mode - DFU USB0 (0b0101)
- SPIFI (0b0001)



LPC4370 IOs



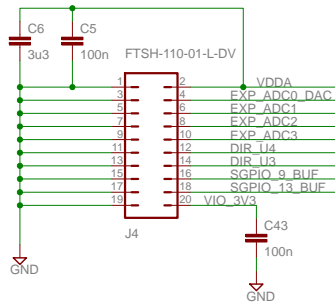
External SPI Flash



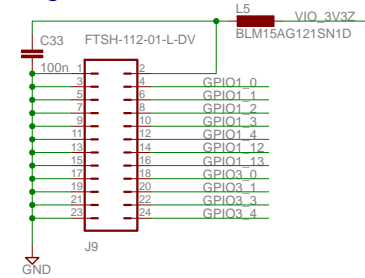
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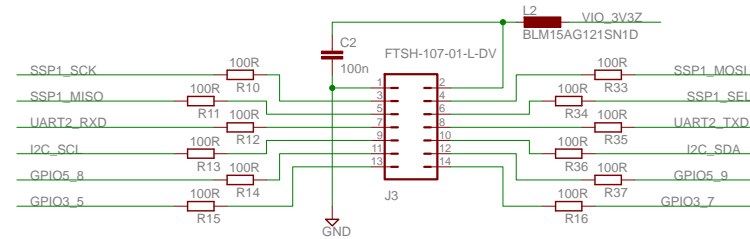
Analog + Digital channels



Digital channels



Serial Expansion Interface



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