+2.5V_LINK - Chng R19 to 4.12ohm; sht 3.
- Add hdr & shunt at JP3; sht 3.
- Add JS28, JS29, JS30; sht 2.

C30 27pF

A1 - Chng R19 to 4.12ohm; sht 3. 05/06/2015

B1

Fanout_TP

U12

12M

GND

12Kohms

12Kohms

12Kohms

C31 27pF

Power-On LED

Link +2.5V Power

Target +3.3V Power

Target +1.8V Power

+2.5V_LINK - Chng JS10 to R80 4.12ohm; sht 3.

- Add hdr & shunt at JP3; sht 3.

- Add JS28, JS29, JS30; sht 2.

- Add C66 - C72 decoupling, sht 1B

- Add JS10 to R80 4.12ohm; sht 3.

- Add hdr & shunt at JP3; sht 3.

- Add JS28, JS29, JS30; sht 2.

Buffer Pwr Select (JP2)
- On-board Target 1 - 2 (default)
- Off-board Target 2 - 3

Target SWD Debug

Target to debug location (JP1)
- On-board Target - open (default)
- Off-board Target - short
LPC5411x Current measurement

ADC111S021 12bit ADC

Vsense (1)  
JP3 open  
LPC5411x voltage 1-lsb  
Current 1-lsb  
maximum current  
ADC input  
1-lsb  
32uV  
3.88uA  
7.77uA  
16mA  
800uV

(1) Vsense voltage is between U16 RS+ to RS-. Total Rvsense = R19 + (JS10 || JP3).

JP3 Setting

<table>
<thead>
<tr>
<th>JP3 Setting</th>
<th>Total Rvsense (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V open</td>
<td>8.24</td>
</tr>
<tr>
<td>1.8V shunted</td>
<td>4.12</td>
</tr>
</tbody>
</table>

Target External Vin 5V

Open use P1_6 for FC7_SCK

USB_DP  
USB_DM  
+3.3V  
0.1uF  
C39  
GND

USB_DP  
USB_DM  
+3.3V  
0.1uF  
C39  
GND
The diagram illustrates the connectivity and components of a system based on the LPC5411x microcontroller. It includes various pins and connections for different functionalities:

- **VDD/LPC5411x**
- **GND**
- **+5V**
- **+3.3V**

### SPI / I2C Bridge Header

The SPI / I2C bridge header is Pmod compatible and features pins for configuration and communication. Note: 2.2k on BRIDGE_T_INTR-ISP1 (P0_4) is required for SPI / I2C boot over host interface.

### NXP A700x / A71x Secure MCU

- **Operating range:** 1.62 - 1.98V; 2.4 - 3.6V
- **I2C address:** 0b1001000 (JCOP default)

### UART to FTDI USB

- **TTL-232R-3V3 compatible**
- **SCI2C protocol**

### Other Notes:

- **2.2k on BRIDGE_T_INTR-ISP1 (P0_4) is required for SPI / I2C boot over host interface.**
- **Note:** 2.2k on BRIDGE_T_INTR-ISP1 (P0_4) is required for SPI / I2C boot over host interface.

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**Diagram Details:**

- **Connectors and Headers:**
- **Cables and Wires:**
- **Components:**
- **Notes and Specifications:**