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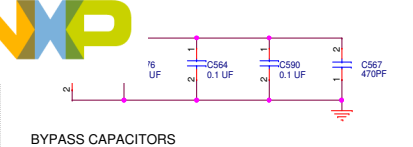
Revisions			
Rev	Description	Date	Approved
A	Released to FAB	04/09/07	DK
B	Pilot Release	08/13/07	DK
B1	- Fixed non RoHS comps - Detailed LCD rework - Detailed serial port rework	09/24/07	DK
B2	- Fixed CAN - Changed PWM1 signal - Input to Rev C layout	10/16/07	DK
C	Production Release	10/18/07	DK
C1	- Added diode protection in power supply - Replaced Logic PD with a 60 pin non shrouded header - Changed LCD_OFF signal on LPD con to P12C1 to match on board LCD - Changed ADC_REF 2 pin hdrs to a single 3 pin hdr	02/21/08	DK
C2	- Updated J4 Footprint	02/26/08	DK
D	Production Release	02/27/08	DK
D1	- Replaced obsolete 32KHz xtal	03/04/08	DK
D2	- Replaced Freescale silicon with ITC compliant MCF52277CVM160J	03/30/10	DK
D3	Updated default switch and jumper settings	06/04/10	DK
D4	Added text regarding BOOTMOD pins connected to SDVDD	02/09/11	DK

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Designer: DANIEL KRUCZEK	Drawing Title: MUSHU/M52277EVb		
Drawn by: DANIEL KRUCZEK	Page Title: TITLE PAGE		
Approved: DANIEL KRUCZEK	Size C	Document Number PDF: SPF-22149 SOURCE: SCH-22149	Rev D4
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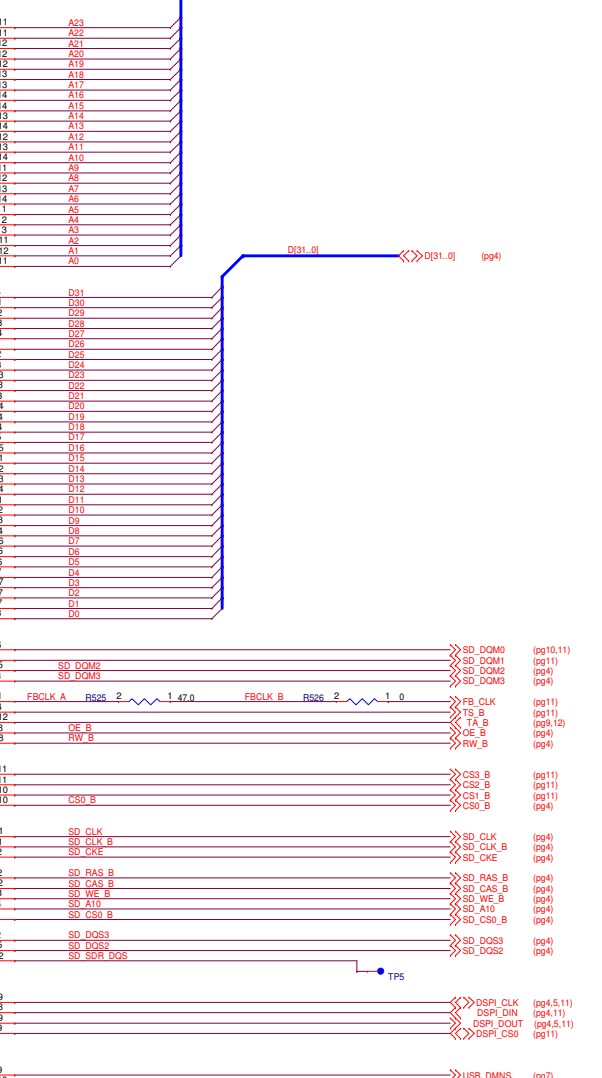
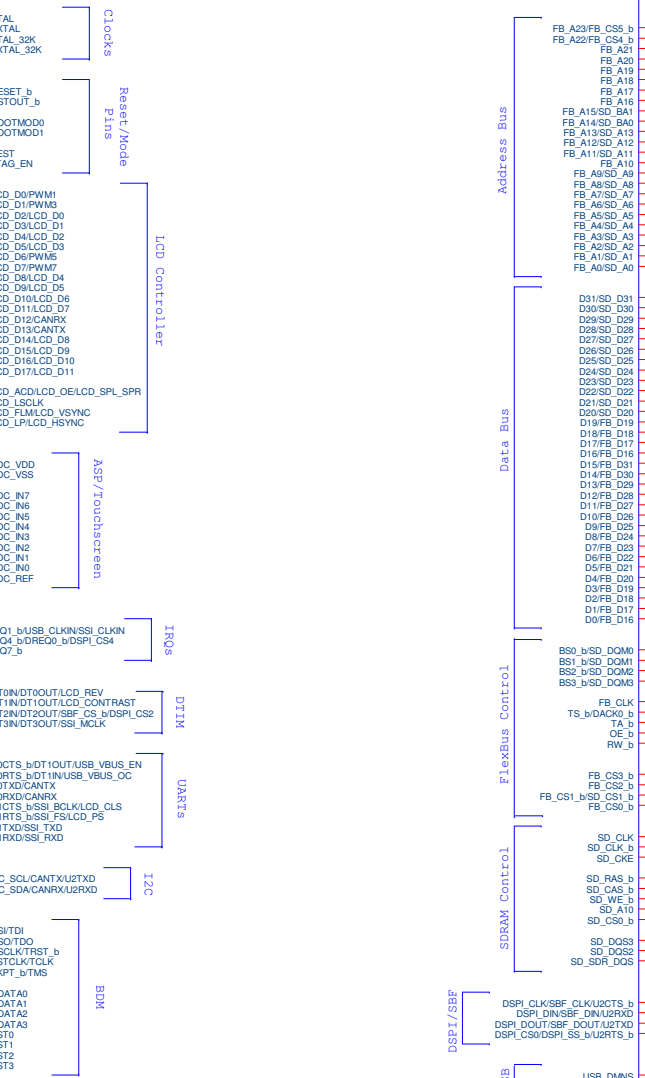
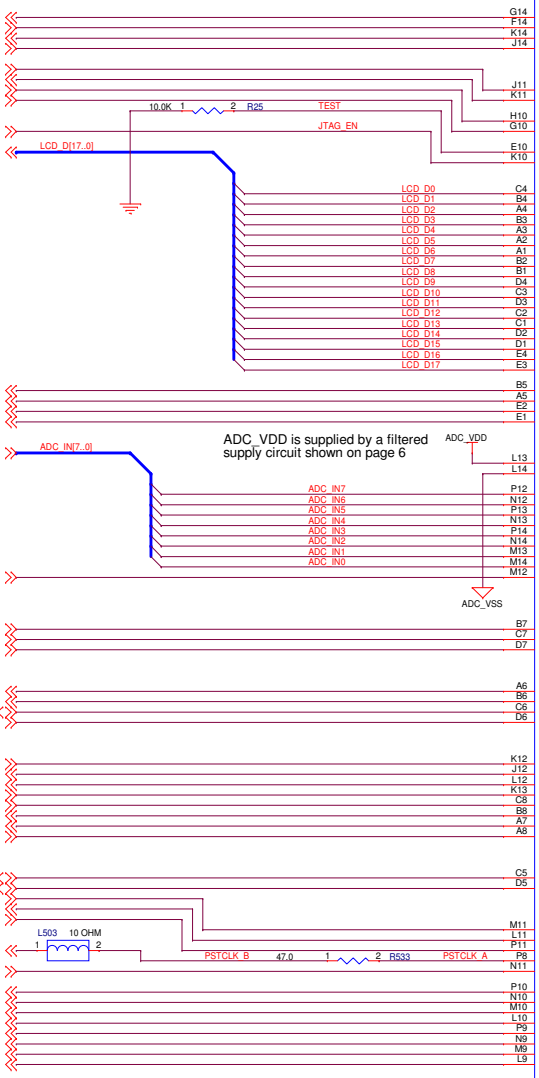
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Drawing Title: MUSHU/M52277EVB			
Page Title: NOTES			
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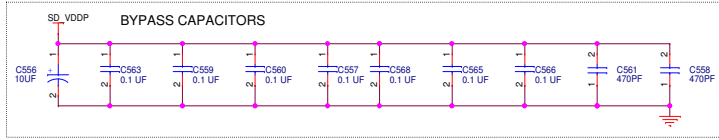
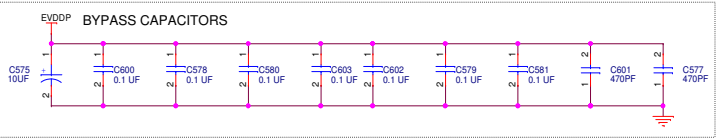


PLL_VDD, RTC_VDD and OSC_VDD are supplied by the filtered supply circuits shown on page 6

- (pg9) XTAL
- (pg9) EXTAL
- (pg9) XTAL_32K
- (pg9) EXTAL_32K
- (pg8) RESET_B
- (pg8) RSTOUT_B
- (pg8,8,11) BOOTMOD0
- (pg8) BOOTMOD1
- (pg9) JTAG_EN
- (pg10,11) LCD_D[17..0]
- (pg10,11) LCD_SPL_SPR
- (pg10,11) LCD_LSCLK
- (pg10,11) LCD_VSYNC
- (pg10,11) LCD_HSVC
- (pg7,10,11) ADC_IN[7..0]
- (pg7) ADC_REF
- (pg11) IRQ1_B
- (pg11) IRQ4_B
- (pg8) IRQ7_B
- (pg7,10,11) LCD_REV
- (pg7,10,11) LCD_CONTRAST
- (pg4) DT2N/DSPI_CS2
- (pg5,7) DT3N
- (pg7) U0CTS_B
- (pg7) U0RTS_B/USB_VBUS_OC
- (pg7) U0TXD
- (pg7) U0RXD
- (pg7,11) U0CTS_B/LCD_CLS
- (pg7,11) U0RTS_B/LCD_PS
- (pg5) U1TXD/SSI_TXD
- (pg5) U1RXD/SSI_RXD
- (pg7) I2C_SCL/CANRX
- (pg7) I2C_SDA/CANRX
- (pg12) DSI
- (pg12) DSO
- (pg12) DSCLK
- (pg12) PSTCLK/CLK
- (pg12) BKPT_B
- (pg9) DDATA0
- (pg9) DDATA1
- (pg9) DDATA2
- (pg9) DDATA3
- (pg12) PST0
- (pg12) PST1
- (pg12) PST2
- (pg12) PST3



Recommended Socket: Emulation Technology BPW-196-3BG014B-30



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SEMICONDUCTOR

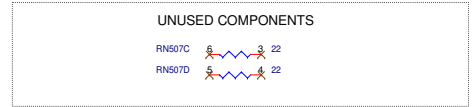
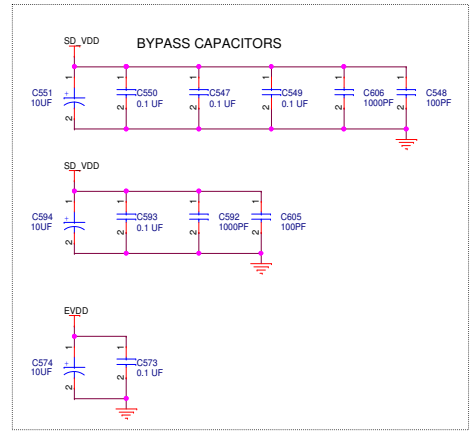
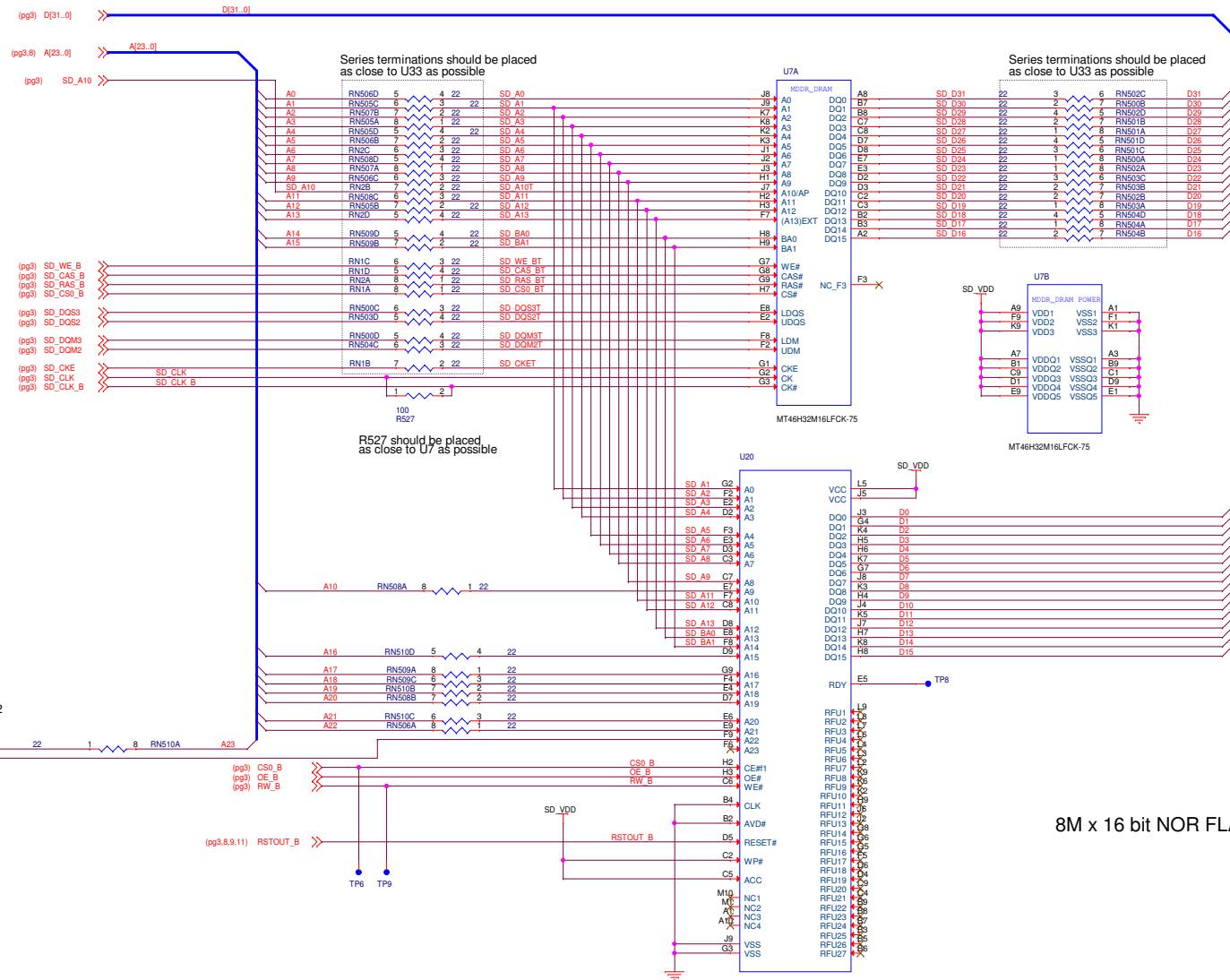
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Page Title: **MCF5227X PROCESSOR**

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32M x 16 bit MOBILE DDR



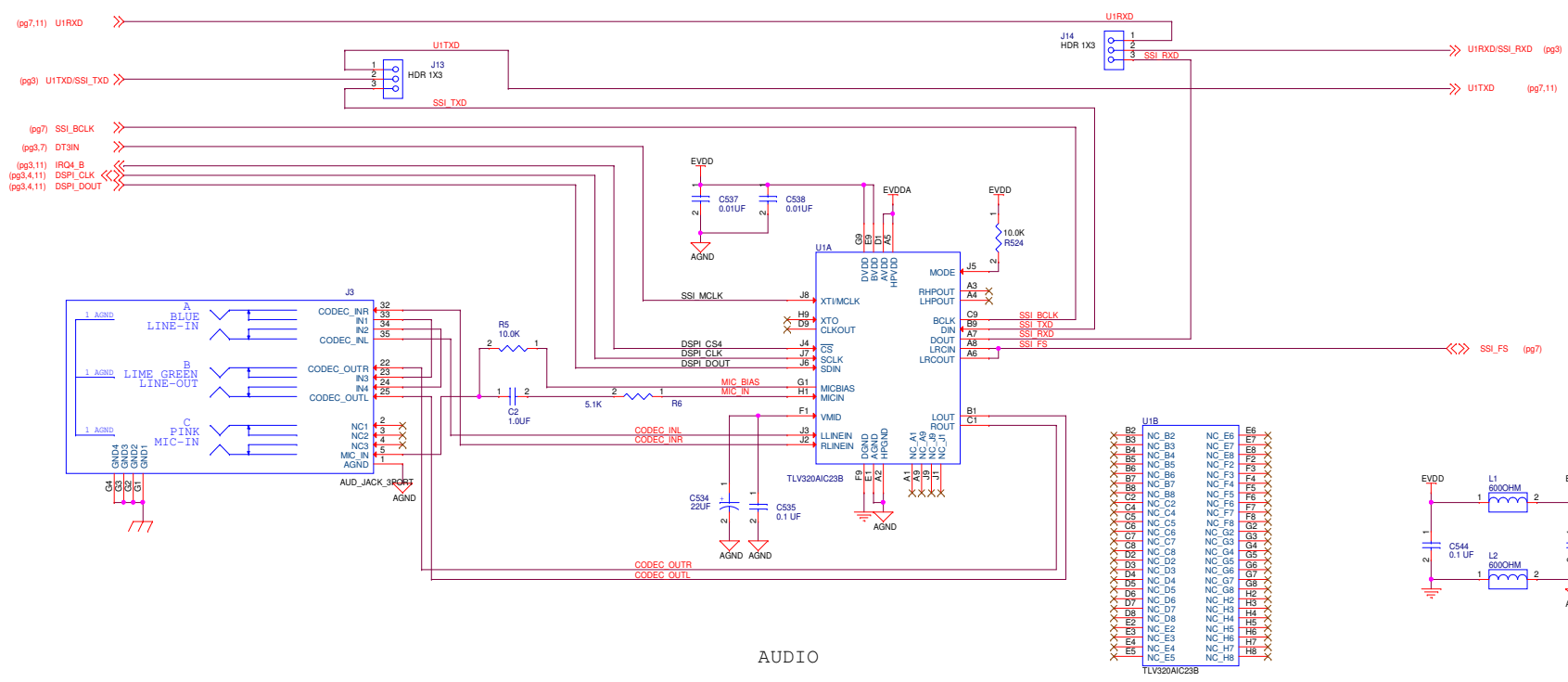
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Drawing Title: **MUSHU/M52277EVB**


Page Title: **MEMORY**

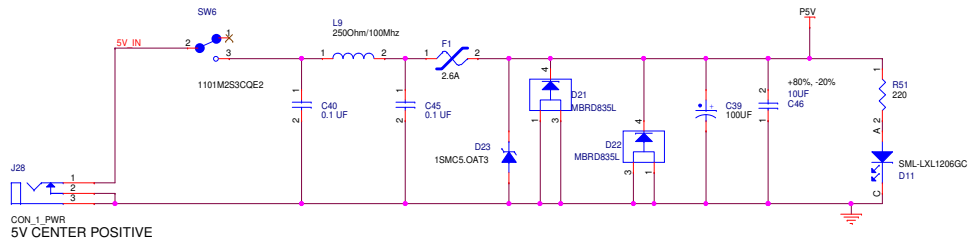
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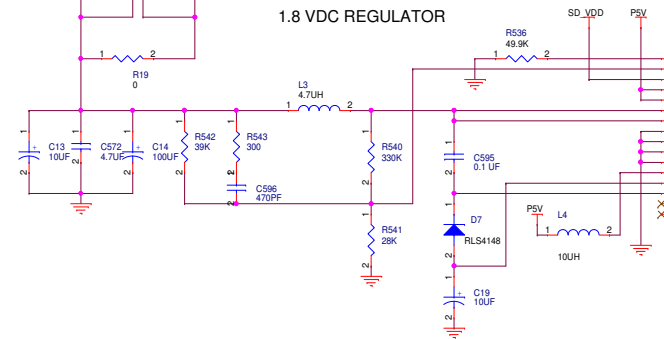
AUDIO

 semiconductor			
Drawing Title: MUSHU/M5227EVb			
Page Title: AUDIO CODEC			
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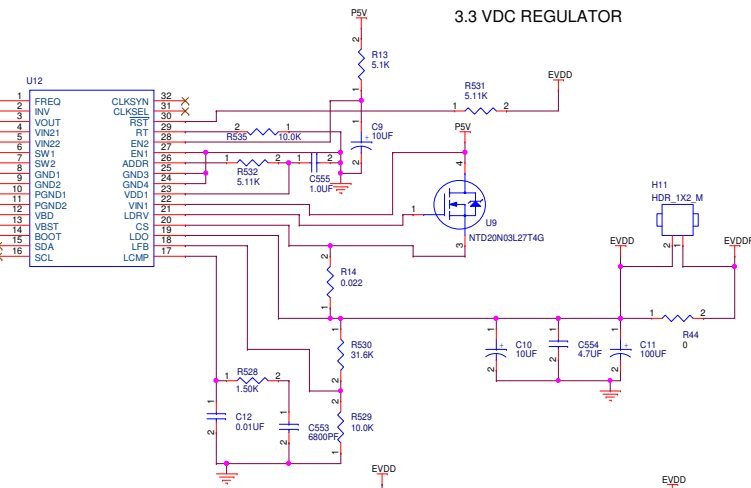


CON_1_PWR
5V CENTER POSITIVE

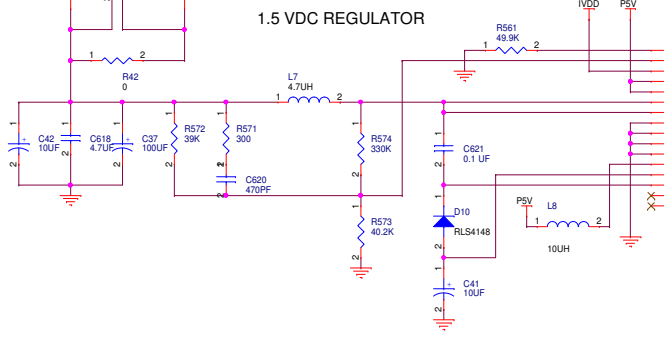
1.8 VDC REGULATOR



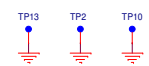
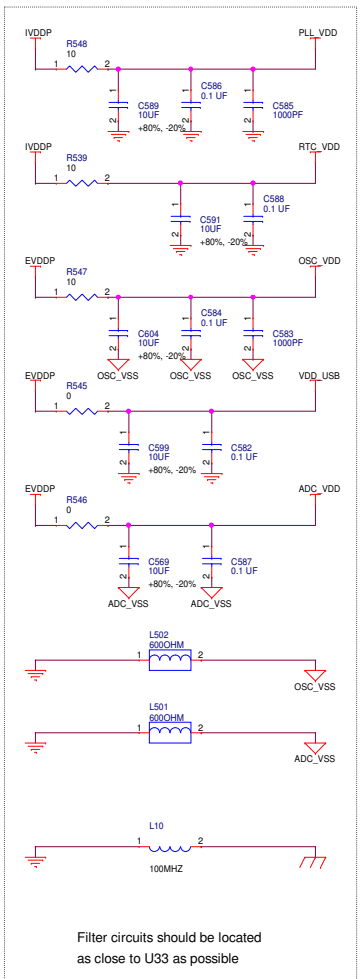
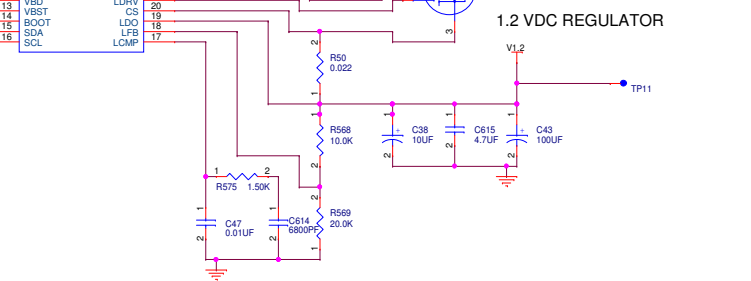
3.3 VDC REGULATOR



1.5 VDC REGULATOR

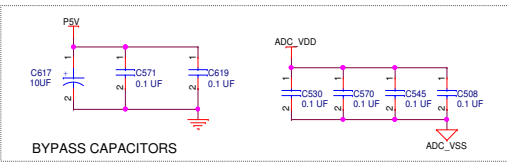


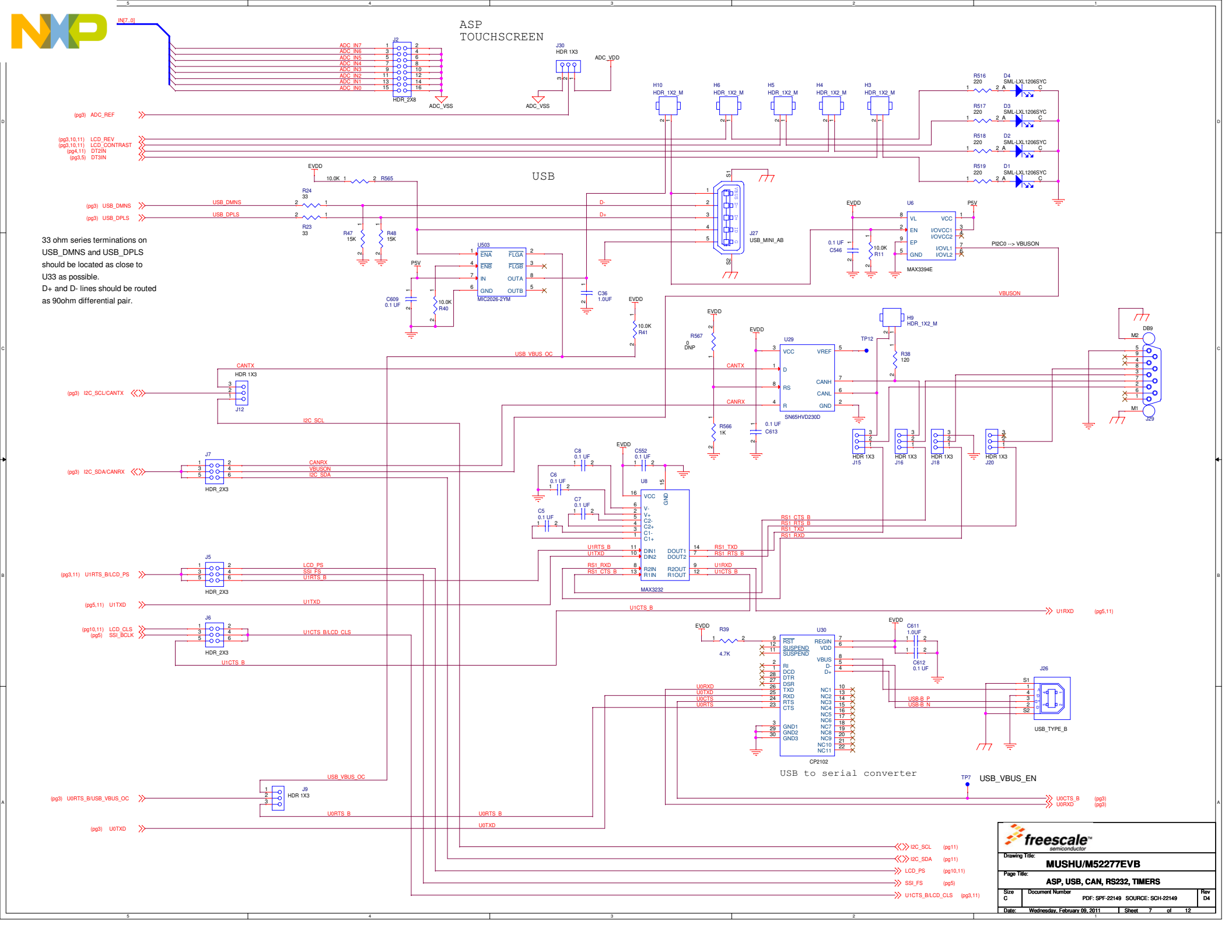
1.2 VDC REGULATOR



Filter circuits should be located as close to U33 as possible

Note: All power rails ending in "P" are dedicated M52277 supplies. The header and 0 ohm resistor facilitate current measurement on these supplies.





ASP TOUCHSCREEN

USB

USB to serial converter

33 ohm series terminations on USB_DMNS and USB_DPLS should be located as close to U33 as possible. D+ and D- lines should be routed as 90ohm differential pair.

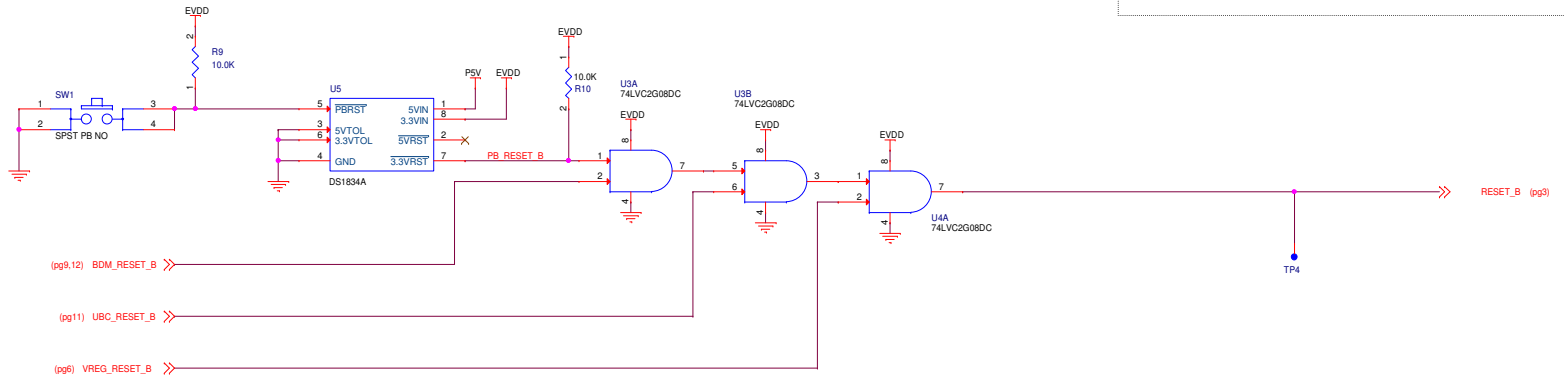
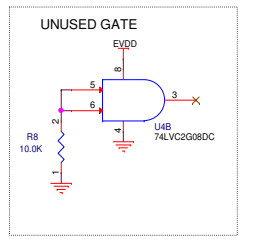
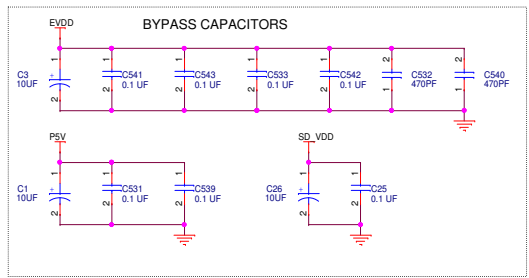
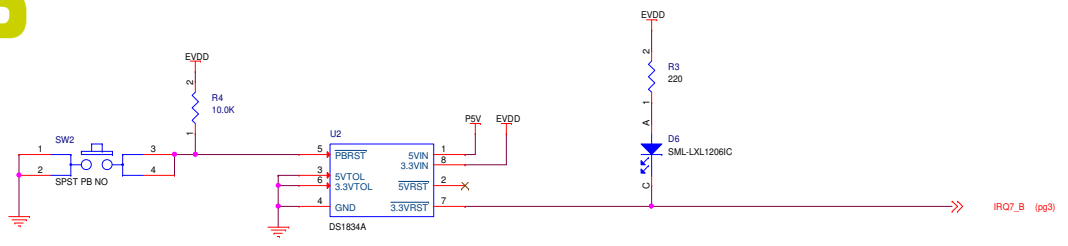
freescale
 semiconductors

Drawing Title: **MUSHUM52277EVB**

Page Title: **ASP, USB, CAN, RS232, TIMERS**

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- <<< I2C_SCL (pg11)
- <<< I2C_SDA (pg11)
- <<< LCD_PS (pg10,11)
- <<< SSI_FS (pg9)
- <<< UICTS_B_LCD_CLS (pg3,11)



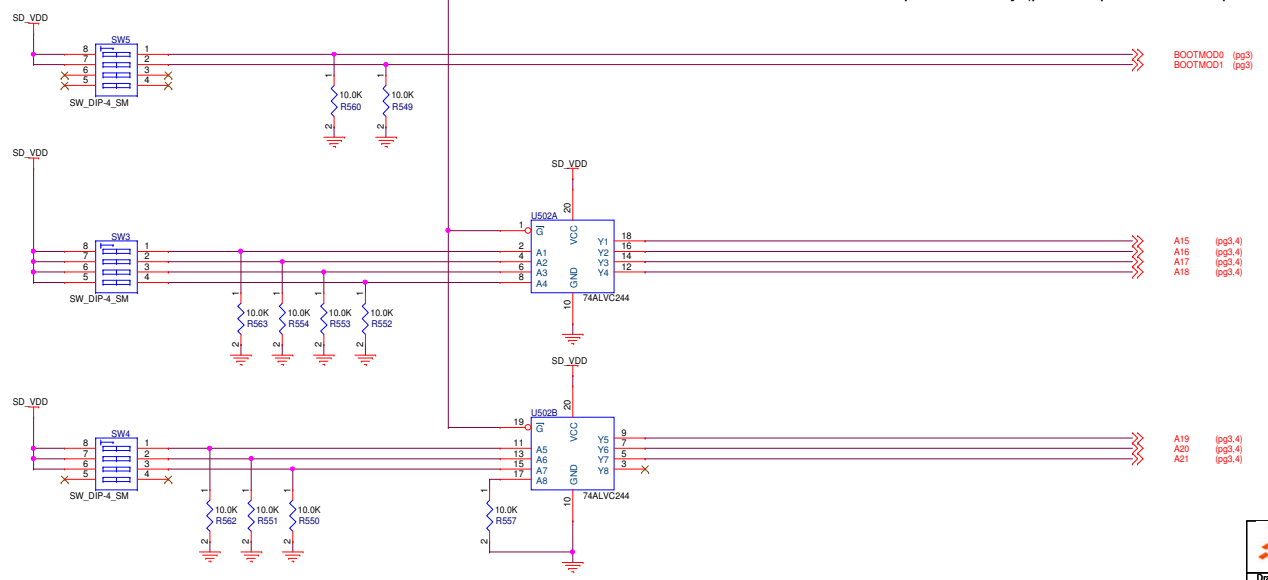
(pg9.12) BDM_RESET_B >>
 (pg11) UBC_RESET_B >>
 (pg6) VREG_RESET_B >>



WARNING: The BOOTMOD[1:0] signals are part of the EVDD domain, so they should have been pulled up through the switches to the 3.3V EVDD domain instead of the 1.8V SDVDD. No functional issues have been seen on the EVB as a result of this misconnection, but customers who are using this design as a reference should make sure to connect the BOOTMOD[1:0] pins correctly (pulled up to 3.3V and pulled down to GND as needed).

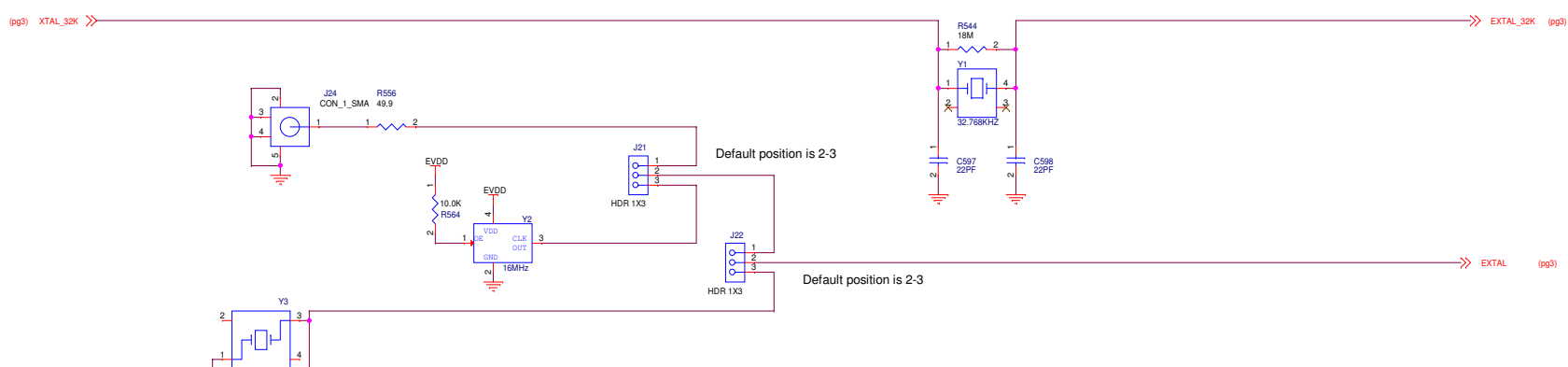
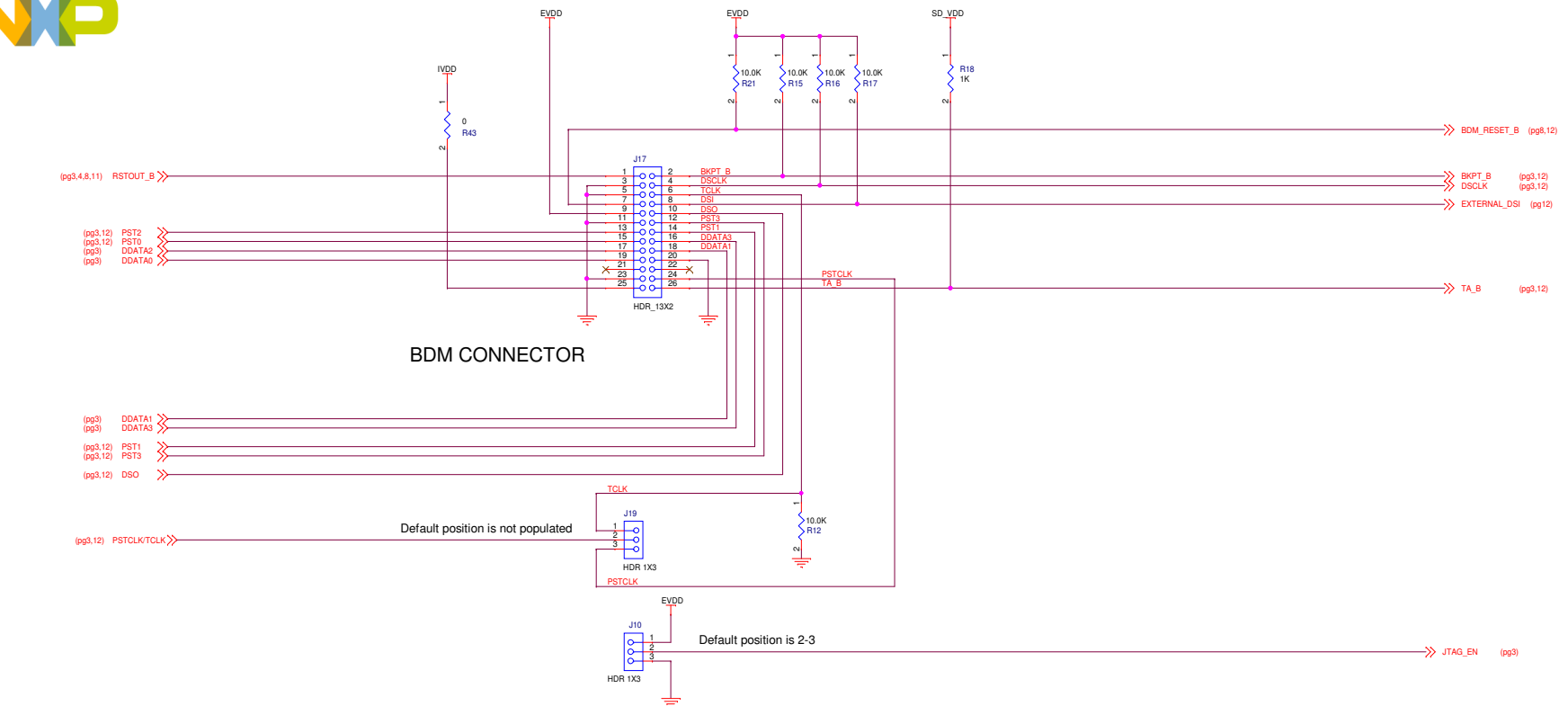
Default Switch Set-Up

- SW5-1 = ON >> BOOTMOD0 = 1
- SW5-2 = OFF >> BOOTMOD1 = 0
- SW3-1 = ON >> A15 = 1
- SW3-2 = ON >> A16 = 1
- SW3-3 = ON >> A17 = 1
- SW4-4 = ON >> A18 = 1
- SW4-1 = OFF >> A19 = 0
- SW4-2 = OFF >> A20 = 0
- SW4-3 = OFF >> A21 = 0
- SW4-4 = OFF >> Not Connected

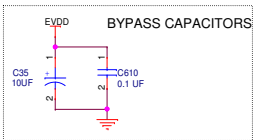


BOOTMOD0 (pg3)
 BOOTMOD1 (pg3)
 A15 (pg3,4)
 A16 (pg3,4)
 A17 (pg3,4)
 A18 (pg3,4)
 A19 (pg3,4)
 A20 (pg3,4)
 A21 (pg3,4)

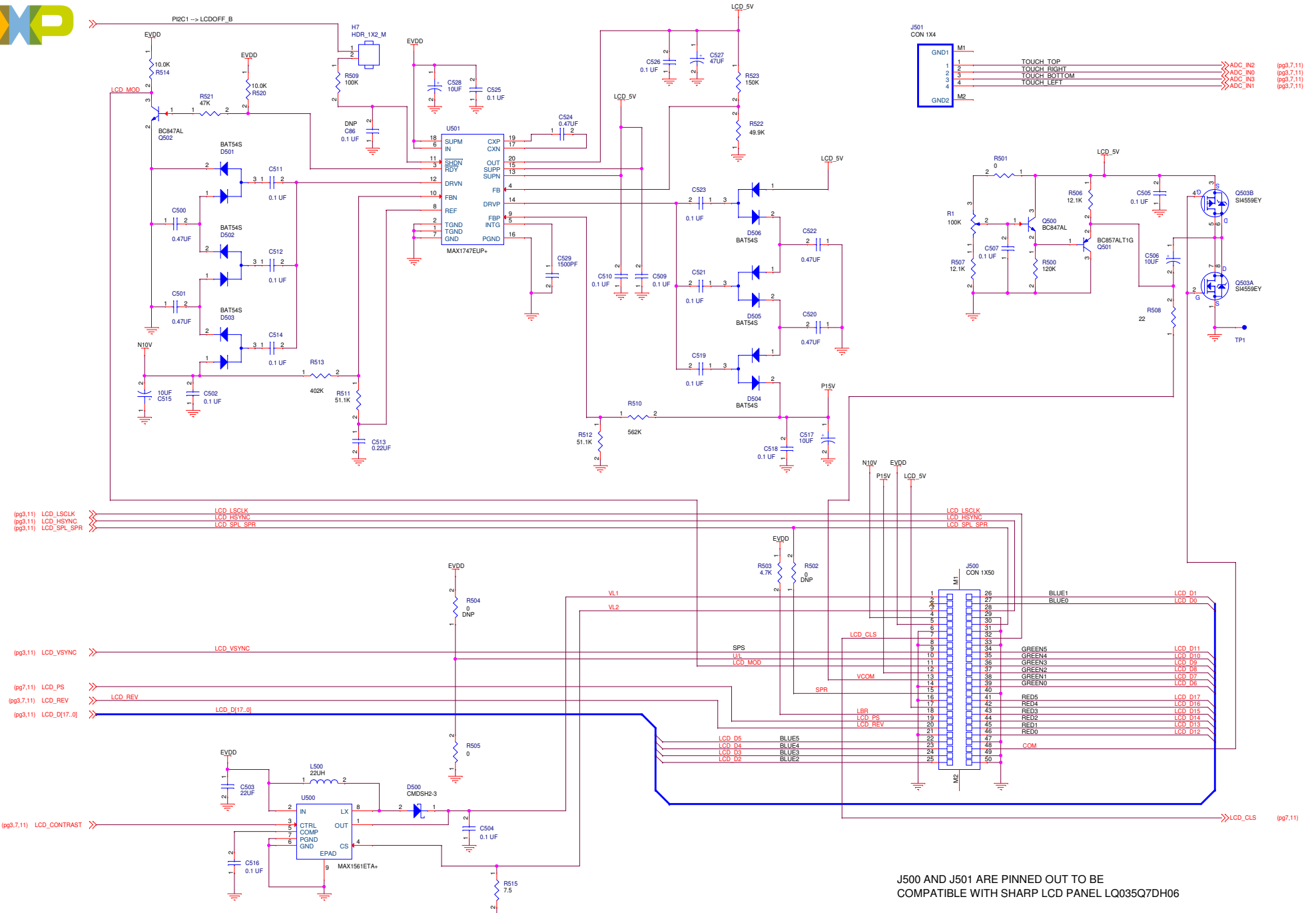
MUSHU/M52277EVB	
RESET AND IRQ	
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All clock lines should be routed as short as possible



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J500 AND J501 ARE PINNED OUT TO BE COMPATIBLE WITH SHARP LCD PANEL LQ035Q7DH06

(pg3.7.11) LCD_LCLK
(pg3.7.11) LCD_HSYNC
(pg3.7.11) LCD_SPL_SPR

(pg3.7.11) LCD_VSYNC
(pg7.11) LCD_PS
(pg3.7.11) LCD_REV
(pg3.7.11) LCD_D[17..0]

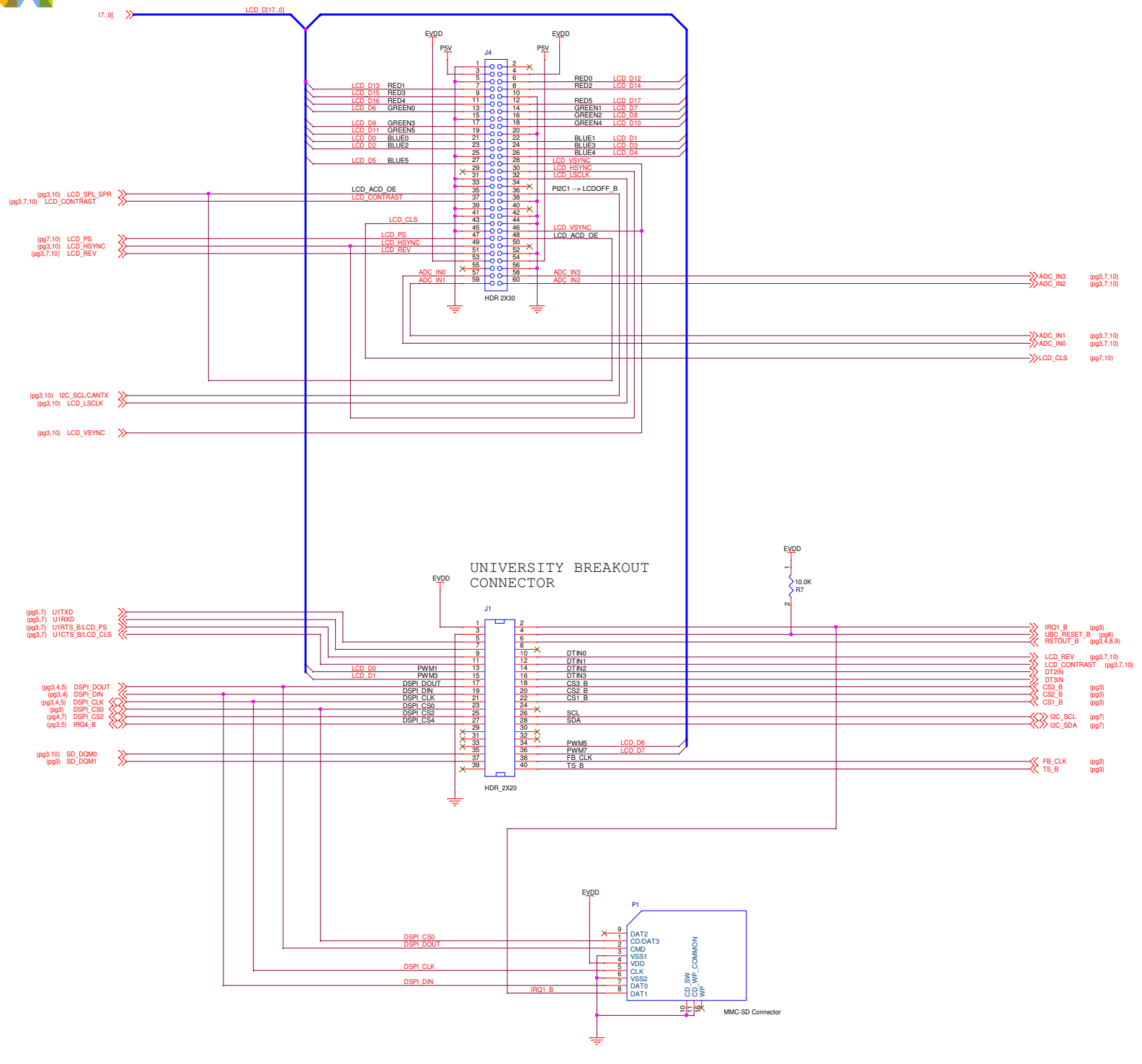
(pg3.7.11) LCD_CONTRAST

(pg3.7.11) ADC_IN2
(pg3.7.11) ADC_IN0
(pg3.7.11) ADC_IN3
(pg3.7.11) ADC_IN1

(pg7.11)



LOGICPD LCD CONNECTOR



freescale
semiconductor

Drawing Title: **MUSHU/M52277EVB**

Page Title: **LCD AND SERIAL IO CONNECTORS**

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**P&E Microcomputer Systems
USB Cold Fire Multilink BDM Interface**

- CF_RESET >> BDM_RESET_B (pg8,9)
- CF_TEA >> TA_B (pg3,9)
- CF_DSO << DSO (pg3,9)

- CF_FREEZE << PSTCLK/TCLK (pg3,9)
- CF_DSCLK >> DSCLK (pg3,9)
- CF_BKPT >> BKPT_B (pg3,9)
- PST0 << PST0 (pg3,9)
- PST1 << PST1 (pg3,9)
- PST2 << PST2 (pg3,9)
- PST3 << PST3 (pg3,9)

- CF_DSI >> DSI (pg3)
- EXTERNAL_DSI << EXTERNAL_DSI (pg9)

Drawing Title:			
MUSHU/M52277EVB			
Page Title:			
P&E BDM BLOCK			
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