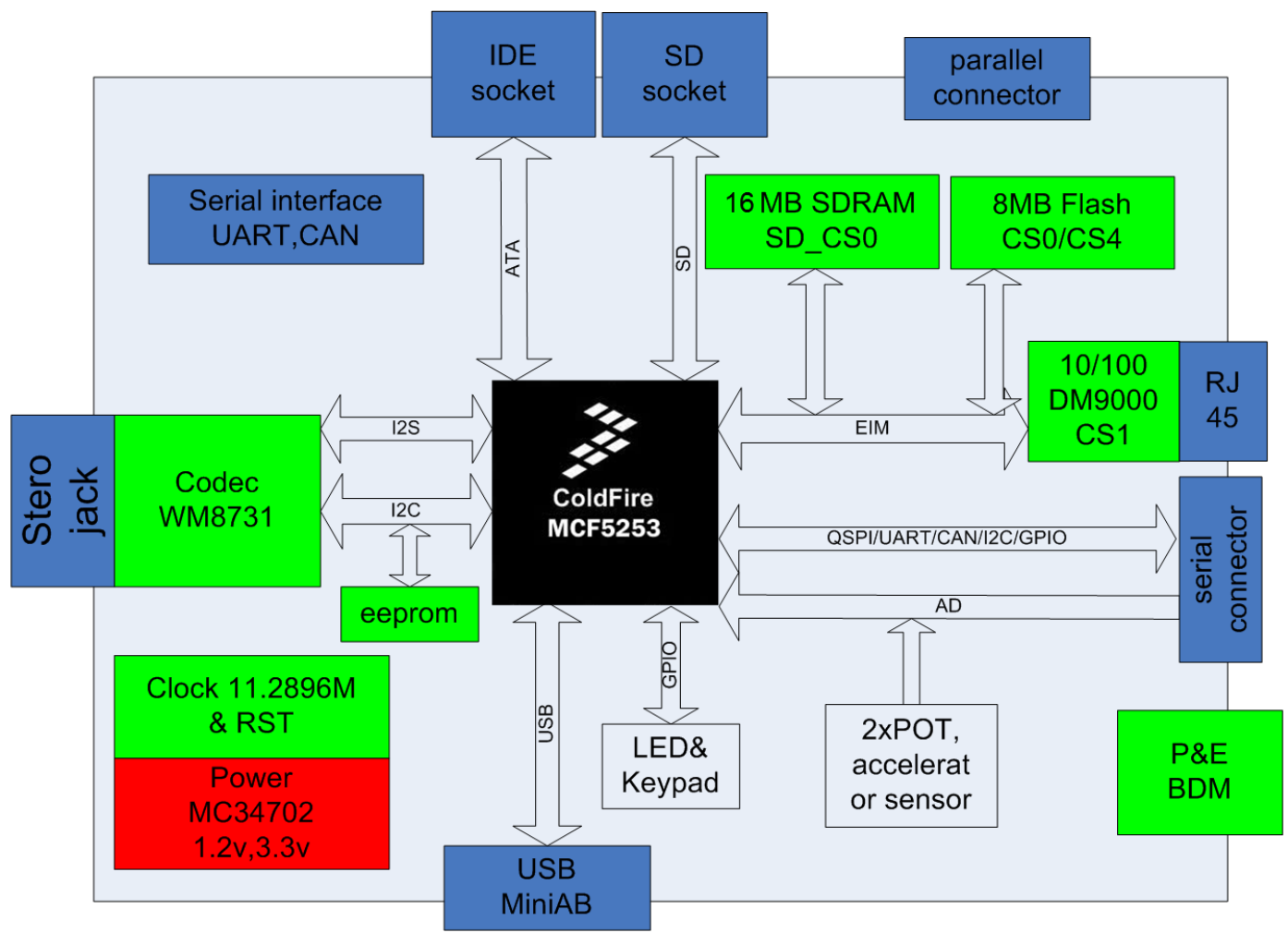


1	Table of Contents
2	Introduction
3	Hardware
4	Software
5	Test
6	Ethernet
7	Connectors
8	USB to BDM Block
9	Misc
10	Power


Block Diagram



Revisions			
Rev	Description	Date	Approved
X	Original Release	09/21/07	Tanis Qiu
X1	Formal Release	10/09/07	Tanis Qiu
X2	Re-sequenced Release to build	10/31/07	Tanis Qiu
X3	Add QSPI connector	11/06/07	Tanis Qiu
A	Remove QSPI connector pullup USB power enable signal to 5v by divider 5.1k/10k Disable USB power channel B Add 1M resistors to Y4, Y6, Y3 Add 0ohm resistor parallel with U2 DNP R25 and U2 add 68k resistors on SD change r51 to 0 ohm Pull up U5.28 Change designator of D8-D11 to LED1-4	01/07/08	Tanis Qiu
B	Change SDRAM from 32MB to 16MB. Swap RTS and CTS on UART buffer	02/18/08	Tanis Qiu
B1	Correct SD_DATA1 and SD_DATA3 connection Change R149 from pull up to pull down	02/16/09	Tanis Qiu
C	Release to rev C	02/23/09	Tanis Qiu



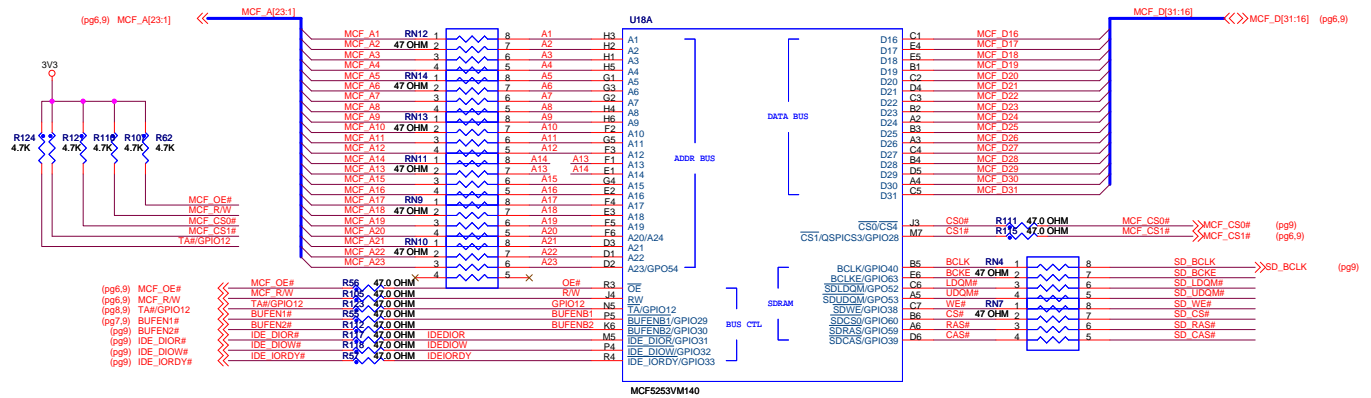
tors, capacitors and ferrite beads are 0603 package.

		
Drawing Title: M5253DEMO		
Page Title: Notes		
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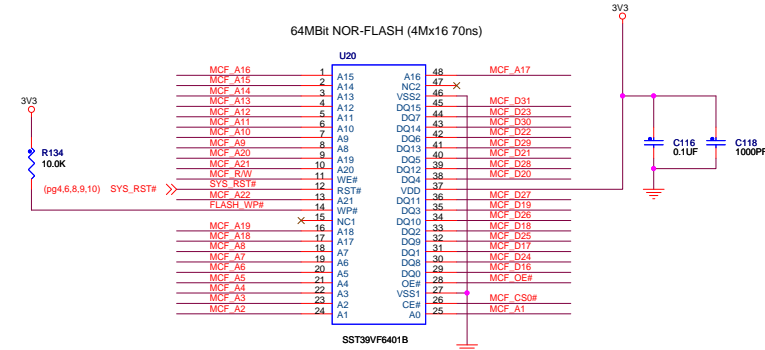
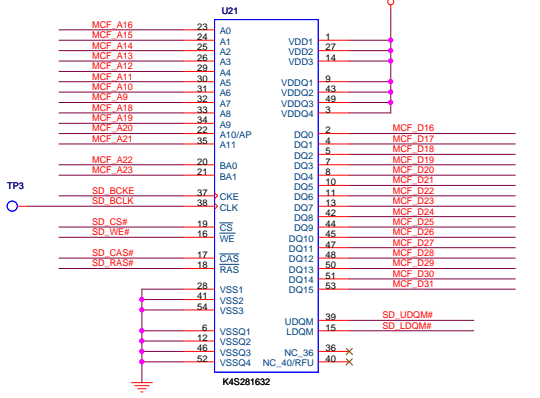
GPI012 << GPI012 (pg10)

Series terminations should be placed close to CPU

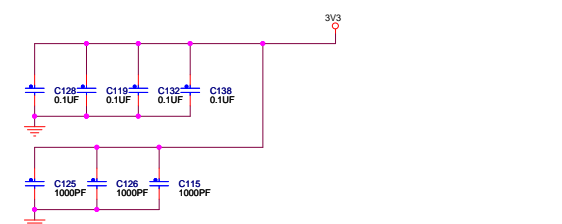


128Mbit SDRAM (8Mx16)

64Mbit NOR-FLASH (4Mx16 70ns)



MCF5253 Pins	A16	A15	A14	A13	A12	A11	A10	A9	A18	A19	A20	A21	A22	A23
Row	16	15	14	13	12	11	10	9	18	19	20	21	22	23
Column	1	2	3	4	5	6	7	8	17	-	-	-	-	-
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13



A23: 0 INTERNAL BOOTROM
1 BOOT FROM CS0 (default)

A20: 0 AUDIO CLK FROM CRIN PIN (default)
1 AUDIO CLK FROM LRCK3 PIN

freescale
semiconductor

Drawing Title: **M5253DEMO**

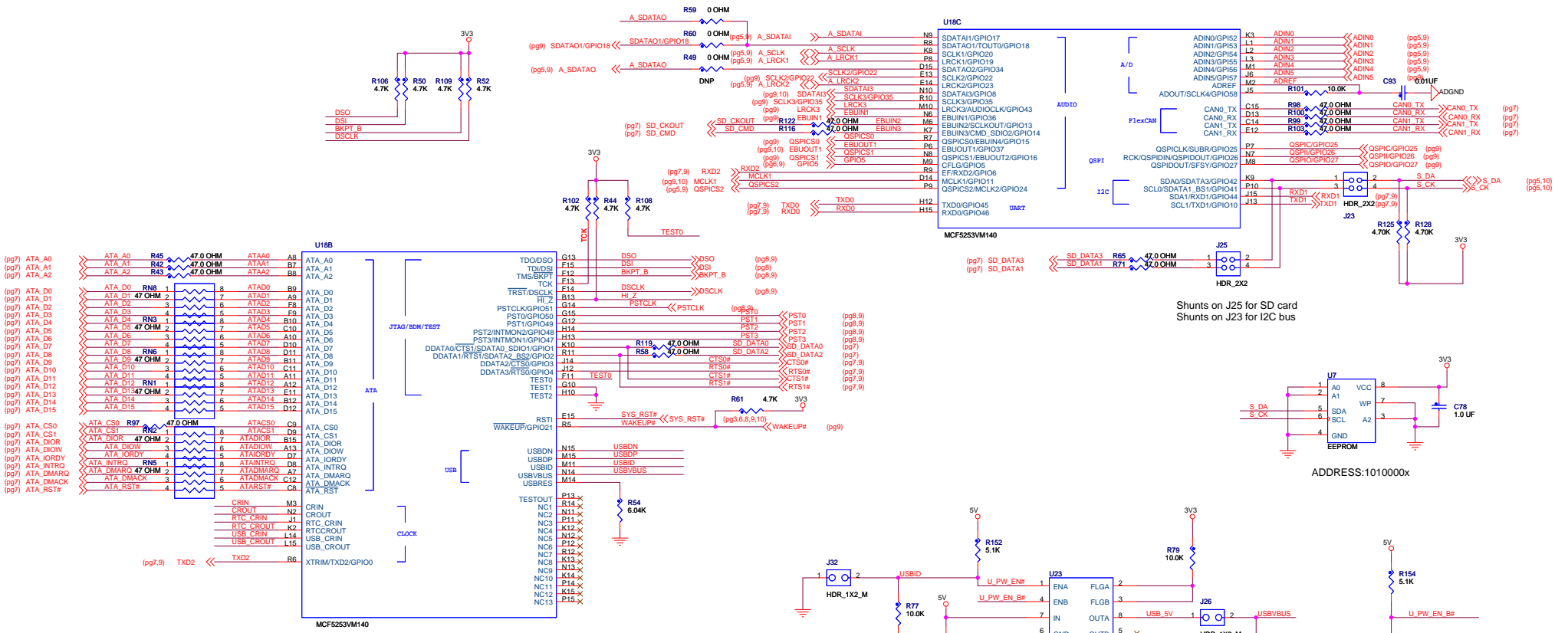
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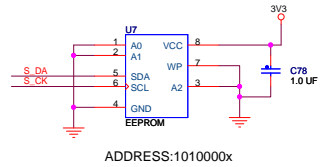
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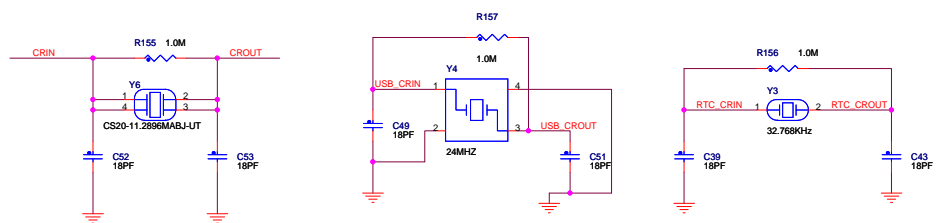
EBUIN2 << EBUIN2 (pg.9)
 EBUIN3 << EBUIN3 (pg.9)



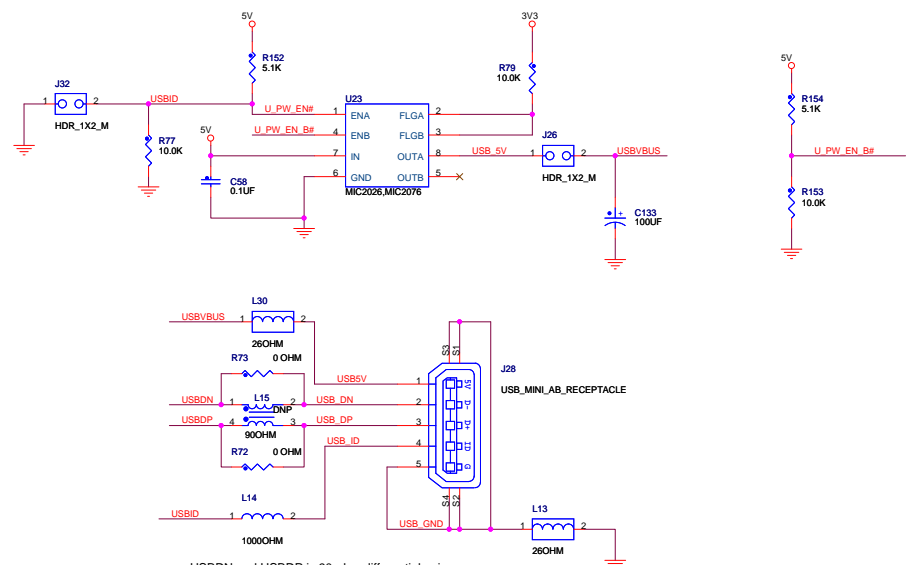
Shunts on J25 for SD card
 Shunts on J23 for I2C bus



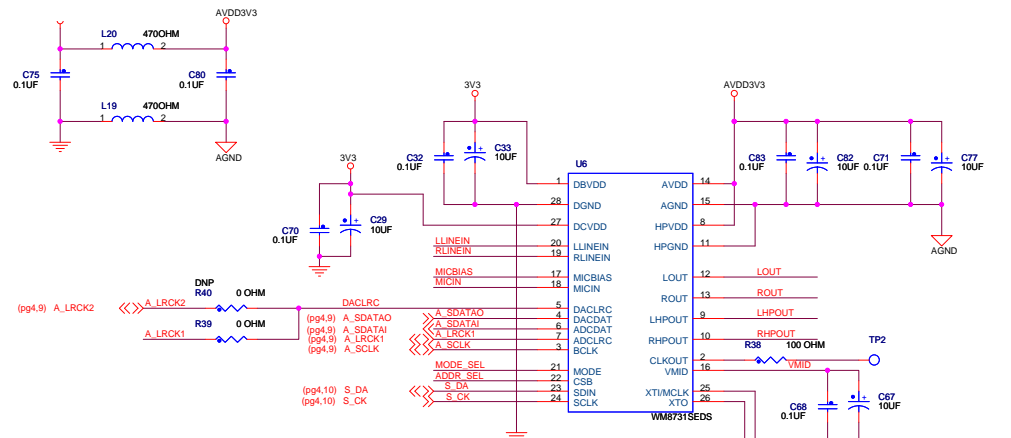
ADDRESS:1010000x



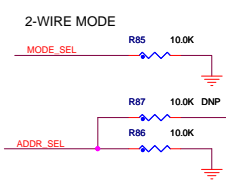
Place Crystals close to U18



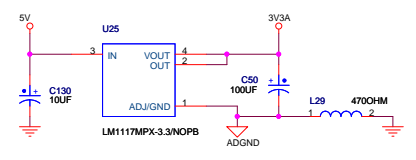
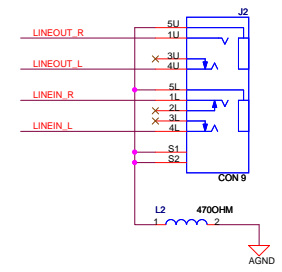
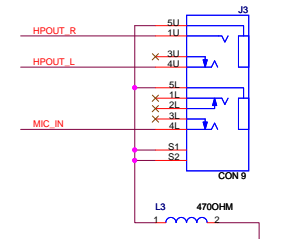
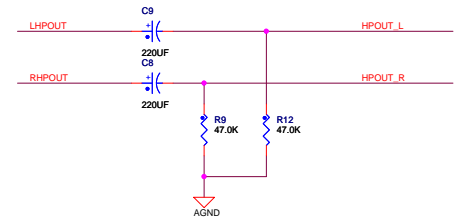
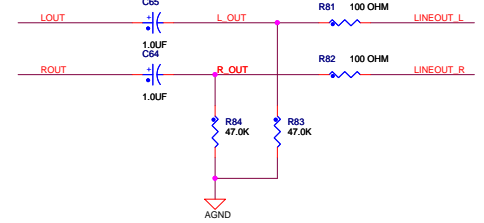
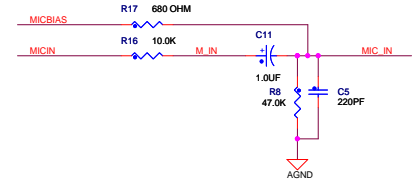
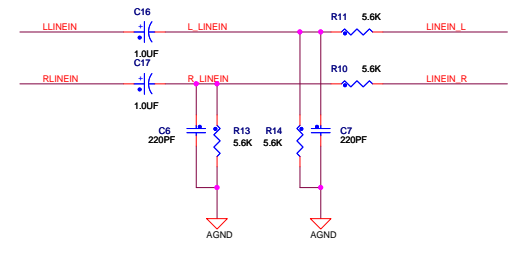
USBIDN and USBIDP is 90-ohm differential pair
 minimize vias and layer transition, reference to continuous GND plane
 L15 is reserved for EMI consideration
 R72, R73 and L15 should be close to J28.
 Try to overlap R72, R73 with L15 to minimize un-differential routing



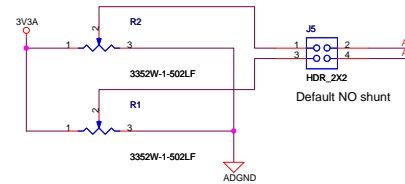
Analog signals should reference to AGND plane



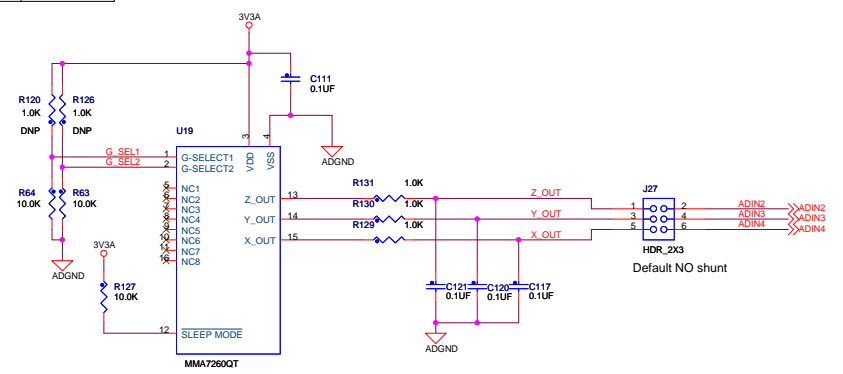
ADDR_SEL	ADDRESS
0 (default)	0011010x
1	0011011x



G_SEL1	G_SEL2	G RANGE	SENSITIVITY
0	0	1.5G	800MV/G
0	1	4G	300MV/G
1	0	2G	600MV/G
1	1	6G	200MV/G



Default NO shunt



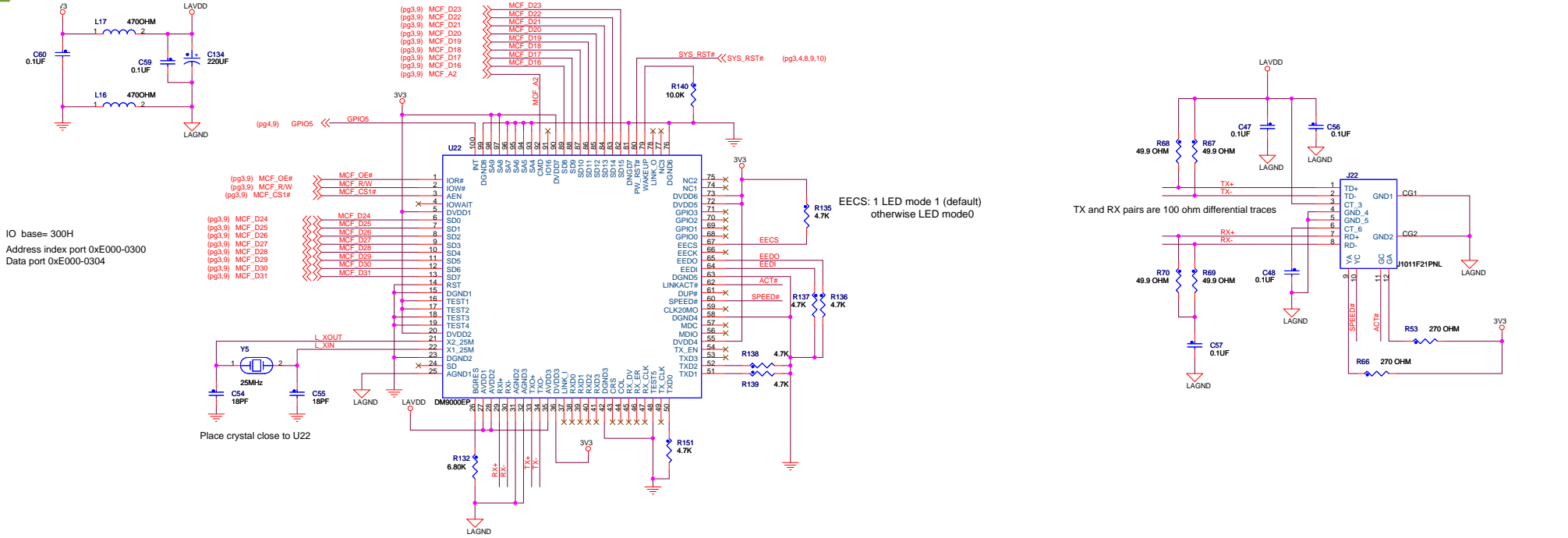
Default NO shunt

freescale
semiconductor

Drawing Title: **M5253DEMO**

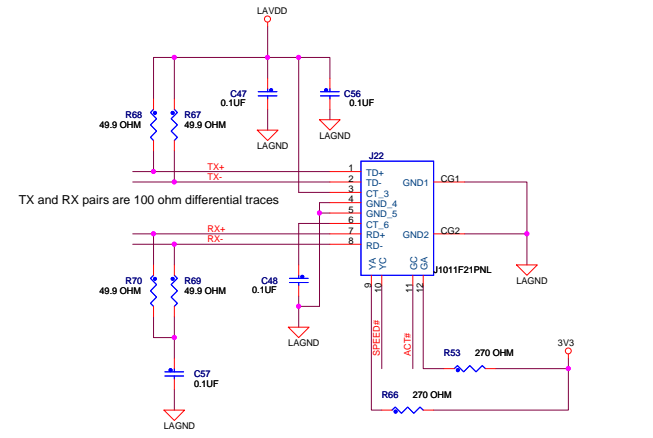
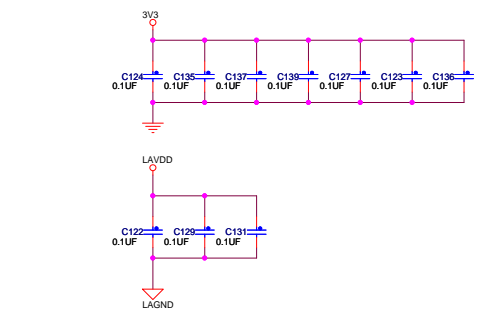
Page Title: **Audio**

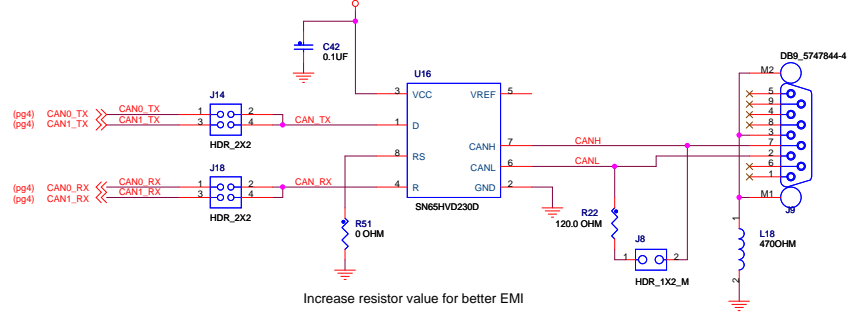
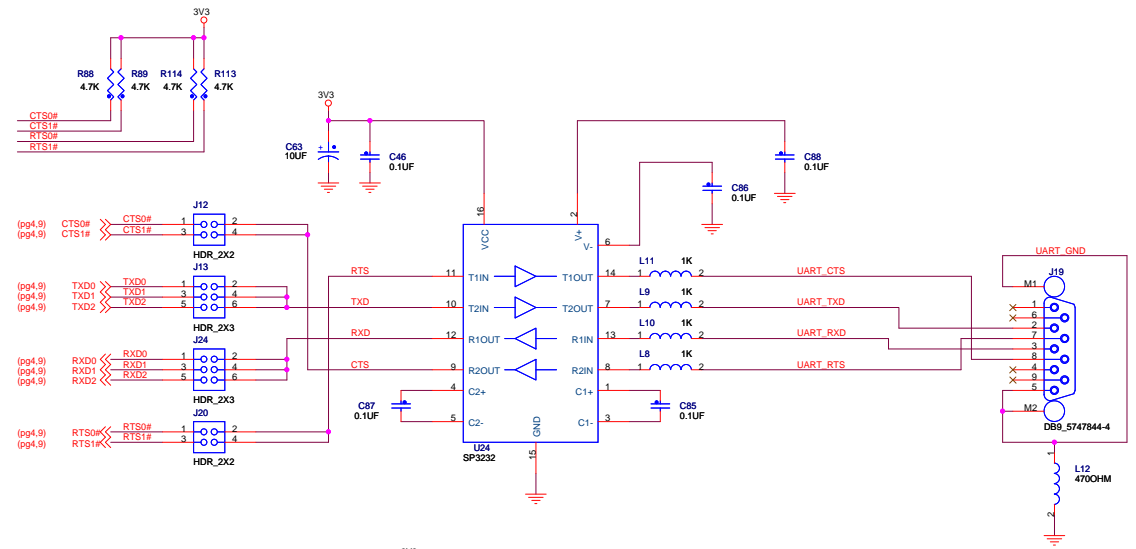
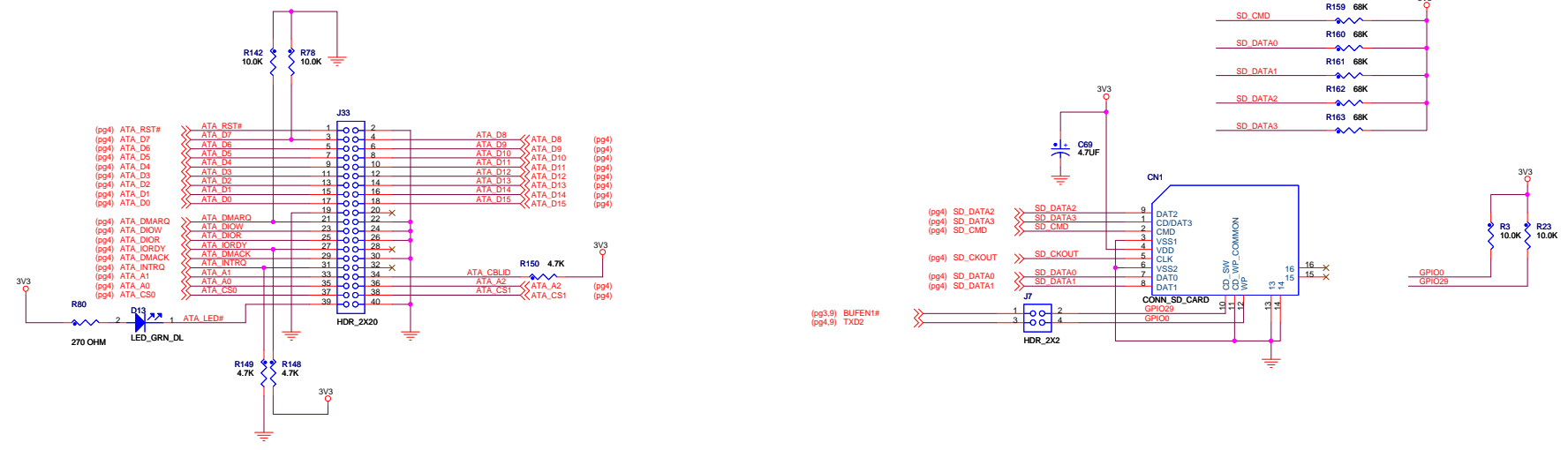
Size C	Document Number SCH-23837 PDF: SPF-23837	Rev C
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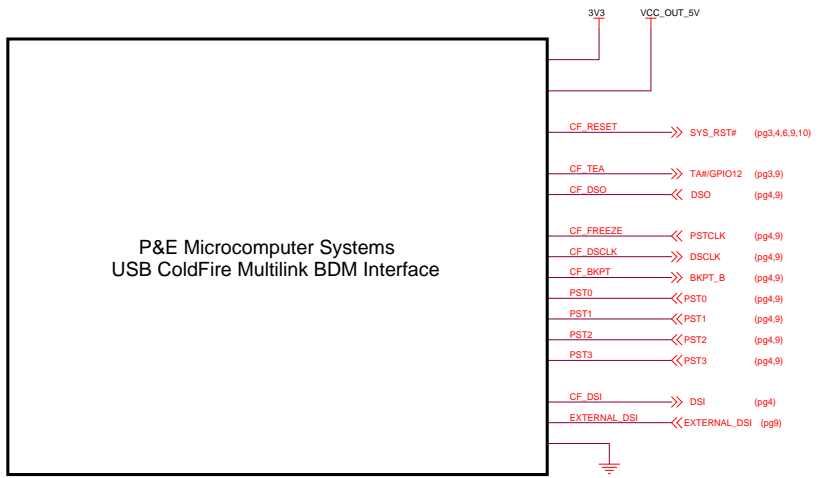
IO base= 300H
 Address index port 0xE000-0300
 Data port 0xE000-0304

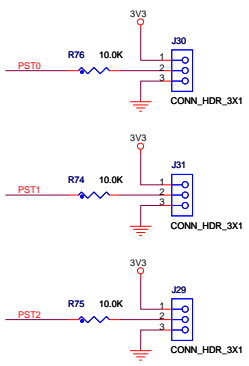
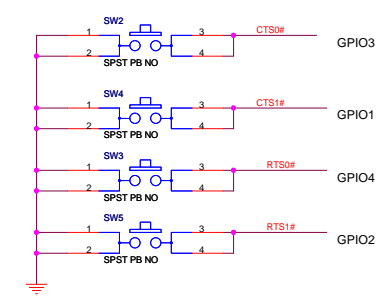
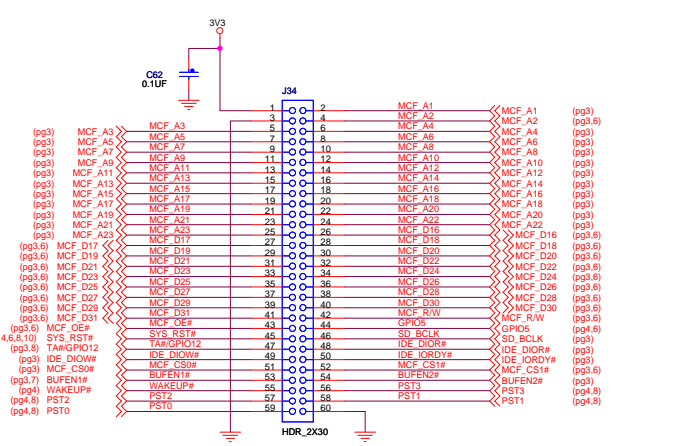
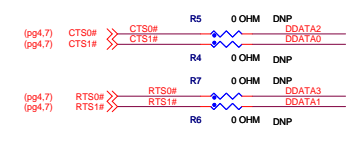
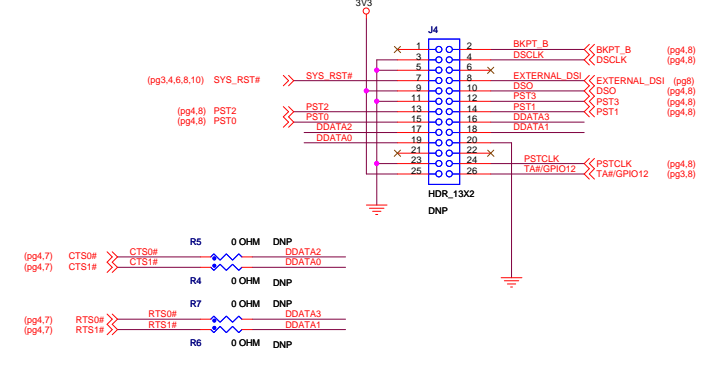
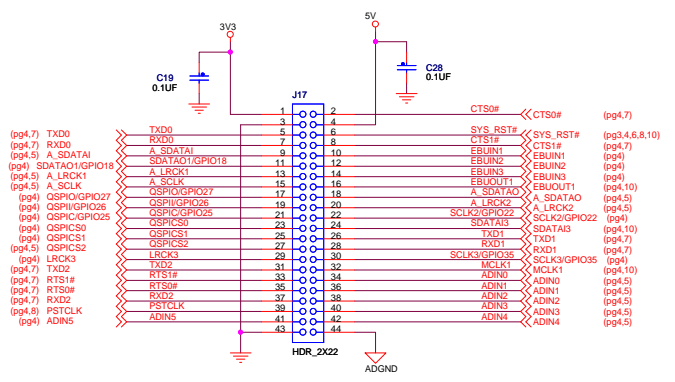
Place crystal close to U22





Increase resistor value for better EMI





BOOT MODE	PST0	PST1	PST2
I2C MASTER	0	0	0
SPI MASTER	0	0	1
IDE MASTER	0	1	0
I2C SLAVE	1	0	0
UART (5.6448/11.2896 MHz Xtal)	1	0	1
UART (8.4672/16.9344/33.8688 MHz Xtal)	1	1	0
UART (5/10/20 MHz Xtal)	1	1	1

Drawing Title: **M5253DEMO**

 Page Title: **Misc**

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