

Customer Evaluation Board [MAC57D5-516DC]

Table of Contents

Index	Page
Title & Notes	Page 1
Daughterboard connectors	Page 2
MCU Power Supply Section	Page 3
MCU Ports	Page 4
MCU Decoupling Capacitors	Page 5
Debug Section	Page 6
Clock	Page 7
DDR2	Page 8
DDR2 PWR Supply	Page 9
QuadSPI FLASH Memory	Page 10
LVDS Interface	Page 11

Revision Information

Rev	Date	Designer	Comments
0.1		Jesus Sanchez	Start of capture, Working version
X1		Jesus Sanchez	1st release for internal review (Complete Board)
X2		Jesus Sanchez	Version sent to Pre Layout, incorporating fixes from review
A		Jesus Sanchez	Post Layout (Back Annotated). Matches PCB RevA

CAUTION:

This schematic is provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale MAC57D5 family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

3 Different test points used in design:

TPVx - Through Hole Pad small

TPV?

TPHx - Through Hole Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TPH5

TP?

TPx - Surface Mount Wire Loop

Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in *ITALICS*

		Microcontroller Solutions Group 6501 William Cannon Drive West Austin, TX 78735-8598	
<small>This document contains information proprietary to Freescale Semiconductor and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of Freescale Semiconductor.</small>			
Designer: <i>Jesus Sanchez - B42964</i>		Drawing Title: MAC57D5-516DC	
Drawn by: <i>Jesus Sanchez - B42964</i>		Page Title: TITLE and NOTES	
Approved: Joseph Martinez	Size B	Document Number SCH-28806 PDF: SPF-28806	Rev A
Date: Wednesday, June 17, 2015		Sheet 1 of 11	

HALO 516BGA

PORT A

Table listing pins for PORT A (PA0-PA15) with pin numbers, names, and functions.

PORT B

Table listing pins for PORT B (PB0-PB15) with pin numbers, names, and functions.

PORT C

Table listing pins for PORT C (PC0-PC15) with pin numbers, names, and functions.

PORT M

Table listing pins for PORT M (PM0-PM15) with pin numbers, names, and functions.

PORT N

Table listing pins for PORT N (PN0-PN15) with pin numbers, names, and functions.

PORT G

Table listing pins for PORT G (PG0-PG15) with pin numbers, names, and functions.

PORT H

Table listing pins for PORT H (PH0-PH15) with pin numbers, names, and functions.

PORT J

Table listing pins for PORT J (PJ0-PJ15) with pin numbers, names, and functions.

PORT E

PORT F

PORT R

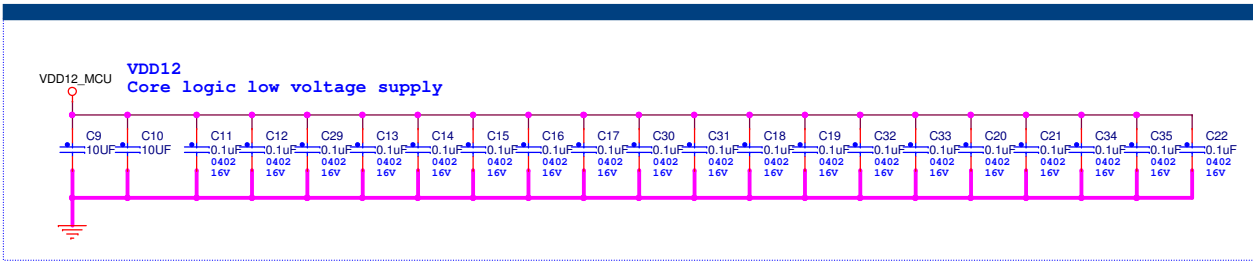
PORT S

PORT K

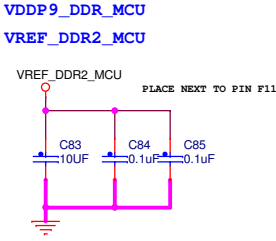
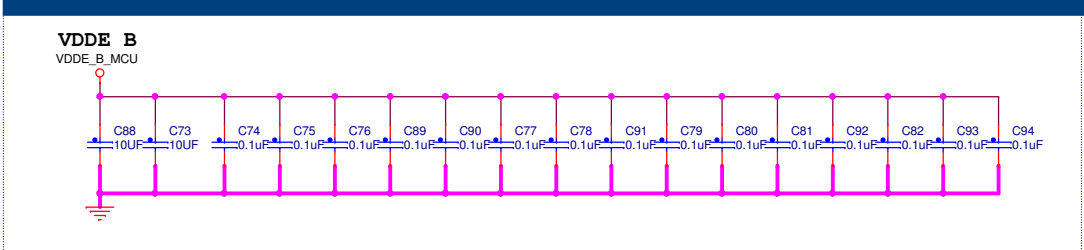
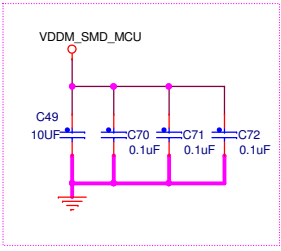
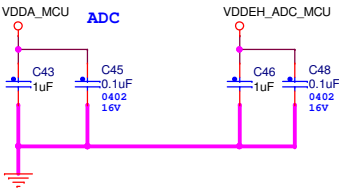
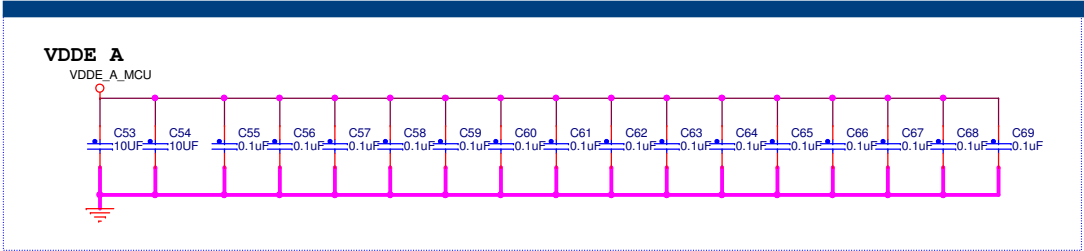
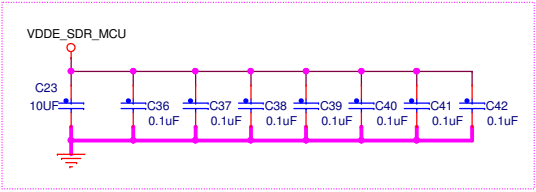
PORT L

Freescale logo and document information including part number MACS705-516DC, date, and version.

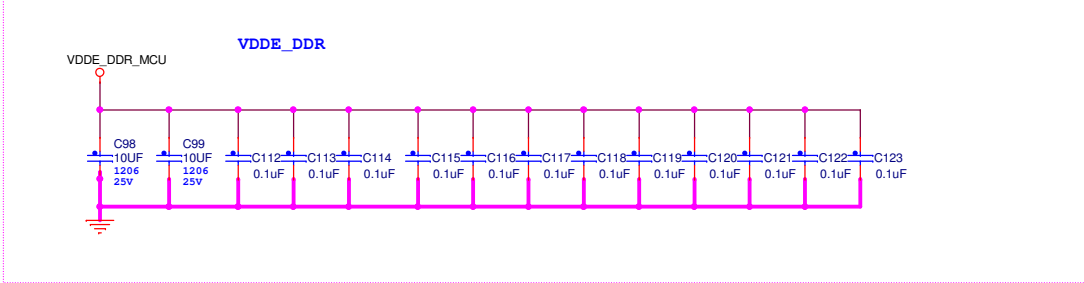
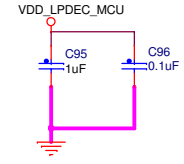
HALO MCU Decoupling and bulk storage



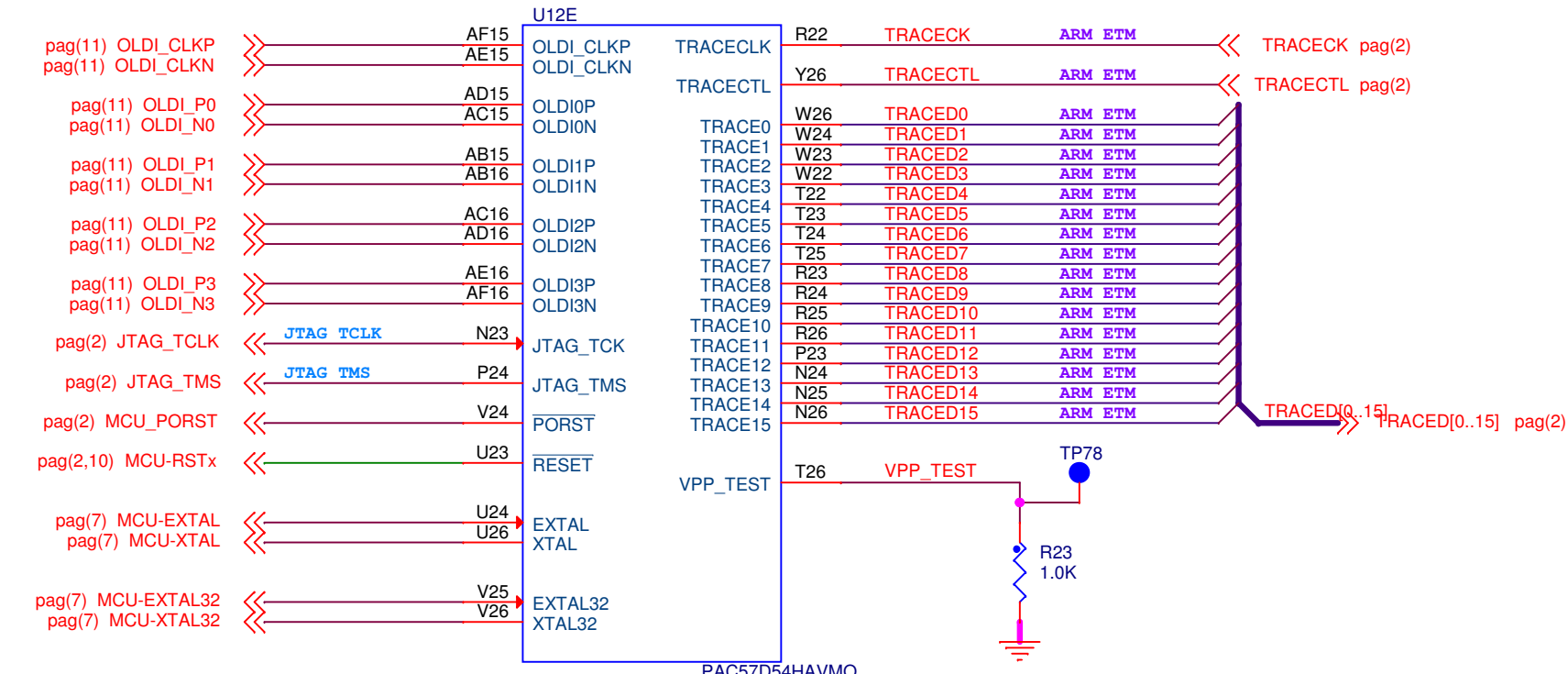
VDDE_SDR



VDD_LP_DEC Low power decoupling capacitors

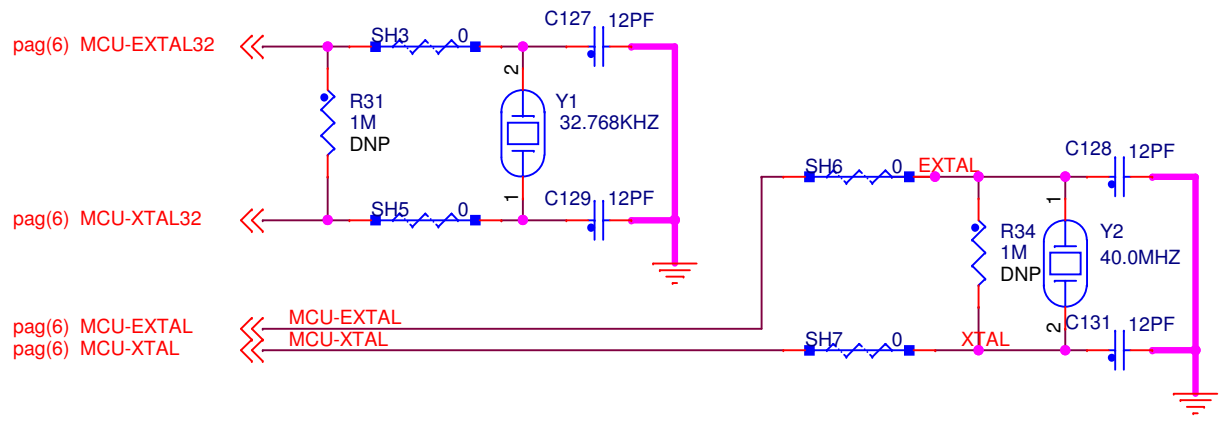


ICAP Classification: FCP: ____ FIUO: X PUBI: ____			
Drawing Title: MAC57D5-516DC			
Page Title: Decoupling Capacitors			
Size B	Document Number	SCH-28806 PDF: SPF-28806	Rev A
Date:	Wednesday, June 17, 2015	Sheet 5 of 11	



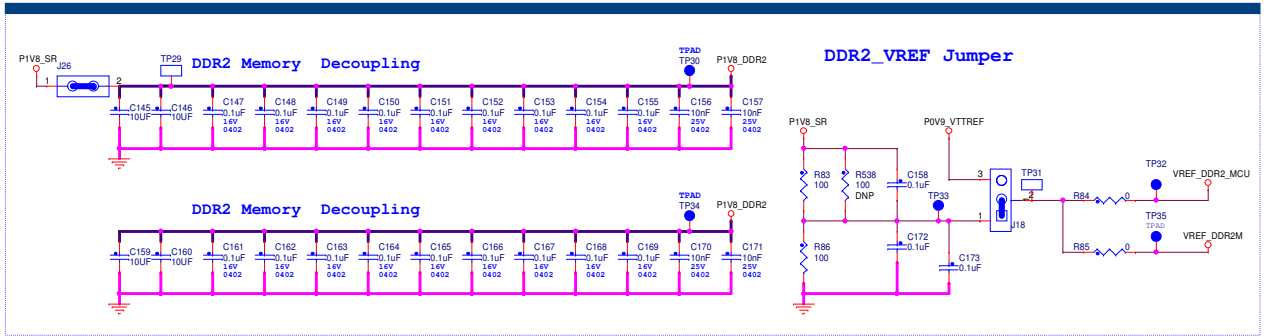
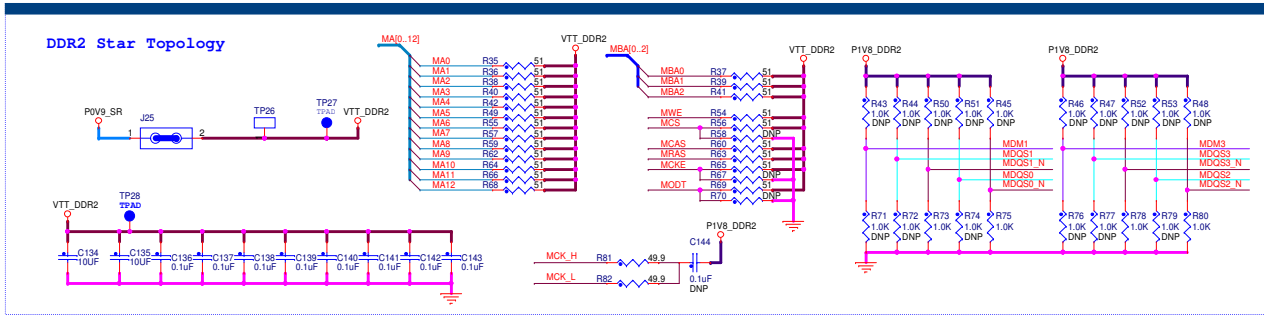
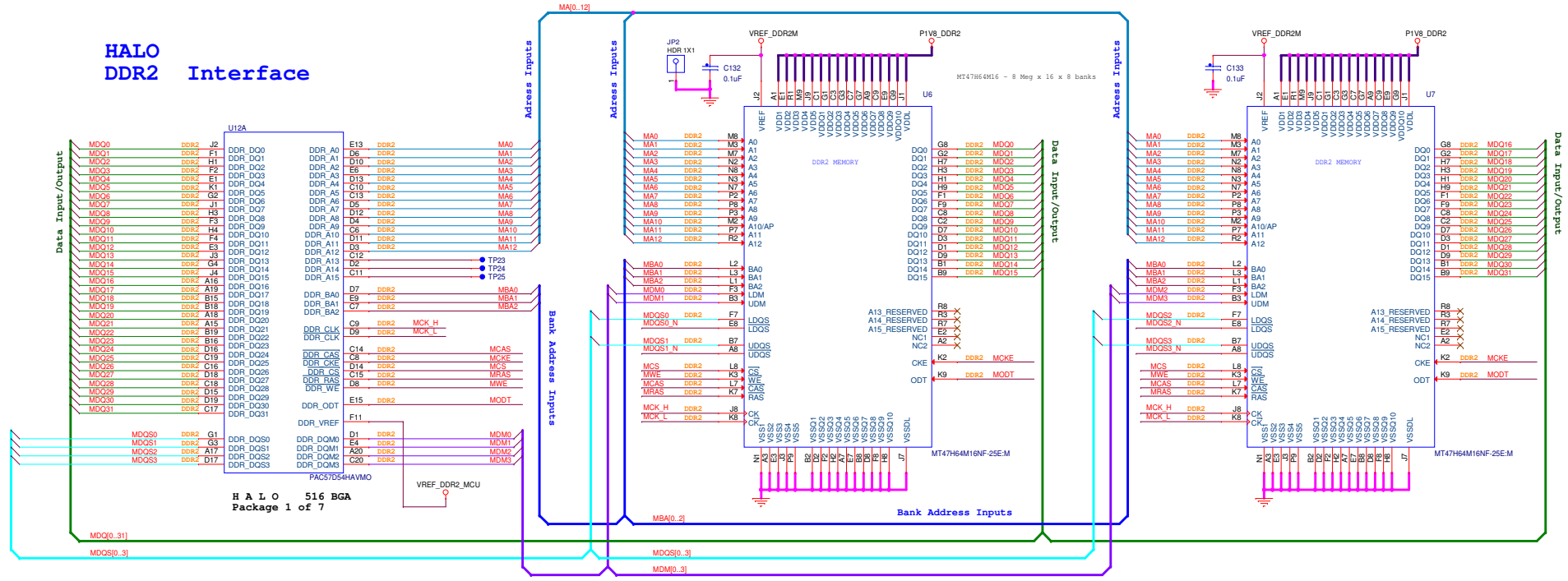
ICAP Classification: FCP: ___ FIUO: X PUBI: ___		
Drawing Title: MAC57D5-516DC		
Page Title: MCU CLK		
Size A	Document Number SCH-28806 PDF: SPF-28806	Rev A
Date: Wednesday, June 17, 2015	Sheet 6 of 11	

Oscillators and External Clock

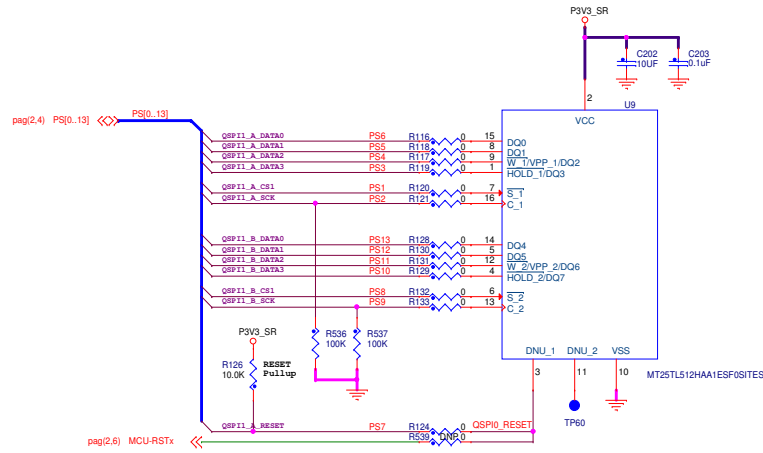


ICAP Classification: FCP: ___ FIUO: X PUBL: ___		
Drawing Title: MAC57D5-516DC		
Page Title: CLK		
Size A	Document Number SCH-28806 PDF: SPF-28806	Rev A
Date: Wednesday, June 17, 2015	Sheet 7 of 11	

HALO DDR2 Interface



512Mb, Twin-Quad I/O Serial Flash Memory



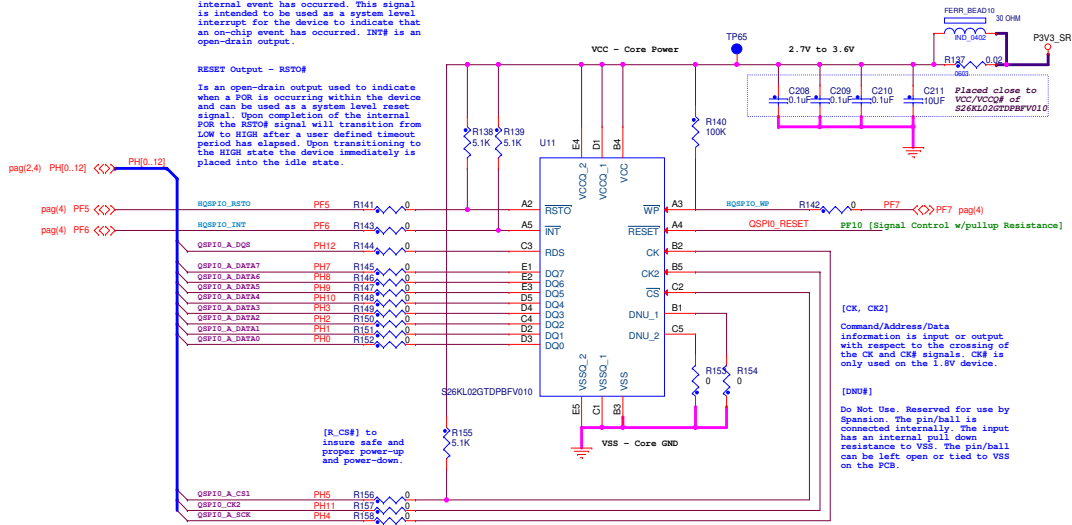
HyperFlash NOR Flash Memory

INT Output

When LOW the device is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output.

RESET Output - RST0#

Is an open-drain output used to indicate when a POR is occurring within the device and can be used as a system level reset signal. Upon completion of the internal POR the RST0# signal will transition from LOW to HIGH after a user defined timeout period has elapsed. Upon transitioning to the HIGH state the device immediately is placed into the idle state.



[CK, CK2]
Command/Address/Data information is input or output with respect to the crossing of the CK and CK# signals. CK# is only used on the 1.8V device.

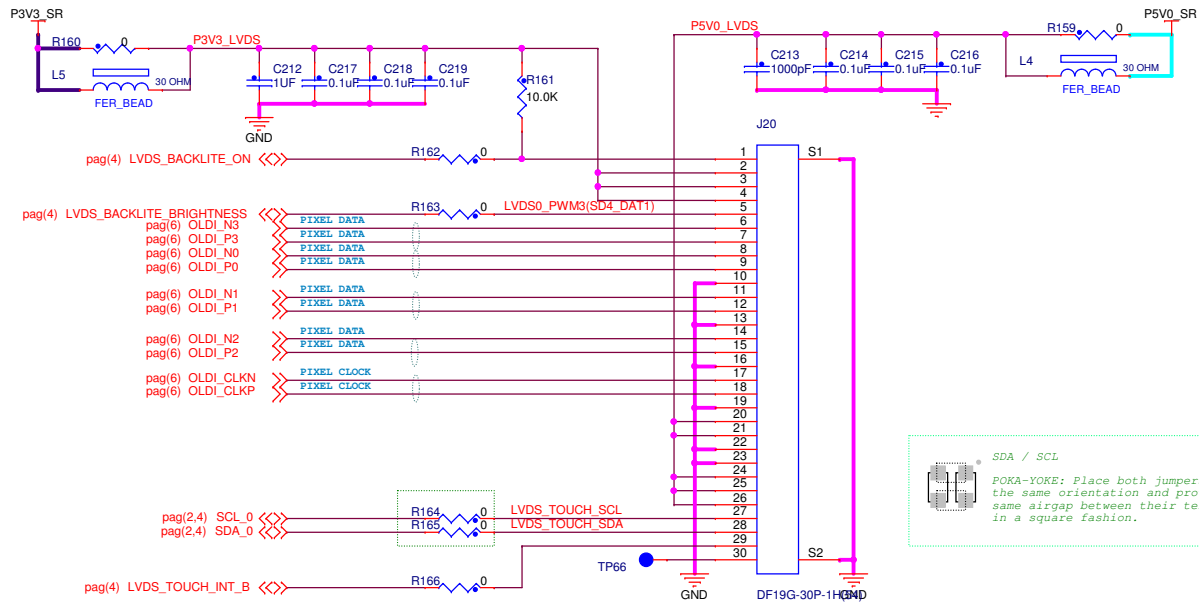
[DNU#]
Do Not Use. Reserved for use by Spansion. The pin/ball is connected internally. The input has an internal pull down resistance to VSS. The pin/ball can be left open or tied to VSS on the PCB.



ICAP Classification: FCP		FUNC: X		PUBI:	
Drawing Title: MAC57D5-516DC					
Page Title: QuadSPI Flash					
Size C	Document Number	SCH-28806 PDF: SPF-28806			Rev A
Date:	Friday, July 10, 2015	Sheet	10	of	11

LVDS LCD with Backlight & Capacitive Touch

Compatible Display: Freescale part number MCIMX-LVDS1



SDA / SCL
 POKA-YOKE: Place both jumpers with the same orientation and provide same airgap between their terminals in a square fashion.

freescale™

ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **MAC57D5-516DC**

Page Title: **LVDS**

Size B | Document Number SCH-28806 PDF: SPF-28806 | Rev A

Date: Wednesday, June 17, 2015 | Sheet 11 of 11