MAC57D5MB Customer Evaluation Board

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Revision Information

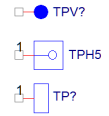
Rev	Date	Designer	Comments
X1	11 Mar 2014	Jesus Sanchez	Start of capture, Working version
			1st release for internal review (Complete Board)
			Version sent to Pre Layout, incorporating fixes from review
			Post Layout (Back Annotated). Matches PCB RevA

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hile Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop



Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2. 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

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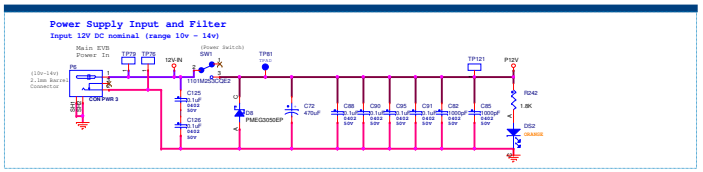
Microcontroller Solutions Group

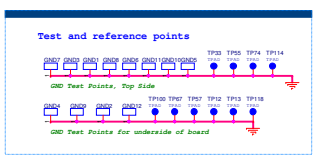
6501 William Cannon Drive West
Austin, TX 78735-8598

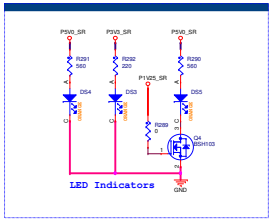
ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Designer: Jesus Sanchez - B42964	Drawing Title: MAC57D5MB		
Drawn by: Jesus Sanchez - B42964	Page Title: TITLE and NOTES		
Approved: Jesus Sanchez - B42964	Size B	Document Number SCH-28792 PDF: SPF-28792	Rev B
	Date: Tuesday, May 19, 2015	Sheet 1 of 12	

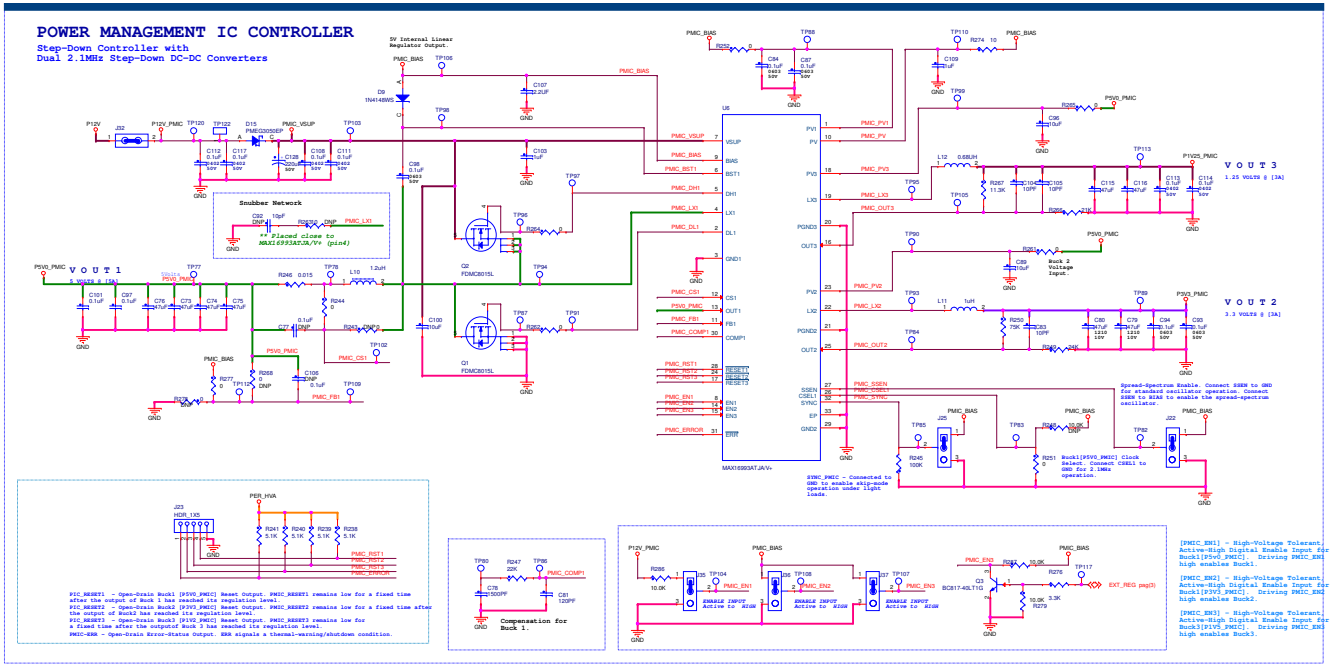
Power Input and Linear Voltage Regulators

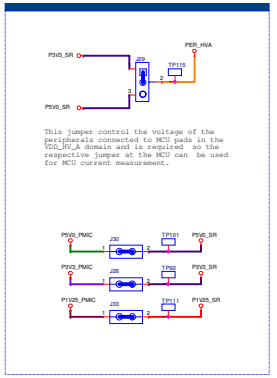






Switching Voltage Regulators and Supply Jumpers





[PMIC_EN1] - High-Voltage Tolerant, Active-High Digital Enable Input for Buck1[P5v0_PMIC]. Driving PMIC_EN1 high enables Buck1.

[PMIC_EN2] - High-Voltage Tolerant, Active-High Digital Enable Input for Buck2[P3V3_PMIC]. Driving PMIC_EN2 high enables Buck2.

[PMIC_EN3] - High-Voltage Tolerant, Active-High Digital Enable Input for Buck3[P1V25_PMIC]. Driving PMIC_EN3 high enables Buck3.

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ICAP Classification:	FCP:	FNO: X	PUB:
Drawing Title:	MAC57D5MB		
Page Title:	SW Pwr Supplies and Grat Pwr Jumpers		
Size: D	Document Number: SCH-28792 PDF: SPF-28792		Rev: B
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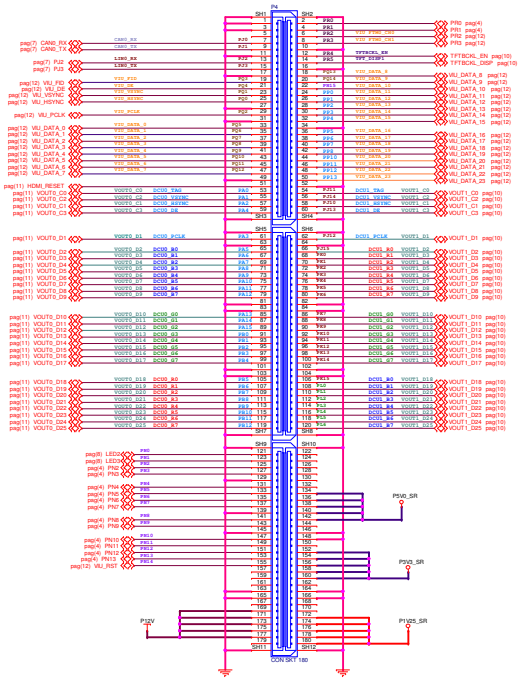

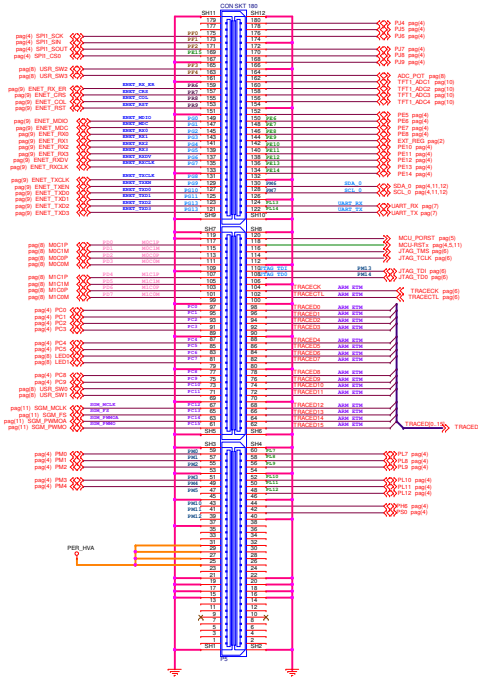

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ICAP Classification:	FCP:	FNDI: X	PURI:
Drawing Title:	MAC57D5MB		
Page Title:	DC Connectors		
Size: D	Document Number: SCH-28792 PDF: SPF-28792		Rev: B
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GPIO Pin Matrix

All pads are DNP (Do Not Populate) 0.1" pitch headers placed GPIO Pin Matrix on a 0.1" grid

PORT A

No spare pins on PortA

PORT B

No spare pins on PortB

PORT C

PORT D

No spare pins on PortD

PORT E

PORT F

No spare pins on PortD

PORT G

No spare pins on PortG

PORT H

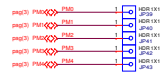
PORT J

PORT K

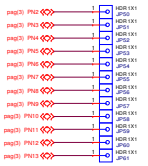
No spare pins on PortK

PORT L

PORT M



PORT N



PORT E

No spare pins on PortG

PORT Q

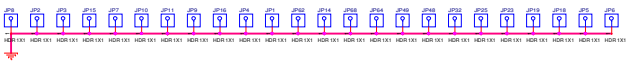
No spare pins on PortG

PORT R

PORT S

Layout Notes:
- Pads must be placed in a 13 x 16 matrix pattern, 2.54 mm pitch
- 13 wide (one column for each port EXCLUDING those with no available pads ie C, E, H, Q)
- 16 tall (1 row for each port number from 0 to 15).
- GND pad at bottom of each colum
- After production, pads should be through hole (not solder filled)

Busses are not used on ports as it makes it harder to see which pins are shared with other functions



GND Pads (one at bottom of each colum)

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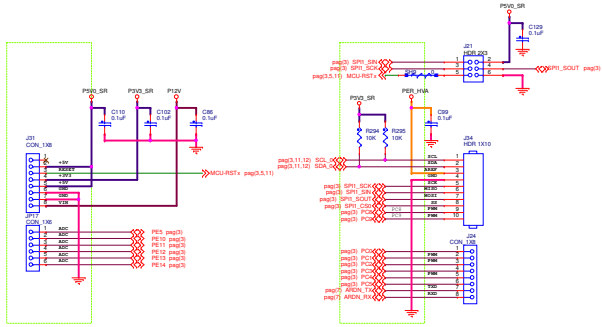

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Drawing Title:	MAC57D5MB		
Page Title:	GPIO Pin Matrix		
Size: D	Document Number: SCH-28792 PDF: SPF-28792		Rev: B
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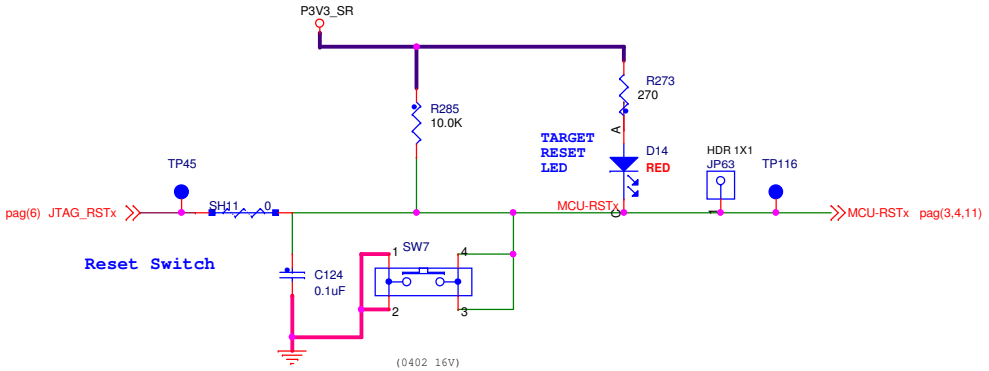
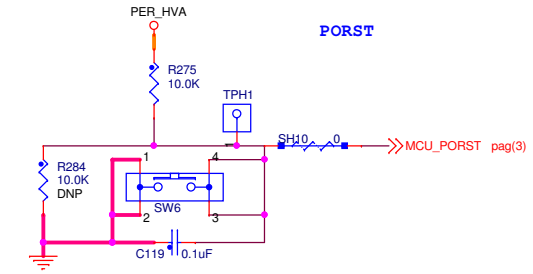
Reset and Clocks





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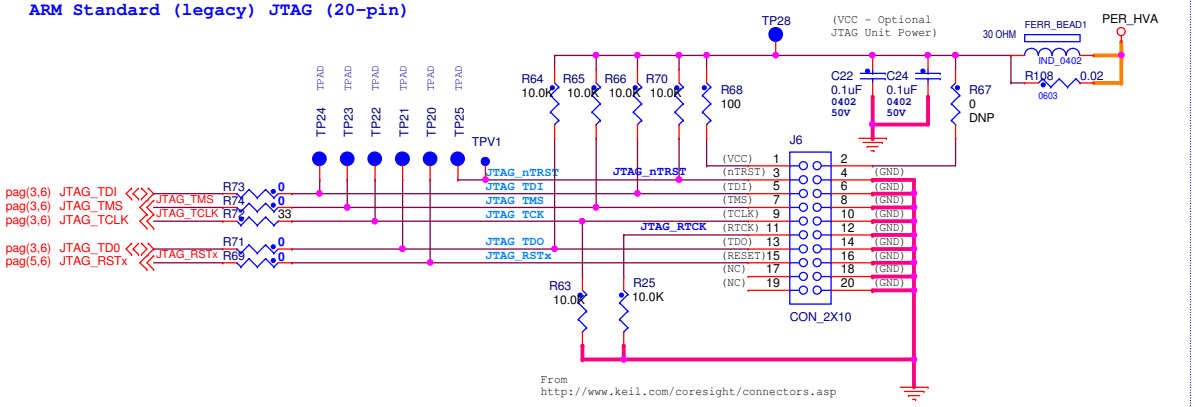
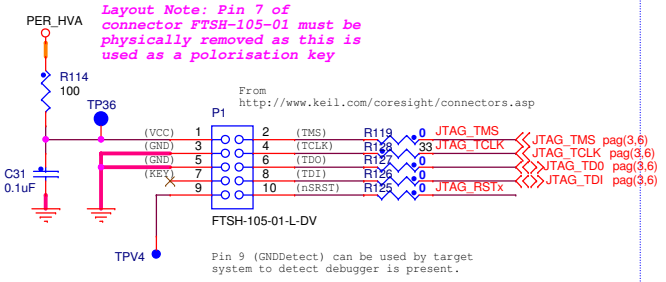
Debug Connectors (JTAG, Cortex and ETM)

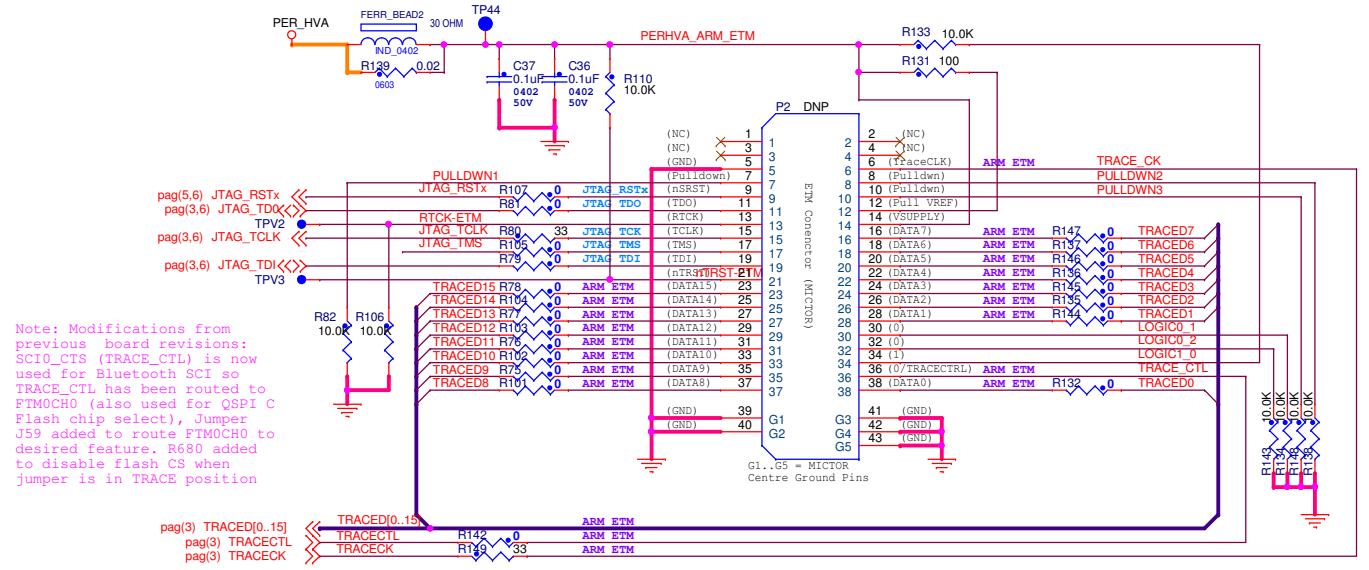
ARM Standard (legacy) JTAG (20-pin)



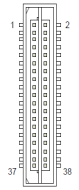
ARM Cortex (10-pin)



ARM ETM - Mictor 38 Pin



1	NC	NC	2
3	NC	NC	4
5	GND	TRACECLK	6
7	Pulldown	Pulldown	8
9	NC/ nSRST	Pulldown	10
11	TDO/SWV	Pullup (Vref)	12
13	RTCK	VSupply	14
15	TCK/SWCLK	0 / TRACEDATA[7]	16
17	TMS/SWIO	0 / TRACEDATA[6]	18
19	TDI	0 / TRACEDATA[5]	20
21	nTRST	0 / TRACEDATA[4]	22
23	0 / TRACEDATA[15]	TRACEDATA[3]	24
25	0 / TRACEDATA[14]	TRACEDATA[2]	26
27	0 / TRACEDATA[13]	TRACEDATA[1]	28
29	0 / TRACEDATA[12]	0	30
31	0 / TRACEDATA[11]	0	32
33	0 / TRACEDATA[10]	1	34
35	0 / TRACEDATA[9]	0 / TRACECTRL	36
37	0 / TRACEDATA[8]	TRACEDATA[0]	38



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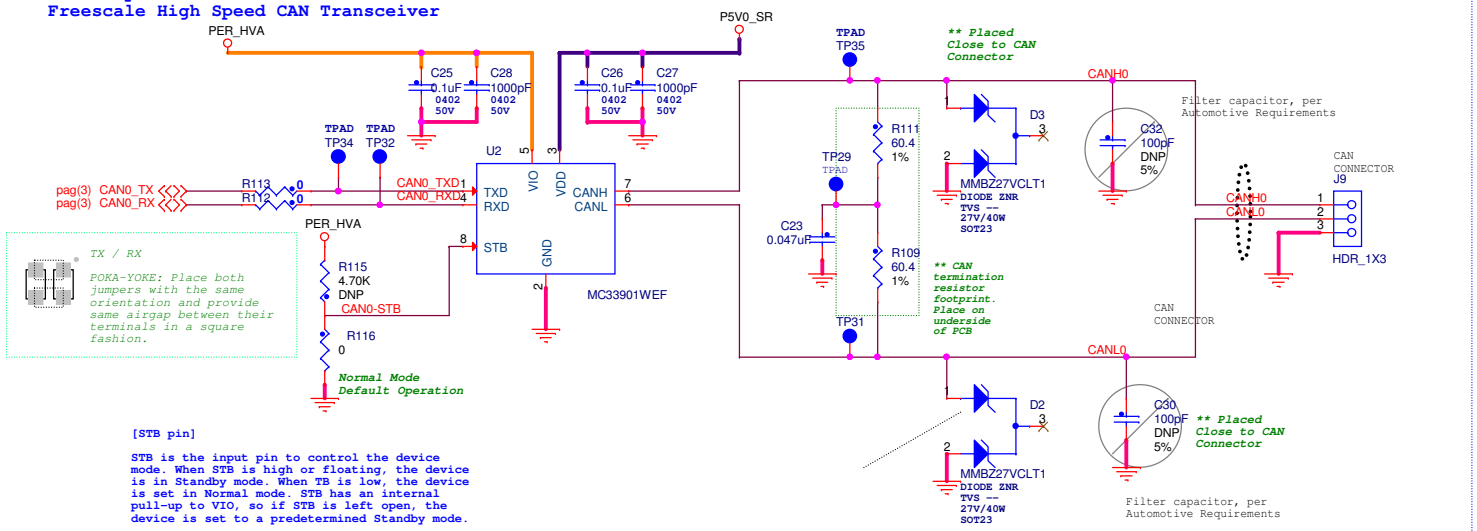
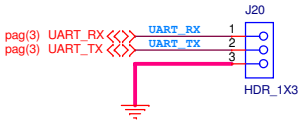
CAN0 Physical Interface
Freescale High Speed CAN Transceiver

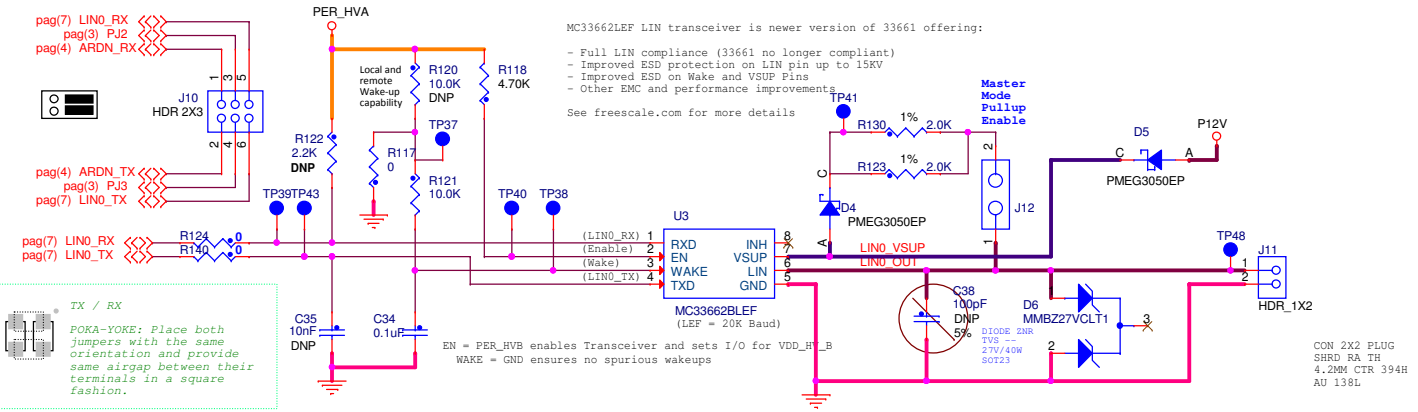


[STB pin]

STB is the input pin to control the device mode. When STB is high or floating, the device is in Standby mode. When TB is low, the device is set in Normal mode. STB has an internal pull-up to VIO, so if STB is left open, the device is set to a predetermined Standby mode.



LIN0 Physical Interface



MC33662LEF LIN transceiver is newer version of 33661 offering:

- Full LIN compliance (33661 no longer compliant)
- Improved ESD protection on LIN pin up to 15KV
- Improved ESD on Wake and VSUP Pins
- Other EMC and performance improvements

See freescale.com for more details

EN = PER_HVB enables Transceiver and sets I/O for VDD_HV_B
WAKE = GND ensures no spurious wakeups

CON 2X2 PLUG SHRD RA TH 4.2MM CTR 394H AU 138L

All CAN and LIN signals are in power domain VDD_HV_A.

All interfaces will work at 3.3V or 5.0V (PER_HVA jumper)

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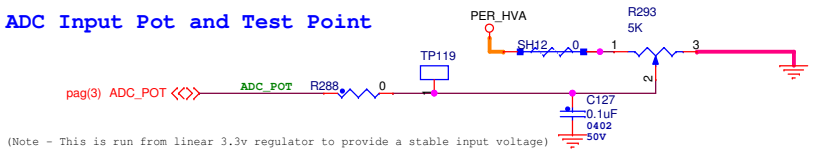
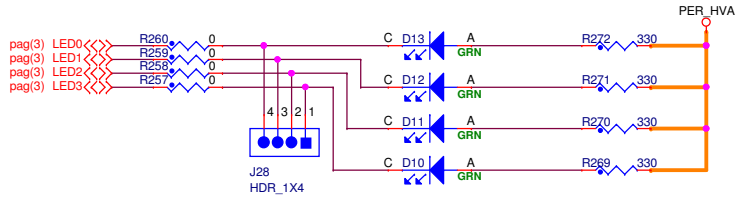
User Peripherals

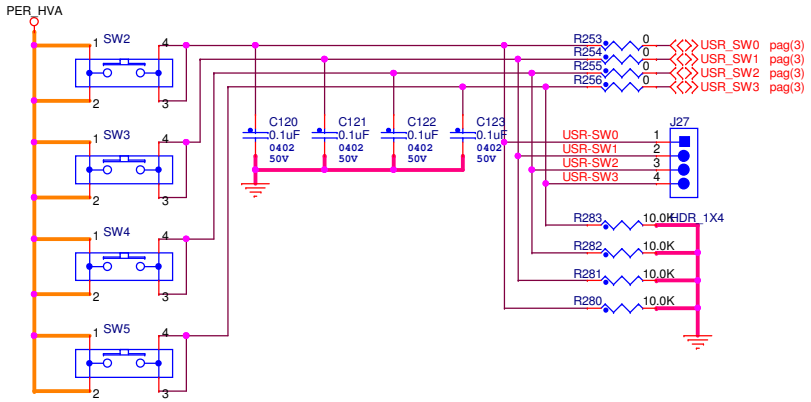
ADC Input Pot and Test Point

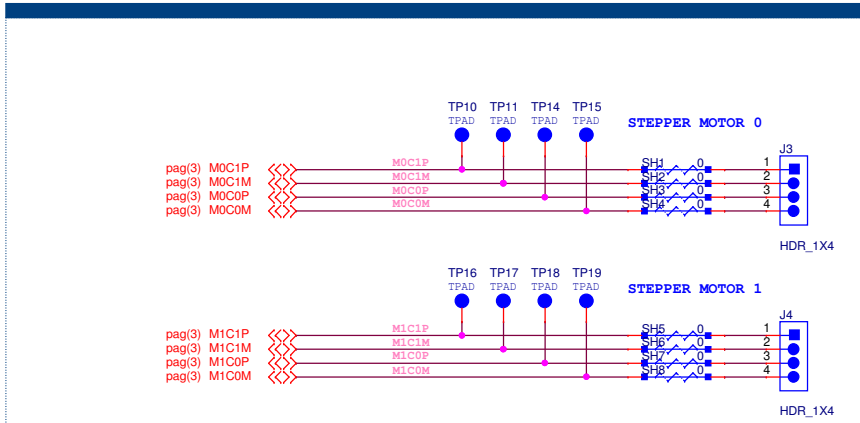


User LED's (Active Low)



User Switches (Active High)





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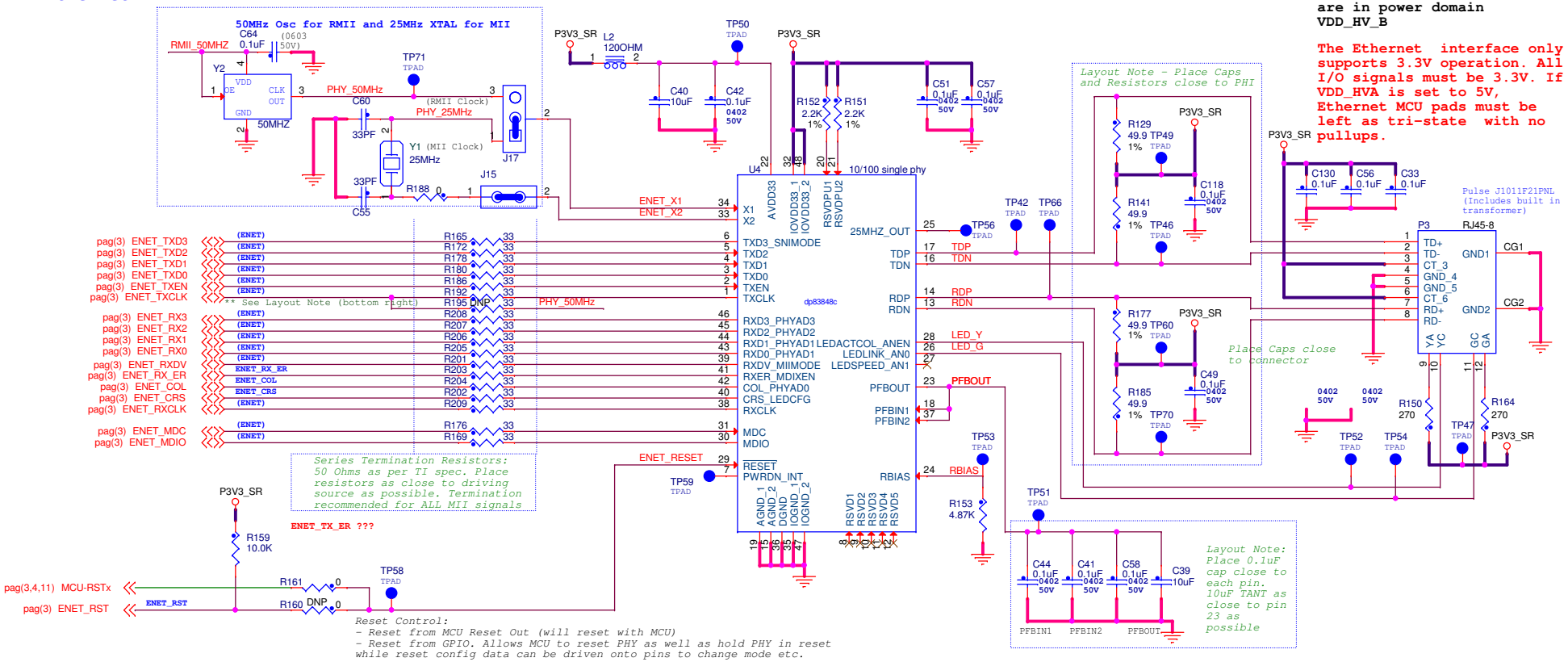
Ethernet

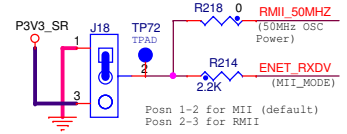


All Ethernet Signals are in power domain VDD_HV_B

The Ethernet interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, Ethernet MCU pads must be left as tri-state with no pullups.

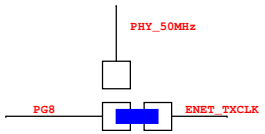
Boot Configuration (using PHY internal Pulls)

- Auto Negotiation Enable (All speeds / duplex supported)
  (AN_EN, AN0 and AN1 all Internal PullUP)
- Operating Mode (MII or RMII)
  (SNI_Mode Internal PullDown, MII_Mode control via jumper)
- LED Configuraiton (Mode1)
  (LED_CFG Internal PullUp)
- MDIX Enable (Auto MDIX Enabled)
  (MDIX_EN Internal PullUP)
- Physical Address (set to 0b00001)
  (PHYAD[0] Internal PullUp, PHYAD[1..4] Internal PullDown)



** Layout Note - Place resistors as shown with shared pad on PG8 side of resistors

For RMII mode, remove resistor between PG1 and TXCLK and place between PG8 and PHY_50MHz



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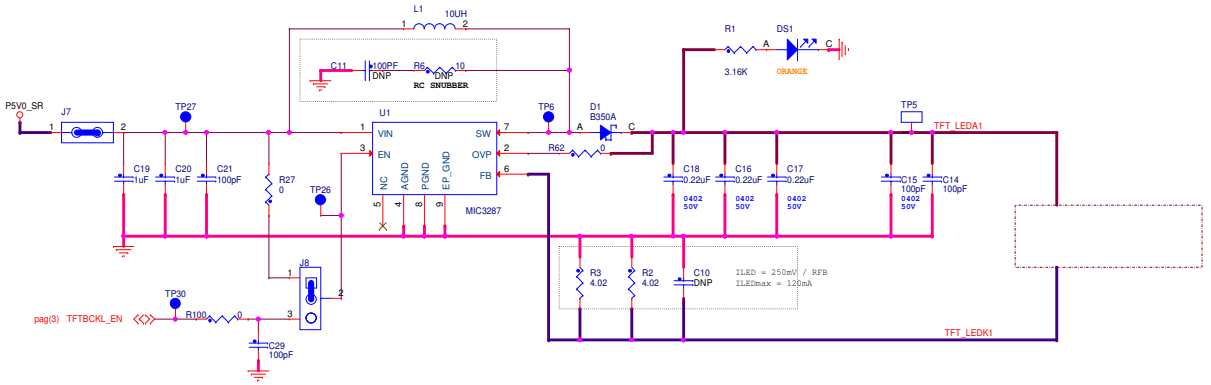
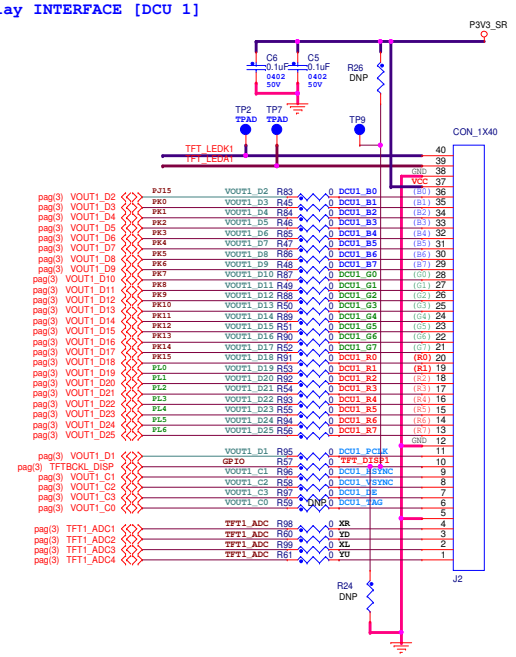
Switching Power Supply
TFT Display



TFT Display INTERFACE [DCU 1]



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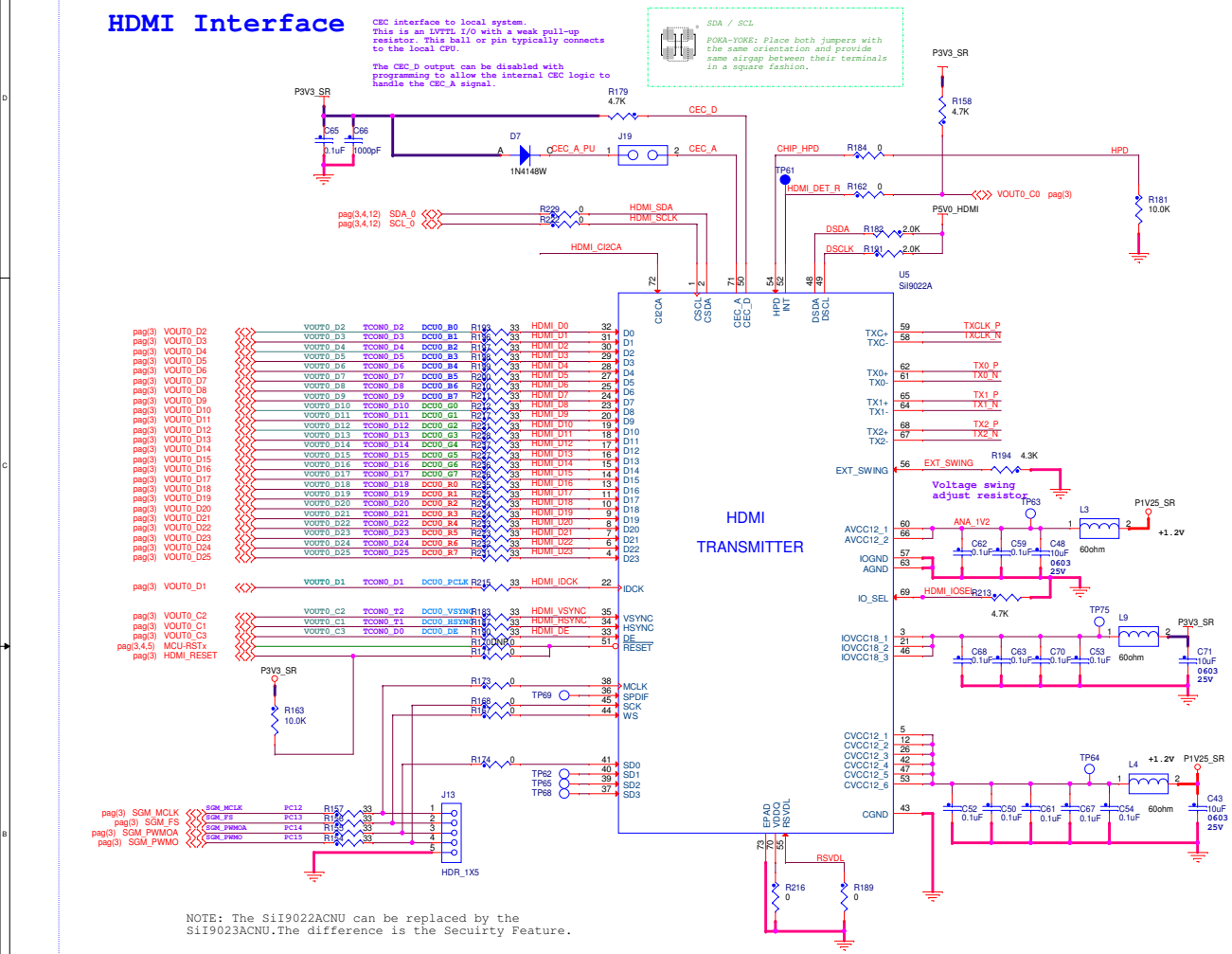
HDMI Interface

CEC interface to local system.
This is an LVTTL I/O with a weak pull-up resistor. This ball or pin typically connects to the local CPU.

The CEC_D output can be disabled with programming to allow the internal CEC logic to handle the CEC_A signal.

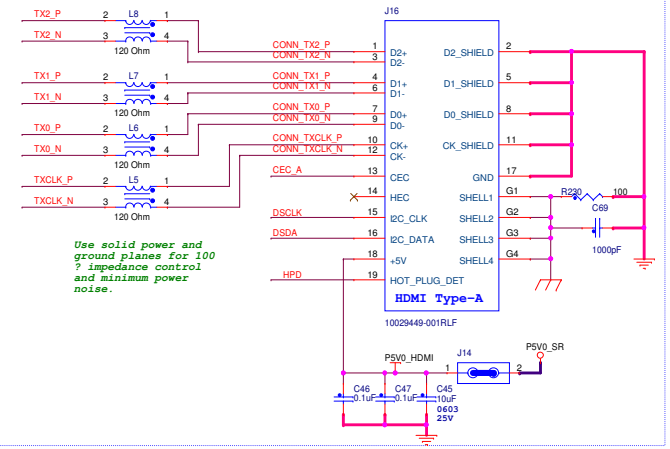
SDA / SCL

POKA-YOKE: Place both jumpers with the same orientation and provide same airgap between their terminals in a square fashion.



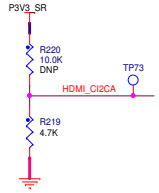
NOTE: The SiI9022ACNU can be replaced by the SiI9023ACNU.The difference is the Secuirty Feature.

HDMI Connector



Use solid power and ground planes for 100 ? impedance control and minimum power noise.

Stuff only of two 4.7kOhms resistors to set chip I2C adress (Required for 81-ball VFGA and 72-pinQFN)



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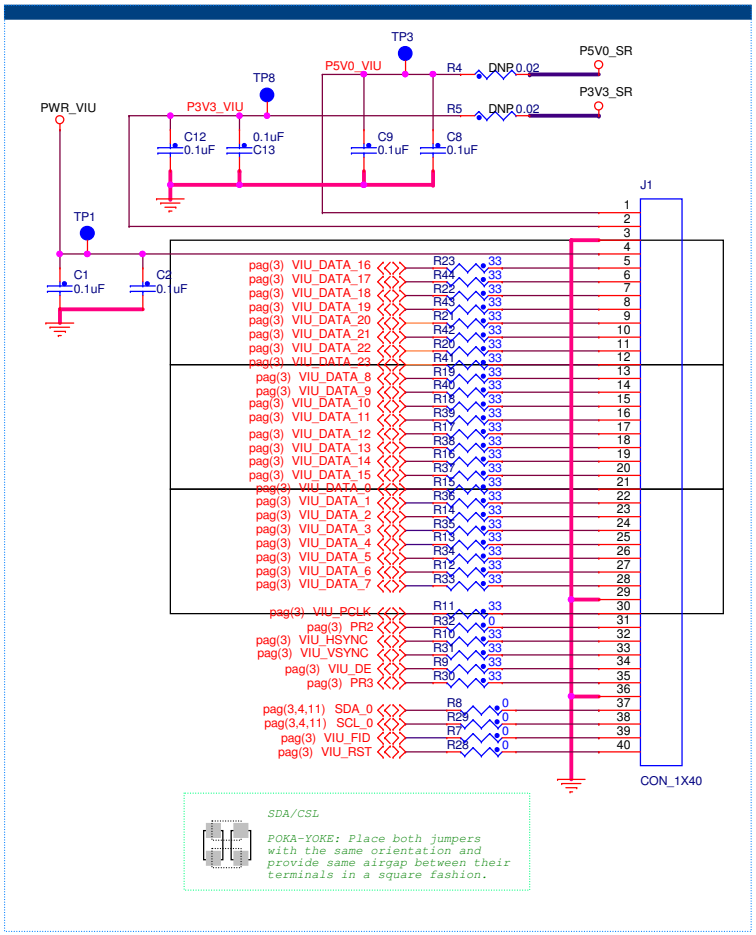
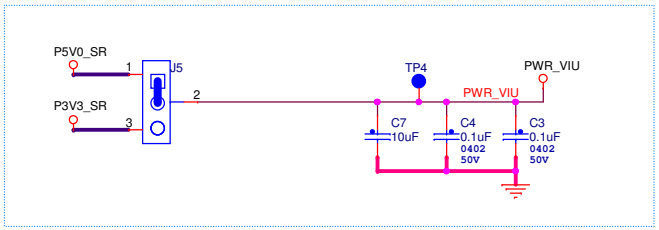
VIU Interface





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