MPC5748G Low Cost Evaluation Board (MPC5748G-LCEVB)

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Revision Information

<table>
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<th>Date</th>
<th>Designer</th>
<th>Comments</th>
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<td>14 Apr 2015</td>
<td>Alasdair Robertson</td>
<td>Start of capture, Working version (256BGA)</td>
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<td>x2</td>
<td>08 May 2015</td>
<td>Alasdair Robertson</td>
<td>Changed to 176 QFP Package and changed peripheral Matrix</td>
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<td>Changes required for initial placement</td>
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<td>19 May 2015</td>
<td>Alasdair Robertson</td>
<td>Tidy Up, Replaced some &quot;hard to source&quot; components</td>
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<td>26 May 2015</td>
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<td>Renumber and Back Annotated from Layout</td>
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<td>27 May 2015</td>
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<td>Correction to GND on 3v3 Regulator circuit</td>
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<td>29 May 2015</td>
<td>Alasdair Robertson</td>
<td>Correction to CAN Test points</td>
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<td>DNP Jumpers. 0 Ohm resistors added across LIN jumpers</td>
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<td>11 Jun 2015</td>
<td>Andrew MacDonald</td>
<td>Prototype Manufacture Release</td>
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<td>AX1</td>
<td>29 Sep 2015</td>
<td>Alasdair Robertson</td>
<td>Prod Build changes (LIN0 default to Slave, LIN1 Master only)</td>
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<td>AX2</td>
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<td>Change to JTAG Pulls to meet latest RM Spec</td>
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<td>AX3</td>
<td>29 Oct 2015</td>
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<td>Pull DOWN on TCLK to mitigate against STANDBY exit issue.</td>
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<td>Alasdair Robertson</td>
<td>Updated NXP Logos</td>
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<td>B1</td>
<td>26 Aug 2016</td>
<td>Karthikeyan</td>
<td>The text mentioned as &quot;Calypso&quot; in all places updated to &quot;MPC5748&quot;. Title block document number changed.</td>
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Caution:

These schematics are provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP MPC5748G family of Microcontrollers. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and NXP does not assume any liability for such a hardware design.

Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
  - Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via buses as this makes it harder to determine where each signal goes.

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

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Specific PCB LAYOUT notes are detailed in ITALICS
Main Power In (SR = Switching Reg)

Power Supply Input

3.3v Switching Regulator

Power Control

Jumper's can be fitted to facilitate power measurements

Input Voltage 5V, Output 3.3V at 700mA. Ripple 1.4mV, Approx 90% efficient
MPC5748G MCU Power Connections

Power Supply Constraints:
- If VDD_HV_A is driven from 3.3V, VDD_HV_FLA must also be supplied from 3.3V.
- If VDD_HV_A is driven from 5V, the VDD_HV_FLA pin must be disconnected from 3.3V.
- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain.

Default Configuration:
- All MCU supply voltages are set to 3.3V (ADC0, ADC1, VDD_HV_A, VDD_HV_B, VDD_HV_C, VBallast).
- VDD_HV_FLA = External 3.3V supplied (jumper fitted)

The analogue pins can only be driven to the same voltage as the VDD_HV_A domain they are situated in (i.e. max 3.3V) so makes sense for the analogue supply and reference to be 3.3V.

Notes on signal grounds:
- The scheme shown has the analogue and digital grounds connected to the same plane.
- This results in better ADC performance than using an analogue ground plane with single entry point (or ferrite) to digital ground plane.
MPC5748G MCU Decoupling and bulk storage

Capacitor Types:
- 4700pF - Ceramic X7R, 50V 10% 0402 (Kemet C0402C104K49AC)
- 0.1μF - Ceramic X7R, 16V 10% 0402 (Murata GCM219R71CS84K37)
- 0.68μF - Ceramic X7R, 16V 10% 0805 (Murata GCM219R71CS84K37)
- 1μF - Ceramic X7R, 10V 10% 0603 Low ESR (Taiyo Yuden LMR107B7105KA-T)
- 2.2μF - Ceramic X7R, 10V 10% 0603 Low ESR (Taiyo Yuden LMR107B7225KA-T)

Place small Caps as close as possible to MCU pins.

One 0.1μF cap per VDD_NV_x pin. Place as close as possible to pin.

VDD_LV (1.25V) Decoupling. Place one of the 0.1μF caps close to each VDD_LV pin. Place the 0.68μF caps on each side of the package such that there is no cap on the side with the ballast transistor.

(For regulator stability the total capacitance should be around 2.2μF).

Place close to transistor.

Ballast Transistor

LP Internal Reg Cap
Reset and External Clock In

Reset is in the VDD_HVA domain.

Table 3-3: Functional terminal state during power-up and reset

<table>
<thead>
<tr>
<th>TERMINAL TYPE</th>
<th>POWERUP pull state</th>
<th>RESET pull state</th>
<th>DEFAULT pull state</th>
<th>Comments</th>
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<tr>
<td>RST-OUTx</td>
<td>Strong pull-down</td>
<td>Weak pull-up</td>
<td>No pull</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>High impedance</td>
<td>High impedance</td>
<td>High impedance</td>
<td></td>
</tr>
<tr>
<td>PER_HVA</td>
<td>POWER/OUT pin only</td>
<td>Weak pull-up</td>
<td>No pull</td>
<td></td>
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<tr>
<td>GND</td>
<td>High impedance</td>
<td>High impedance</td>
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<tr>
<td>ANA10G</td>
<td>High impedance</td>
<td>High impedance</td>
<td>High impedance</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>High impedance</td>
<td>High impedance</td>
<td>High impedance</td>
<td></td>
</tr>
<tr>
<td>JTAG-RSTx</td>
<td>Weak pull-down</td>
<td>Weak pull-up</td>
<td>No pull</td>
<td>Active reset drive (high / low) for any peripherals that need to be reset when MCU is in Reset</td>
</tr>
<tr>
<td>MCU-RSTx</td>
<td>Weak pull-down</td>
<td>Weak pull-up</td>
<td>No pull</td>
<td></td>
</tr>
<tr>
<td>GND</td>
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<td>High impedance</td>
<td>High impedance</td>
<td></td>
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</table>

Note: The Reset pad on MPC5748G is in the VDD_HVA domain which can be run from either 3.3V or 5V (selected by the VDD_HVA and PER_HVA jumpers). To maintain brightness of the LED's irrespective of the voltage setting, the LED's are powered from constant 3.3V, grounded via the reset line.
Clocks

Oscillators

- PB8 (EXTAL32)
- PB9 (XTAL32)
- C17 12PF
- C18 12PF
- C19 12PF
- C20 12PF
- T3 32.768kHz
- Y2 40.0MHz
- Y3 32.768kHz
- R41 1.0M DNP
- R42 1.0M DNP

PC-255 32.768kHz-A3
(Lead Capacitance 1pF)

FC-255 32.768kHz-A3
(Lead Capacitance 7pF)

MCU-XTAL
- PB8
- PB9

MCU-EXTAL
- PB8
- PB9

NXP General Business Use
CAN & LIN Physical

CAN0 Physical Interface
- VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)
- VI/O - determines the signal level on MCU TX and RX pins and can range from 2.4 to 5.5V
- STB - High for Standby mode, pulled low for normal mode.

CAN1 Physical Interface
- VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)
- VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V
- STB - High for Standby mode, pulled low for normal mode.

LIN0 Physical Interface
- Configured as SLAVE by default (LIN0 supports Master and Slave)
- Total current through resistors (LIN Bus at GND) = 12mA (0.144W)
- Each resistor spec = 0.1W (0.2W total)

LIN1 Physical Interface
- Configured as MASTER by default (LIN only supports Master mode)
- Total current through resistors (LIN Bus at GND) = 12mA (0.144W)
- Each resistor spec = 0.1W (0.2W total)

All CAN and LIN signals are in power domain VDD_HV_A.
All interfaces will work at 3.3V or 5.0V (PER_HVA)

MC33662BLEF LIN transceiver is newer version of 33661 offering:
- Full LIN compliance (33661 no longer compliant)
- Improved ESD protection on LIN pin up to 15KV
- Improved ESD protection on Wake and VSUP Pins
- Other EMC and performance improvements
See freescale.com for more details
USB RS232 (serial) Interface

FTDI USB <-> Serial Interface
- Self Powered mode. No power is taken from USB
- Device defaults to Dual serial (RS232) mode ie RS232 on both A and B
- Configurable I/O voltage on CHA / CHB via VDDIOA / B

Send Immediate / Wakeup Disabled for CHA
Send Immediate / Wakeup Disabled for CHB
Disable Receiver when in USB suspend mode

All Signals are in power domain VDD_HV_A.

FTDI Pin 40 (TXD) is Output from FTDI Device, connect to MCU RXD
FTDI Pin 39 (RXD) is Input to FTDI device, connect to MCU TXD

Drawing Title: MPC5748G-LCEVB
Page Title: US2 RS232 Interface
USB (Type A Host and Type AB OTG)

USB Signals are in power domain.

VDD_RV_A

The USB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_RVA is set to 5V, USB MCU pads must be left as tri-state with no pullups.

General Layout Note. Recommendation is to keep all tracks between MCU and USB PHI less than 3". See additional SMSC Layout guidelines PDF to the right.

USB Host, Type A
(Available on all packages)

USB POWER SWITCH

USB Type A / Type AB

MPC5748G-LCEVB

Drawing Title: SCH-28822
Document Number: PDF: SPF-28822
Rev: B1

Date: Friday, August 26, 2016
Sheet: 11 of 15
Ethernet (Configured for MII Mode)

All Ethernet signals are in power domain VDD_HVA

The Ethernet interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, Ethernet MCU pads must be left as tri-state with no pullups.

Layout Note - Place Caps and Resistors close to PHI

Place Caps close to connector

Place 0.1uF cap close to each pin. 10uF TANT as close to pin 23 as possible as shown in diagram below taken from TI device specificaiton
Note on VBAT:
- Operational range is 4.5v to 6v
- Undervoltage definition is 4.1v

On any this is supplied from 5v, in theory this should be ok battery with slow delay between applying Vbat and 1V. If necessary, 1V can be externally supplied by removing the resistor and connecting pad to 12v

**FlexRAY Physical Interface**

All Signals are in power domain VDD_HV_A.

FlexRAY interface will work at 3.3V or 5.0V (PER_HVA)

Decoupling Caps for BOTH IC's. Place next to power pins.

PER_HVA

FRBATA, SV_S, PER_HVA

Decoupling Caps for BOTH IC's. Place next to power pins.

PER_HVA

FRBATA, SV_S, PER_HVA

**FlexRAY A**

**FlexRAY B**

Bus voltage +/- 12V (VBAT = 12v)

Components spec'd for 12V operation

Bus voltage +/- 12V (VBAT = 12v)

Components spec'd for 12V operation

**FlexRAY Debug Connector**

- FlexRAY debug connector

- FlexRAY debug connector

**Connections**

- FlexRAY debug connector

- FlexRAY debug connector

**Component List**

- C69 10UF
- C88 10UF
- C87 10UF
- C86 10UF

- C89 10UF
- C88 10UF
- C87 10UF
- C86 10UF

**Additional Information**

- Crimped lead - 279-9522 Receptacle housing - 279-9156
- Crimped lead - 279-9522 Receptacle housing - 279-9156
- Crimped lead - 279-9522 Receptacle housing - 279-9156
- Crimped lead - 279-9522 Receptacle housing - 279-9156

**Bus Voltage +/- 12V**

- Bus voltage +/- 12V (VBAT = 12v)

- Components spec'd for 12V operation

**Bus Voltage +/- 12V**

- Bus voltage +/- 12V (VBAT = 12v)

- Components spec'd for 12V operation

**Automotive Microcontroller Applications**

**East Kilbride, Scotland**

**NXP General Business Use**

**Drawing Title:** MPC5748G-LCEVB

**Page Title:** FlexRAY Physical Interface

**File Name:** SCH-28822

**PDF:** SPF-28822

**Date:** Friday, August 26, 2016

**Sheet:** 13 of 15
User Peripherals (Led's, Switches and ADC Pot)

Switches are hard wired to 3.3V rather than 5V so it's not possible to drive 5V into a 3.3V pad (which would cause damage).
Similarly, the LED's are active low with 3.3V supply so can be safely coupled to pads on either 3.3V or 5V domains. The ADC input is limited to 3.3V, again to prevent driving 5V into a 3.3V pad which would cause damage.

User LED's (Active Low)

LED's are SMD (1206) Yellow.

Note that LED2 and LED4 (PG3 and PG5) can be controlled in LFU_RUN mode (and also have pad keepers in LFU_STANDBY).

ADC Input Pot and Test Point

Hex Encoded Switch (Active High)

User Pushbutton Switches (Active High)

Note - PA1 is also the NMI pin!

Currently limit resistors to ensure injection spec of 5mA is not exceeded.
All pads are DNP (Do Not Populate) 0.1" pitch headers placed on a 0.1" grid.

GPIO Pin Matrix

Layout Notes:
- Pads must be placed in a 5 (W) x 16(H) matrix pattern, 2.54 mm pitch
- One column for each port
- 16 tall (1 row for each port number from 0 to 15).
- GND pad at bottom of each column
- After production, pads should be through hole (not solder filled)