



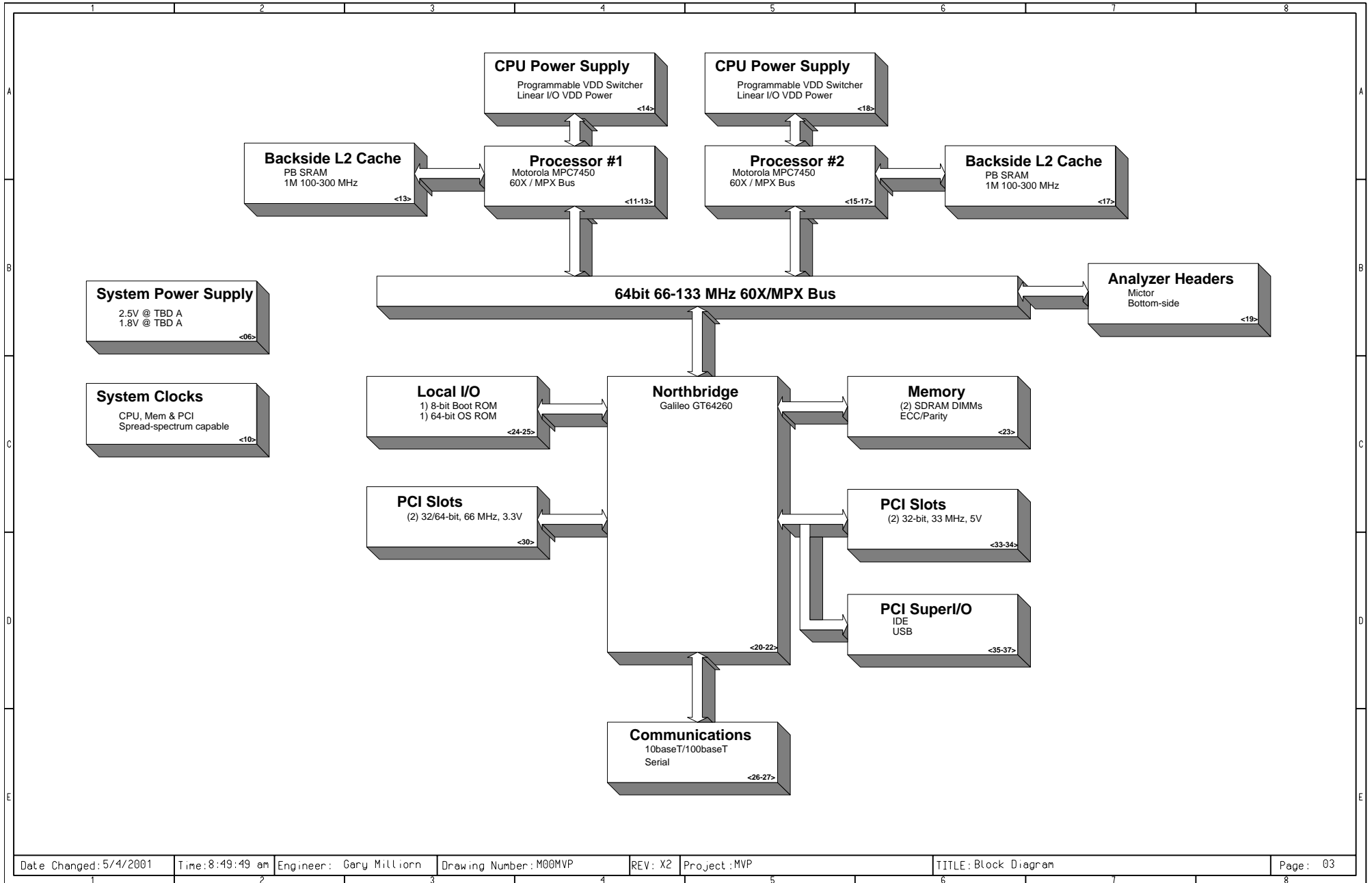
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No warranty, expressed or applied, is made as to the  
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this product.

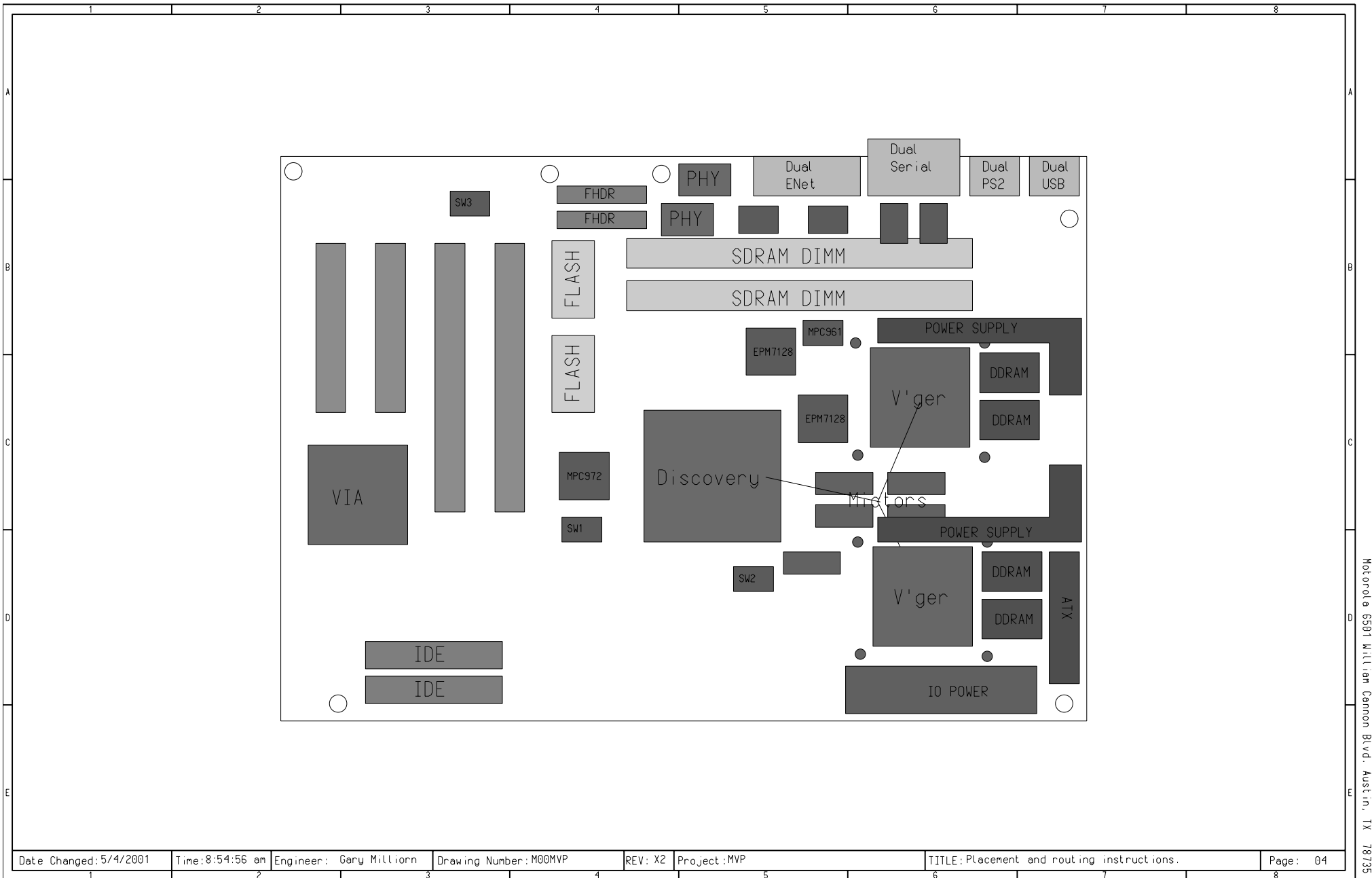
**\*Digital DNA**  
from Motorola

		1			2
<h1>Schematic Notes</h1>					
A	1.	<p>Unless otherwise specified:</p> <ul style="list-style-type: none"> <li>All resistors are SMD0603, in ohms, 0.08W, +/-5%</li> <li>All capacitors are SMD0603, in microfarads (<math>\mu</math>F), +/-20%.</li> <li>All inductances are in microhenries (<math>\mu</math>H).</li> <li>All ferrites are Z-50 ohms at 100 MHz.</li> <li>All fuses are self-resetting polyswitch (PTC) devices.</li> <li>Board impedance is 55 +/- 5 ohms.</li> </ul>			
	2.	<p>Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are:</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div>VCC_3.3</div> <div>VCC_2.5</div> <div>OVD</div> <div>GND</div> </div> <div style="display: flex; justify-content: space-around; align-items: center;"> <div></div> <div>pVCORE</div> <div>sVCORE</div> <div></div> </div>			
	3.	<p>Part numbers used are for reference only; compatible parts may be used, refer to the bill of materials.</p>			
	4.	<p>Motorola and the Motorola logo are registered trademarks of Motorola. PowerPC is a trademark of IBM. Other trademarks are the respective property of their respective copyright holders. Under the syncware terms, All rights reserved. No warranty is made, express or implied.</p>			
B	5.	<p>The sheet-to-sheet cross reference format is: Sheet -- VerZoneLetter HorizZoneNumber</p>			
	6.	<p>Components with the label "No Stuff" are not to be installed by default; they are for test or manufacturing purposes only.</p> <div style="text-align: center;"> <p>The symbol consists of a rectangular box with a diagonal line from the bottom-left to the top-right. To the left of the box is the label 'C123' and to the right is the label 'X1'.</p> </div>			
	7.	<p>All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (e.g. PCI). Little-endian numbering is noted at the source component.</p>			

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05	Main Power, Reset
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09	FPGA Logic: System Logic
10	Clocks
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12	CPU1: Cache Interface
13	CPU1: L2 Cache SRAM
14	CPU1: Power Supply
15	CPU2: MPC7450 System
16	CPU2: Cache Interface
17	CPU2: L2 Cache SRAM
18	CPU2: Power Supply
19	Logic Analyzer
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21	Bridge: Power Supply
22	Bridge: Memory Controller
23	SDRAM DIMMs #1 & #2
24	Bridge: Interface Controller
25	Boot and OS ROMs
26	Bridge: Ethernet Interface
27	Ethernet MACs and connectors
28	Serial Ports
29	Bridge: PCI Interface #0
30	PCI: 66 MHz Slots #1 & #2
31	--reserved--
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33	PCI: 33 MHz Slots #1 & #2
34	PCI: 33 MHz Slots #3
35	PCI I/O: USB, PS2
36	PCI I/O: IDE
37	IDE: Primary and Secondary Ports

REV	DATE	CHANGES
X1	00NOV17	Initial version
X2	01MAY05	Errata corrections (q.v.)





**1 ATX Chassis Power**  
Route VCC and VCC\_3.3  
on separate power planes.

**1 CHASSIS MOUNTING HOLES**  
ATX Chassis: 9 holes.

J19  
conn. battery

F4  
pol.c.smd100  
POLY SW

VBAT → 35-E1

VSTDBY → 35-A1.34-D5

**1 Local Reset Switch**

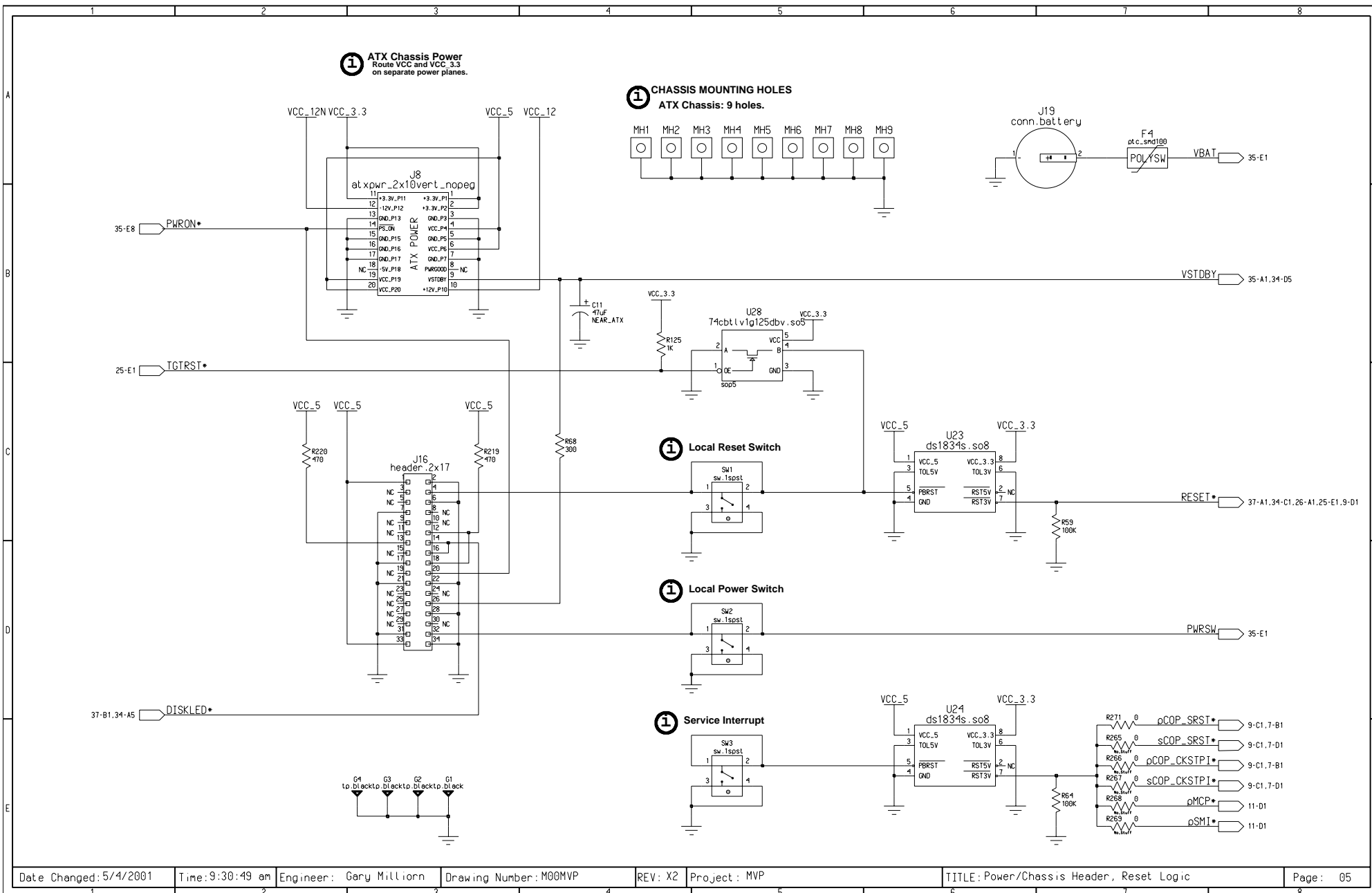
**1 Local Power Switch**

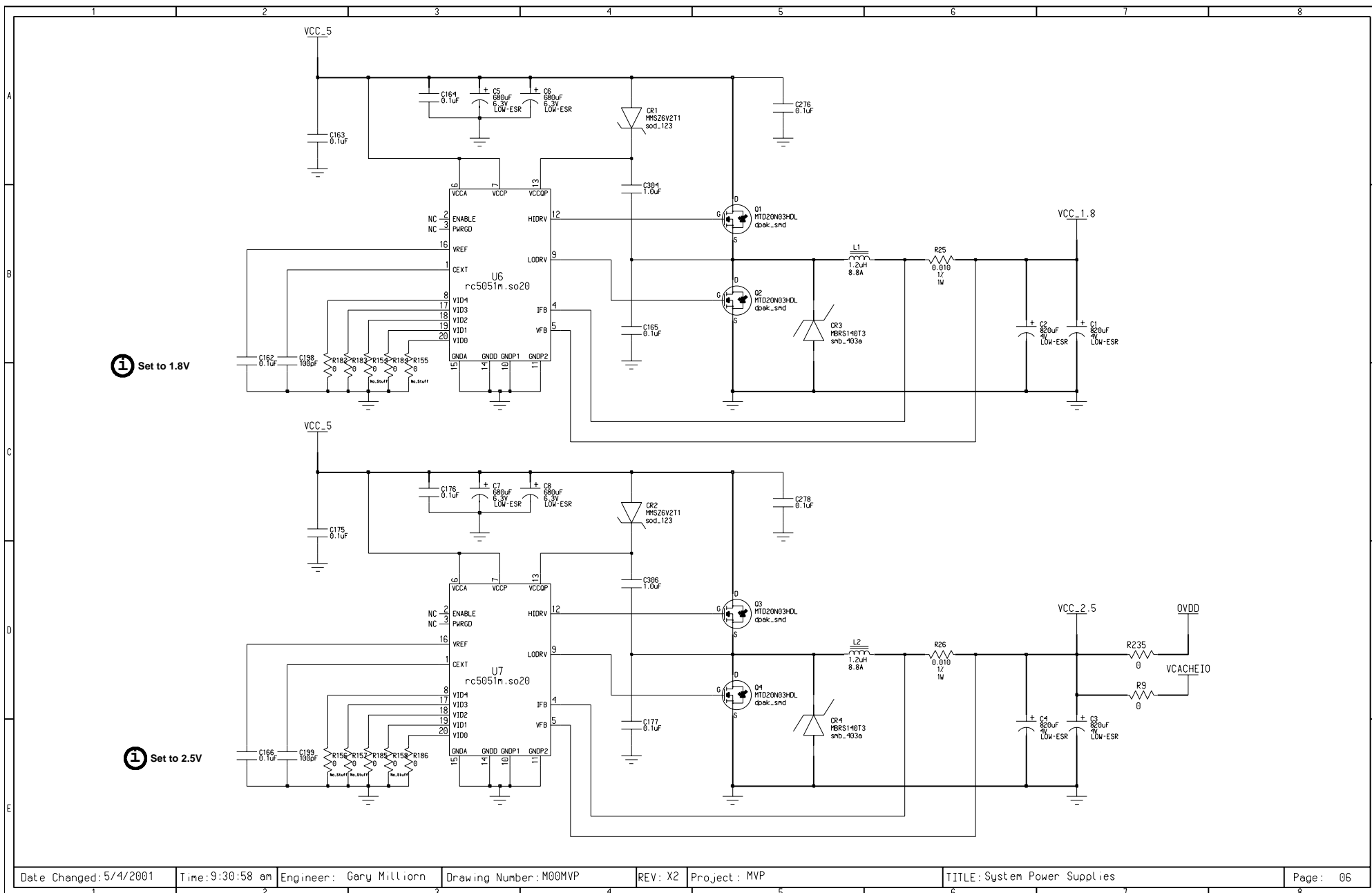
**1 Service Interrupt**

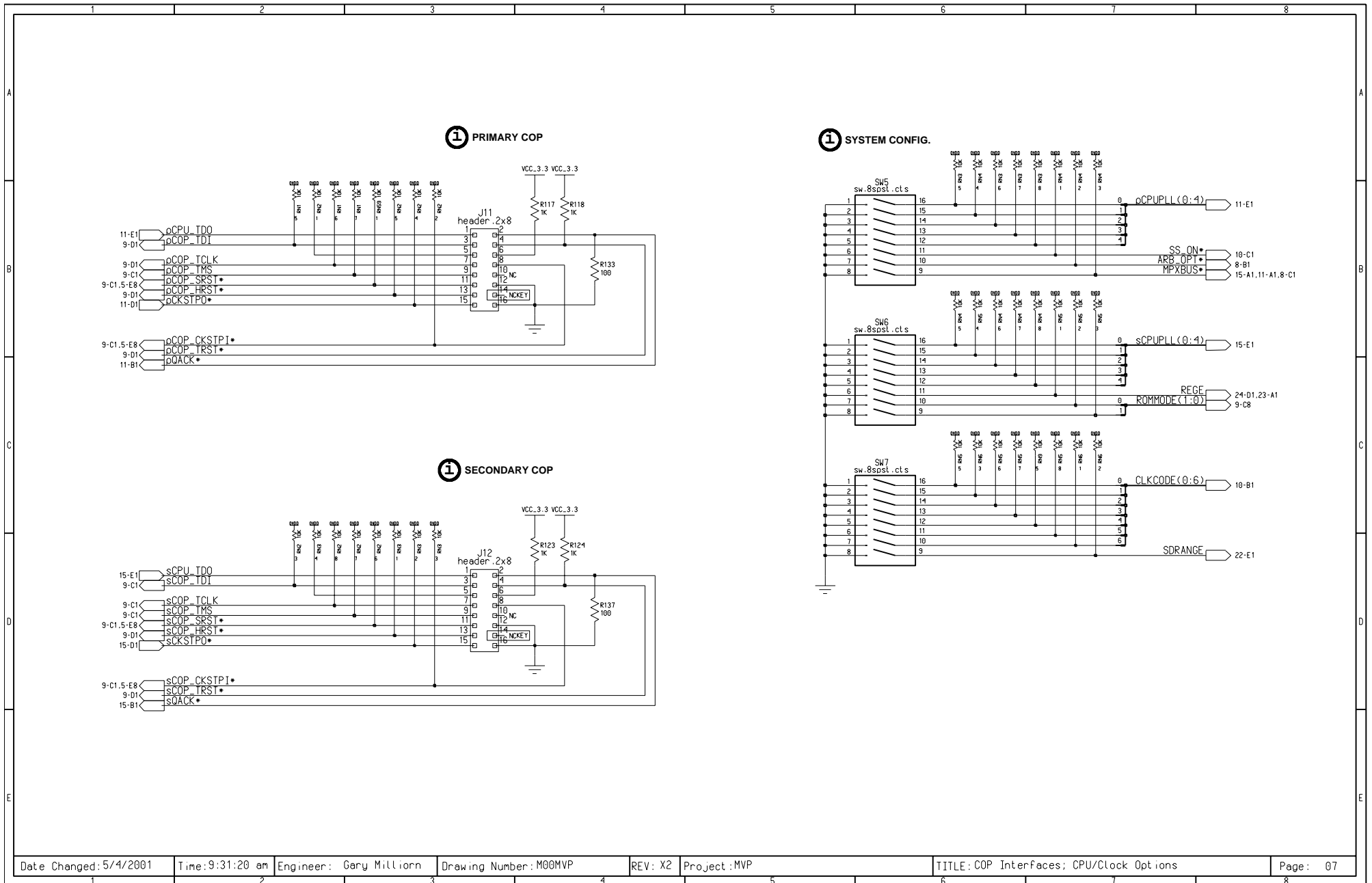
RESET → 37-A1.34-C1.26-A1.25-E1.9-D1

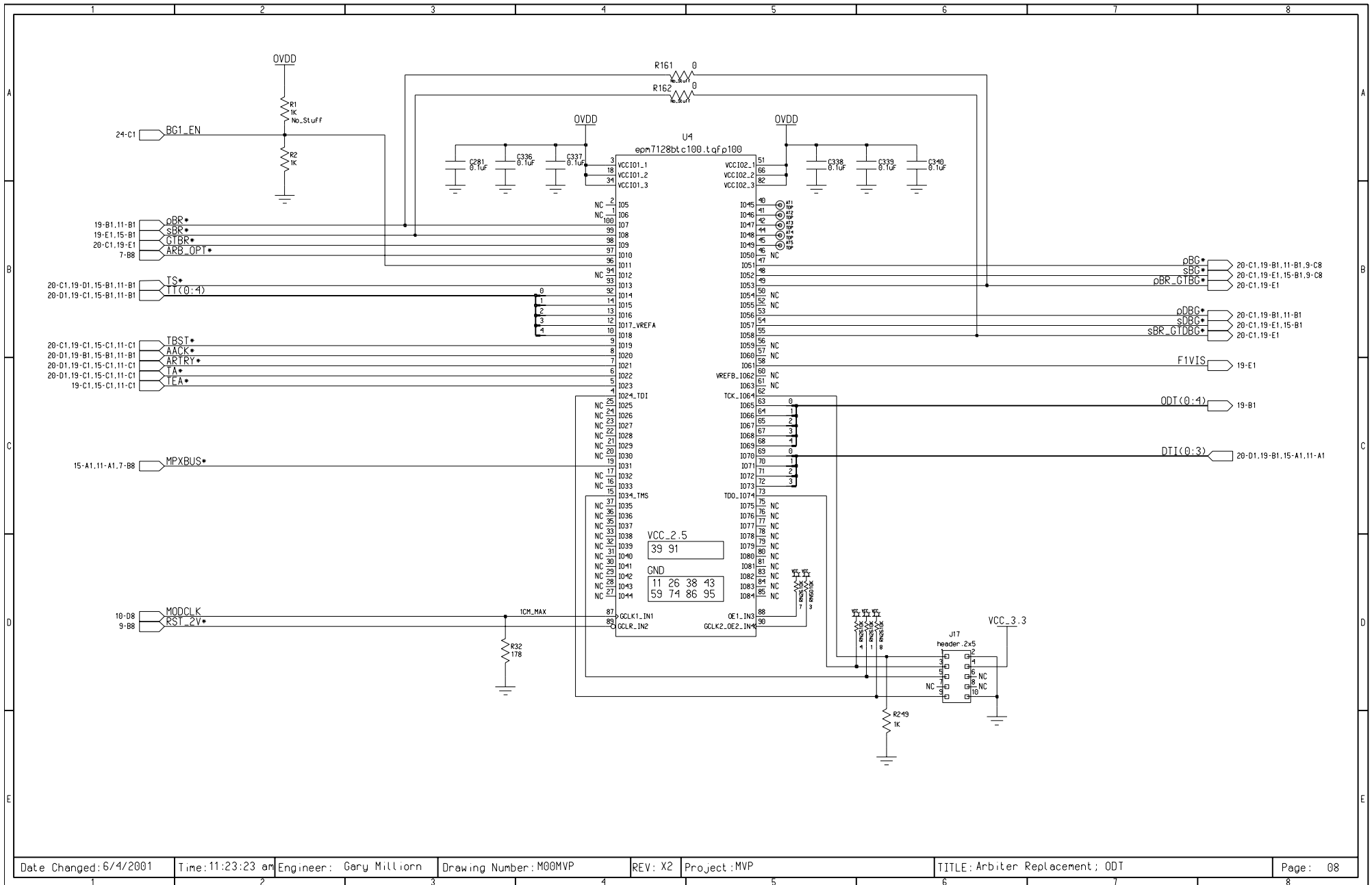
PWRSW → 35-E1

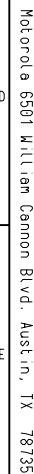
R271 0 pCOP\_SRST → 9-C1.7-B1  
 R265 0 sCOP\_SRST → 9-C1.7-D1  
 R266 0 pCOP\_CKSTPI → 9-C1.7-B1  
 R267 0 sCOP\_CKSTPI → 9-C1.7-D1  
 R268 0 pMCP → 11-D1  
 R269 0 pSMI → 11-D1

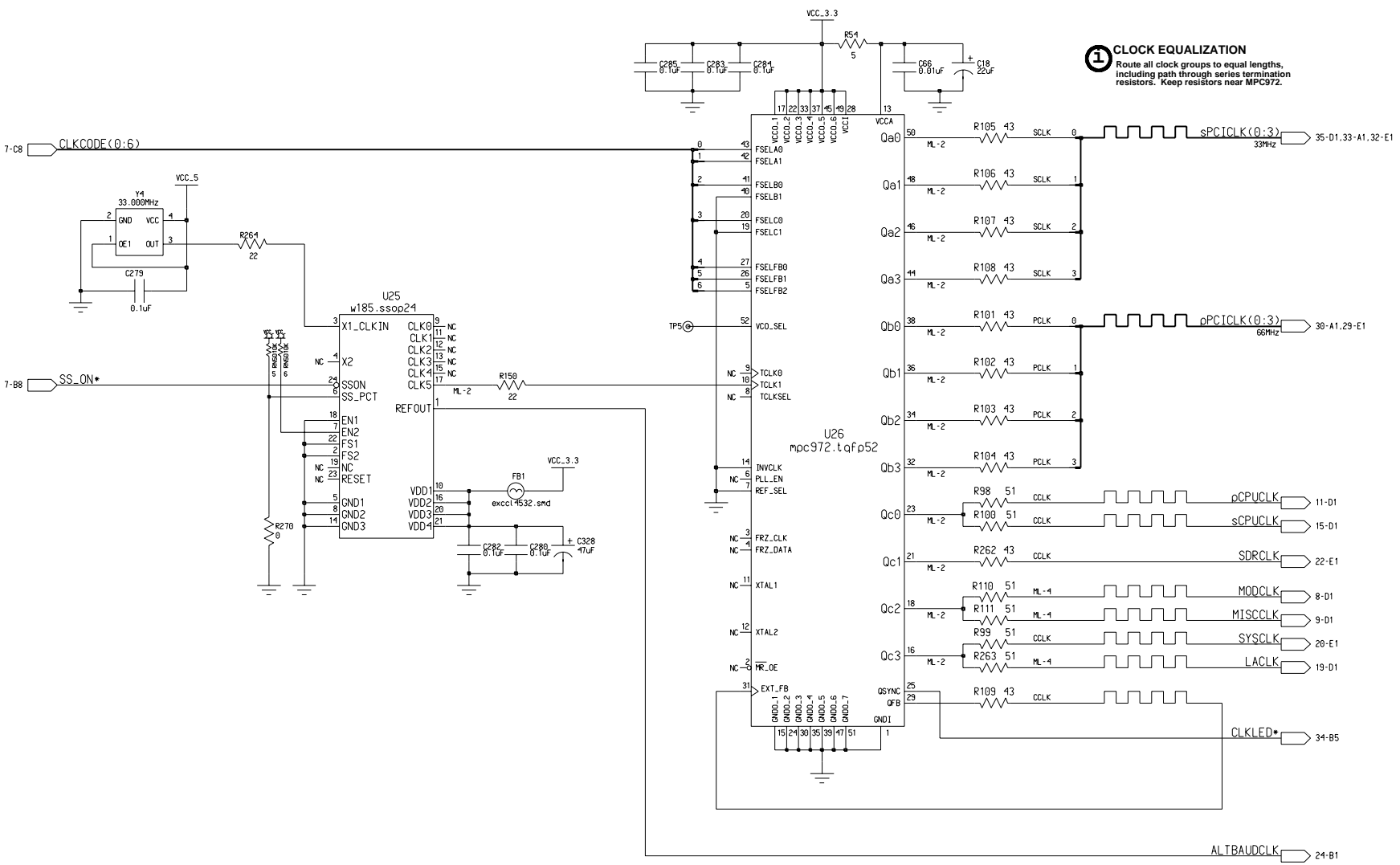


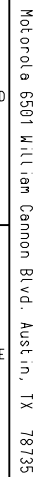


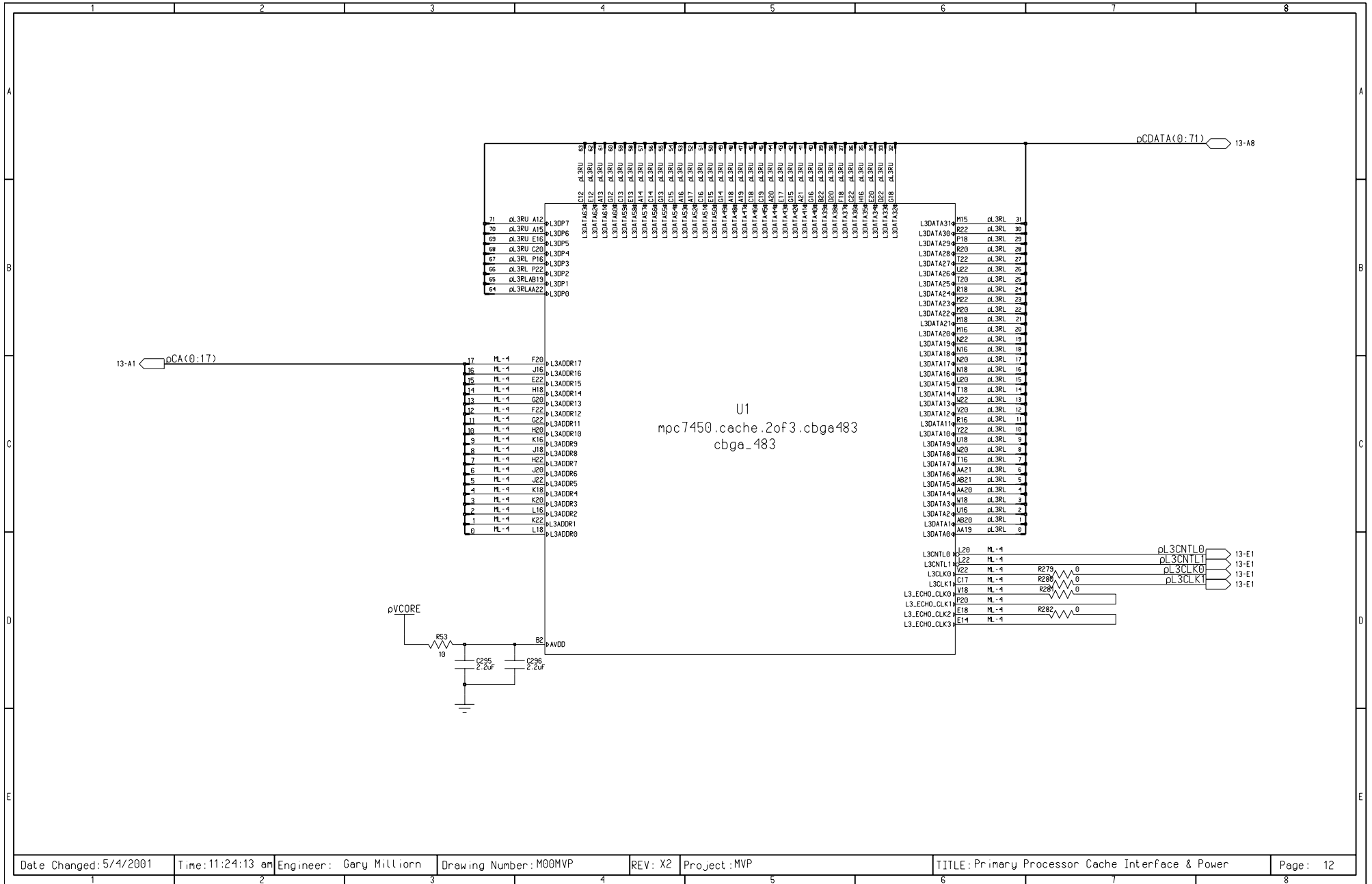




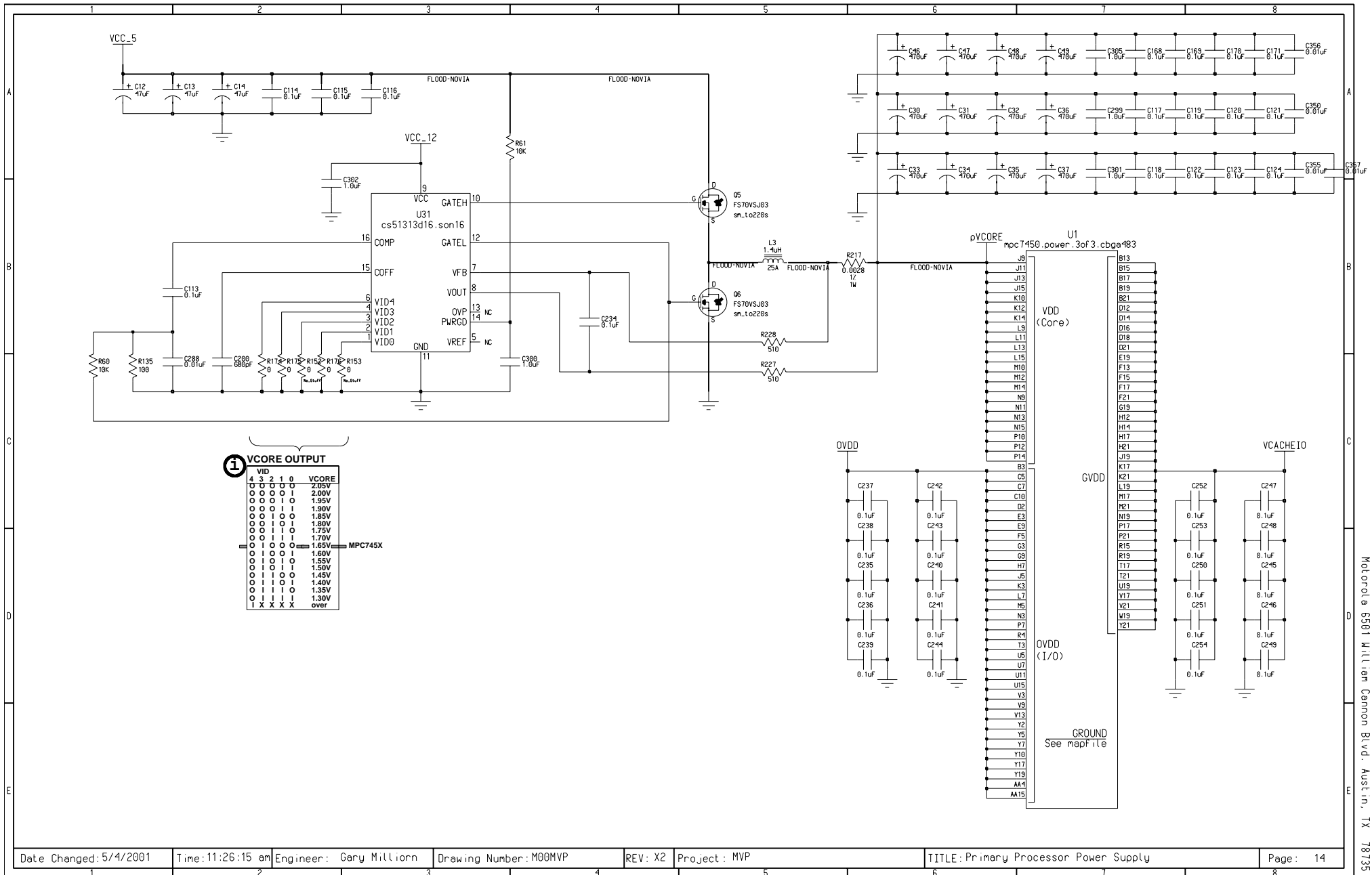


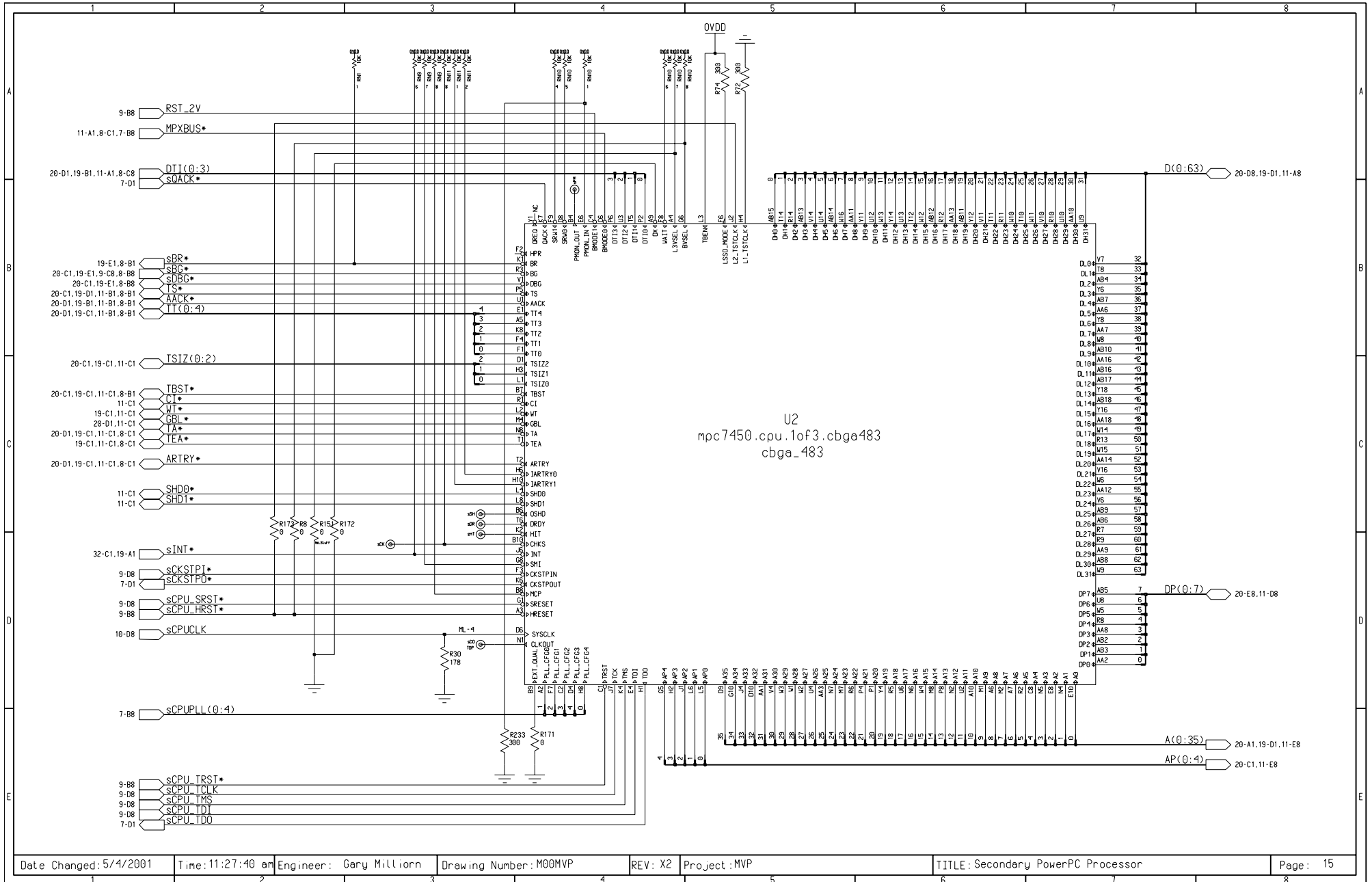


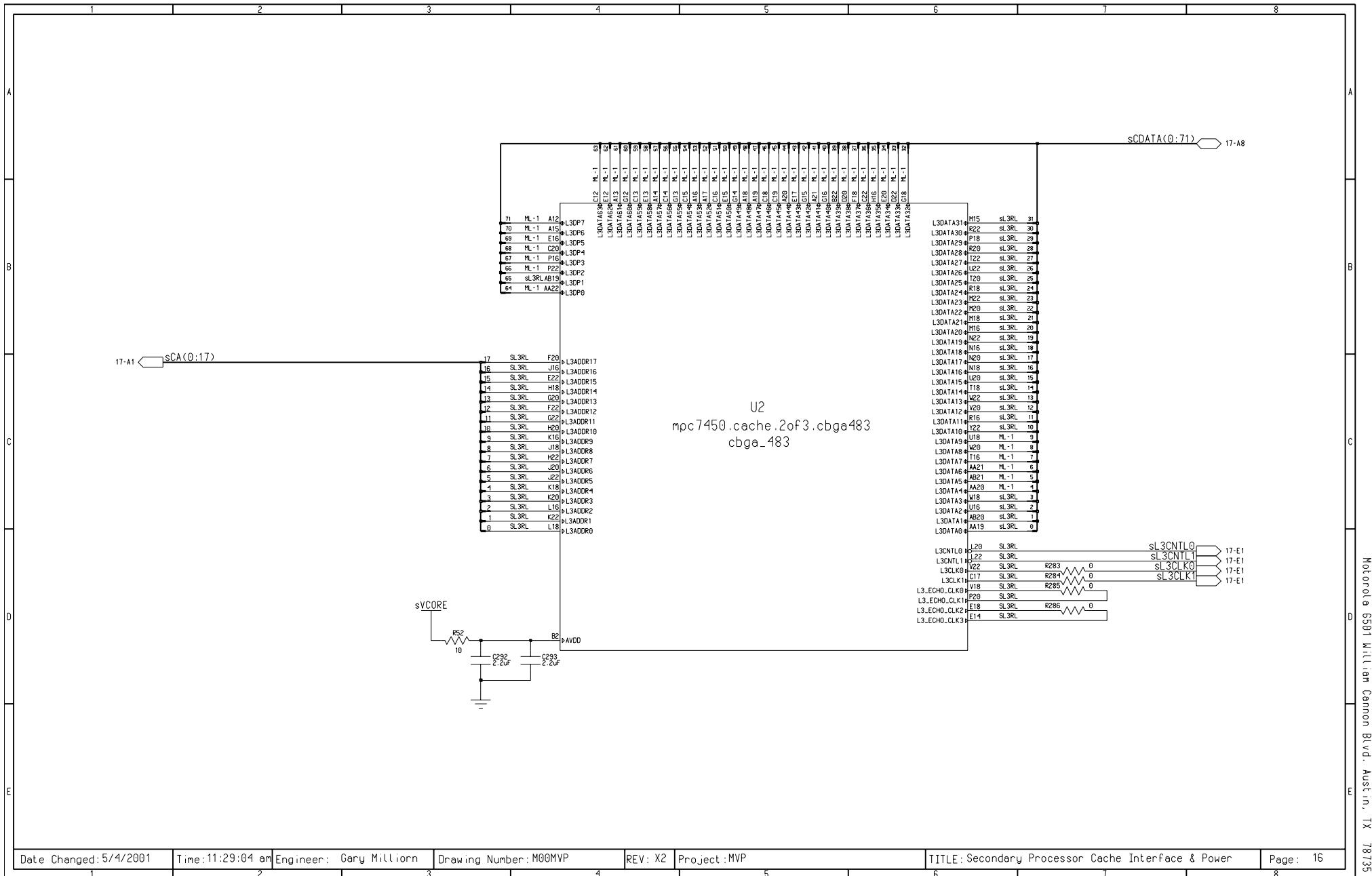


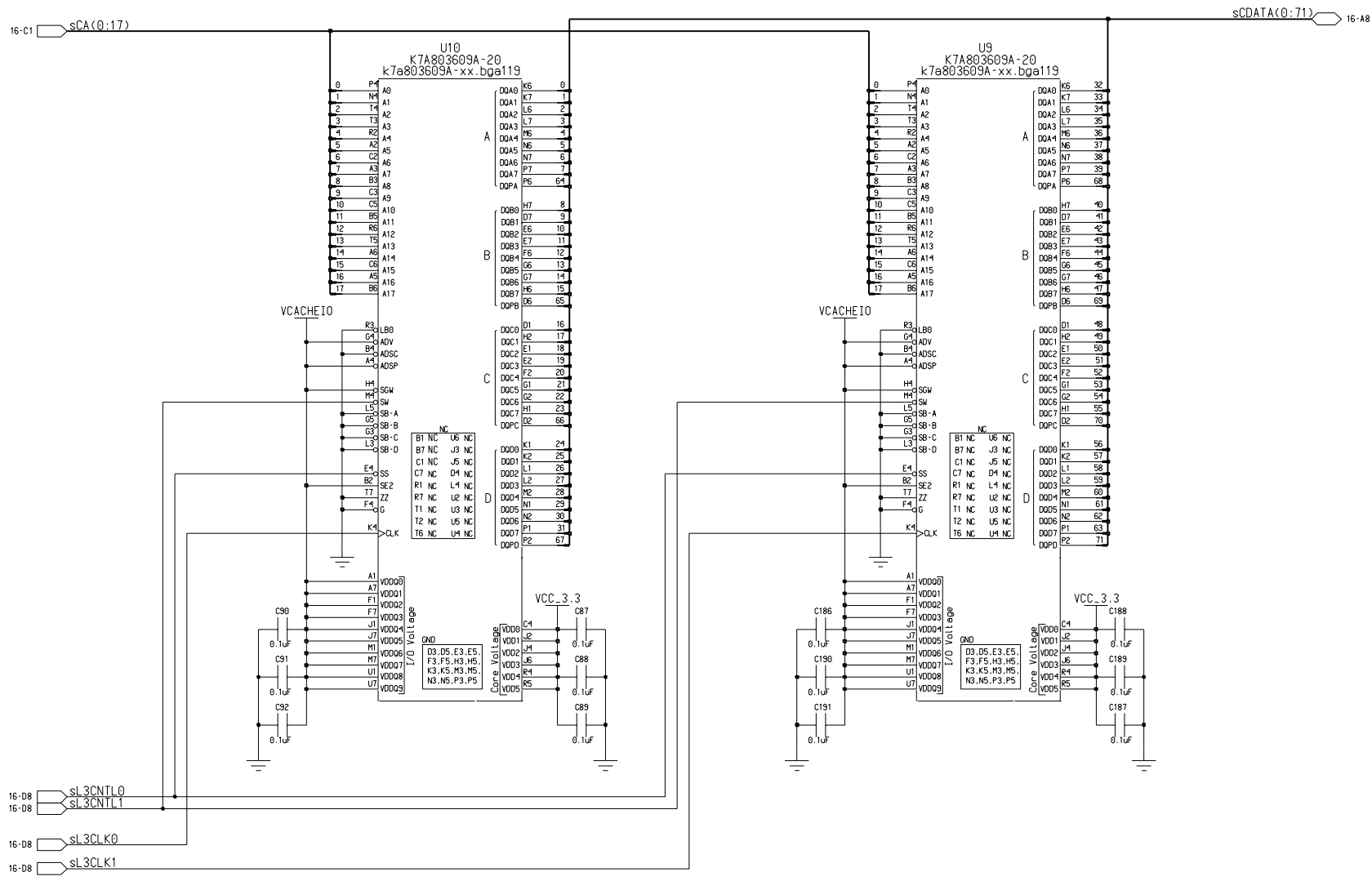


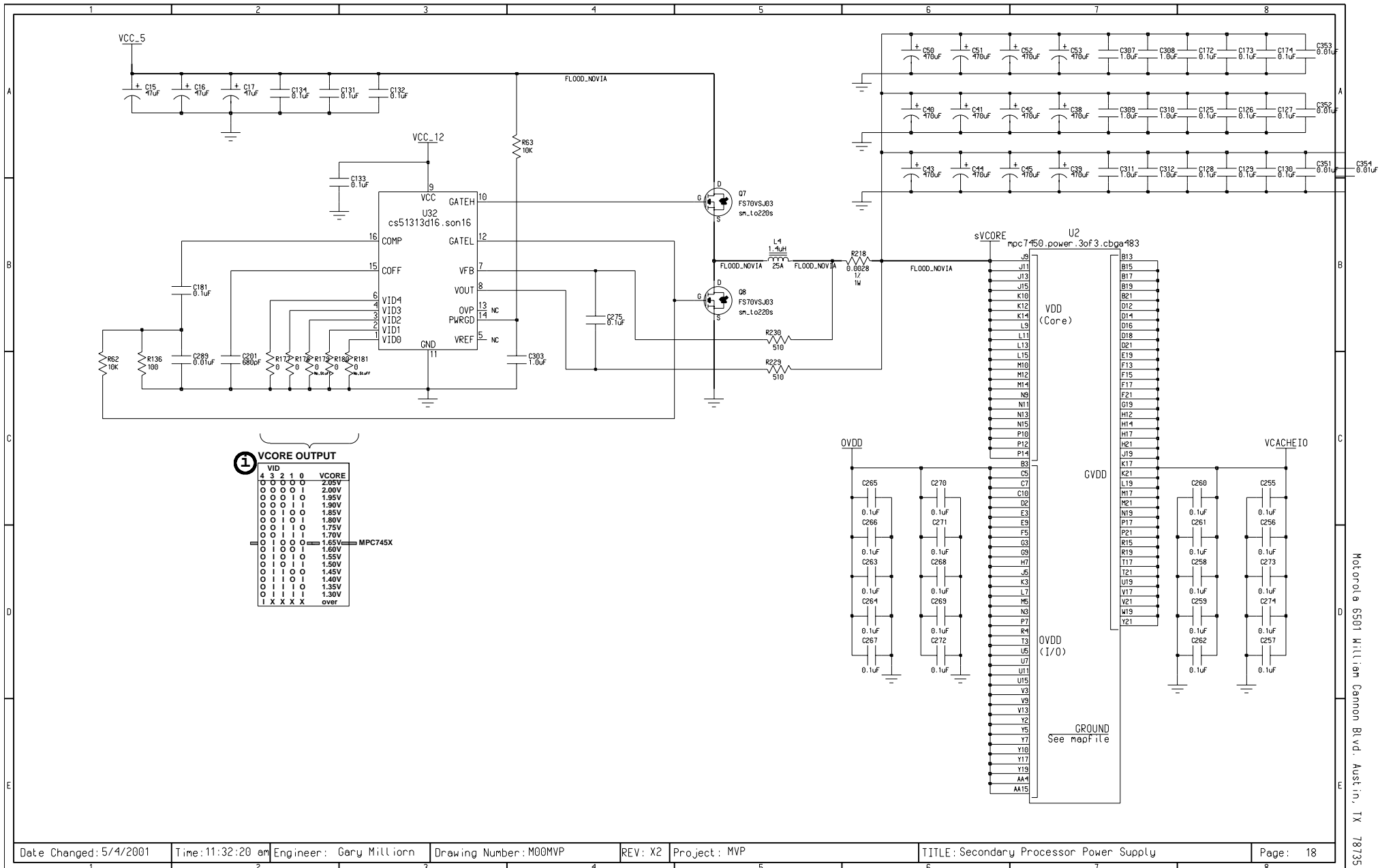


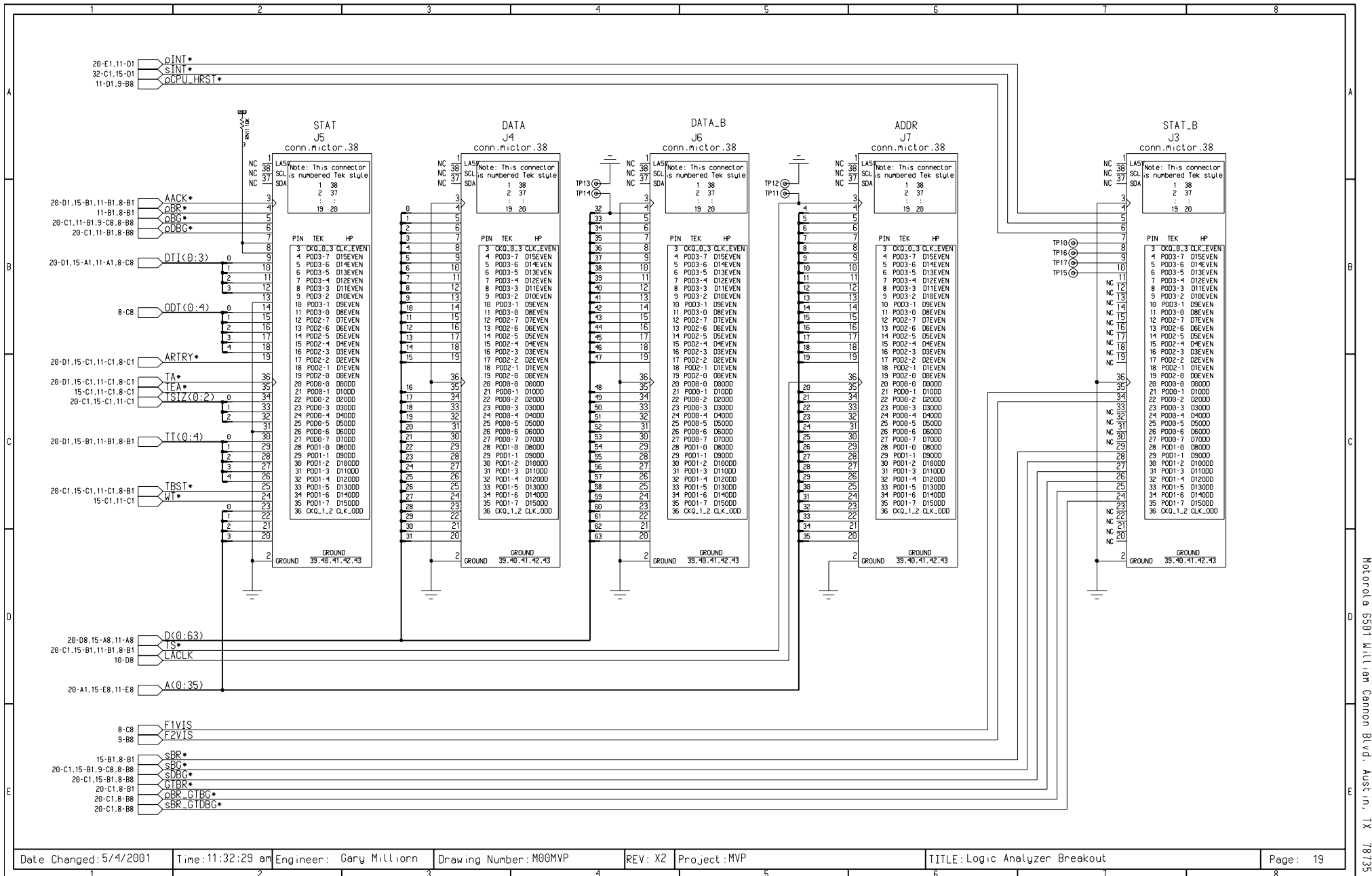


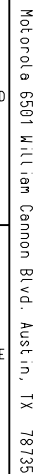


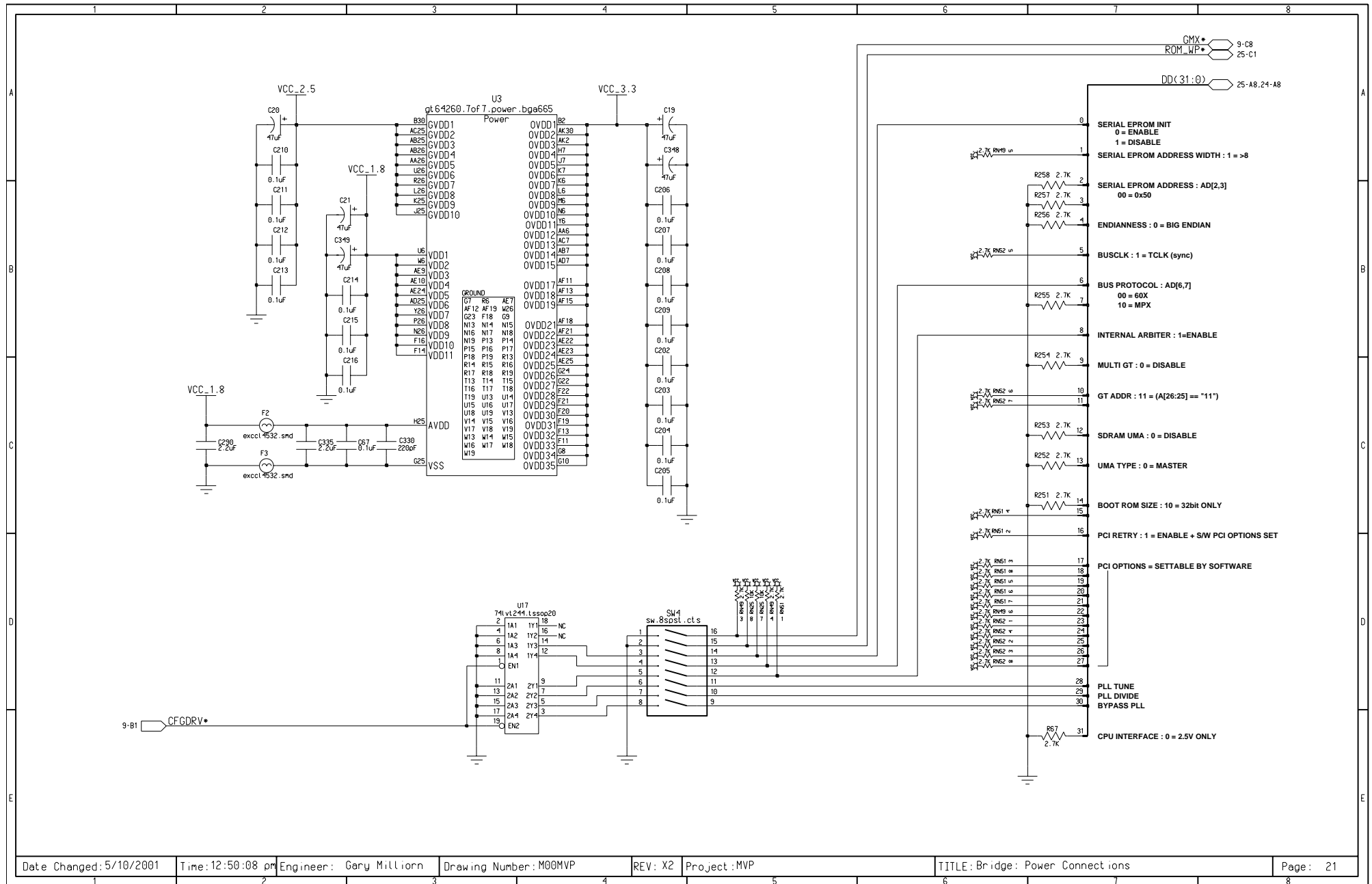


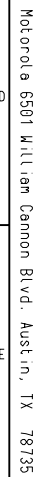


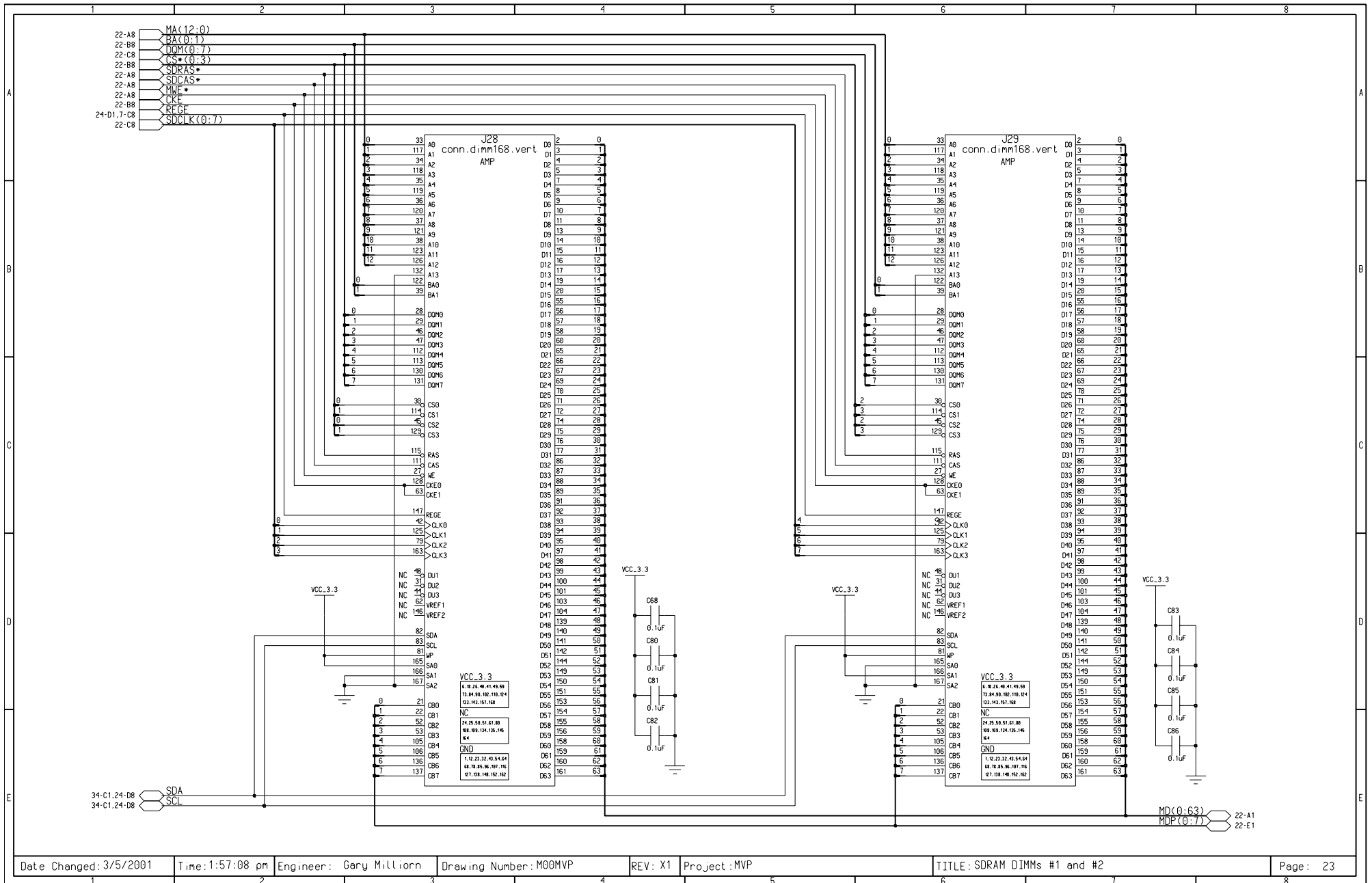


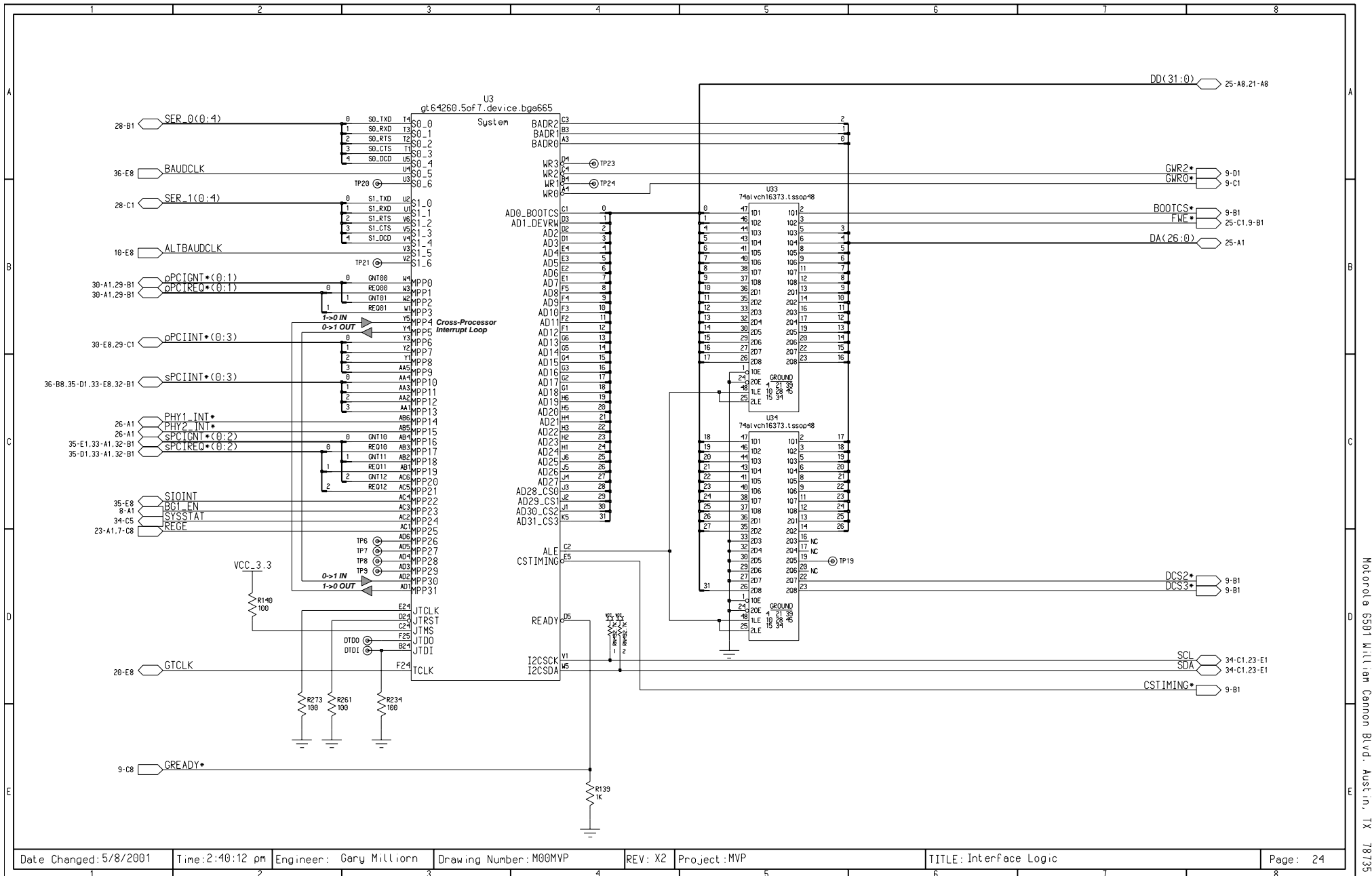


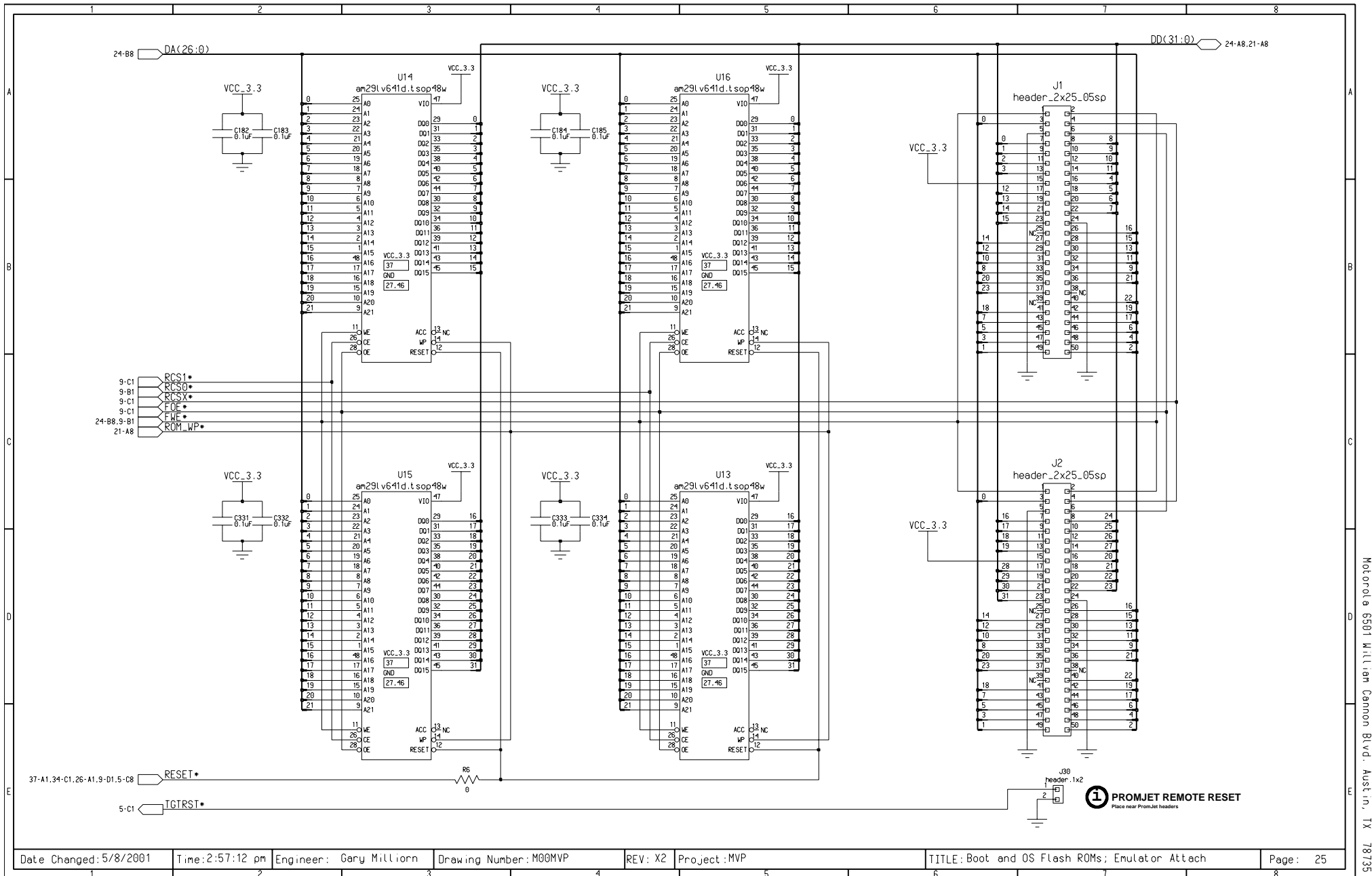


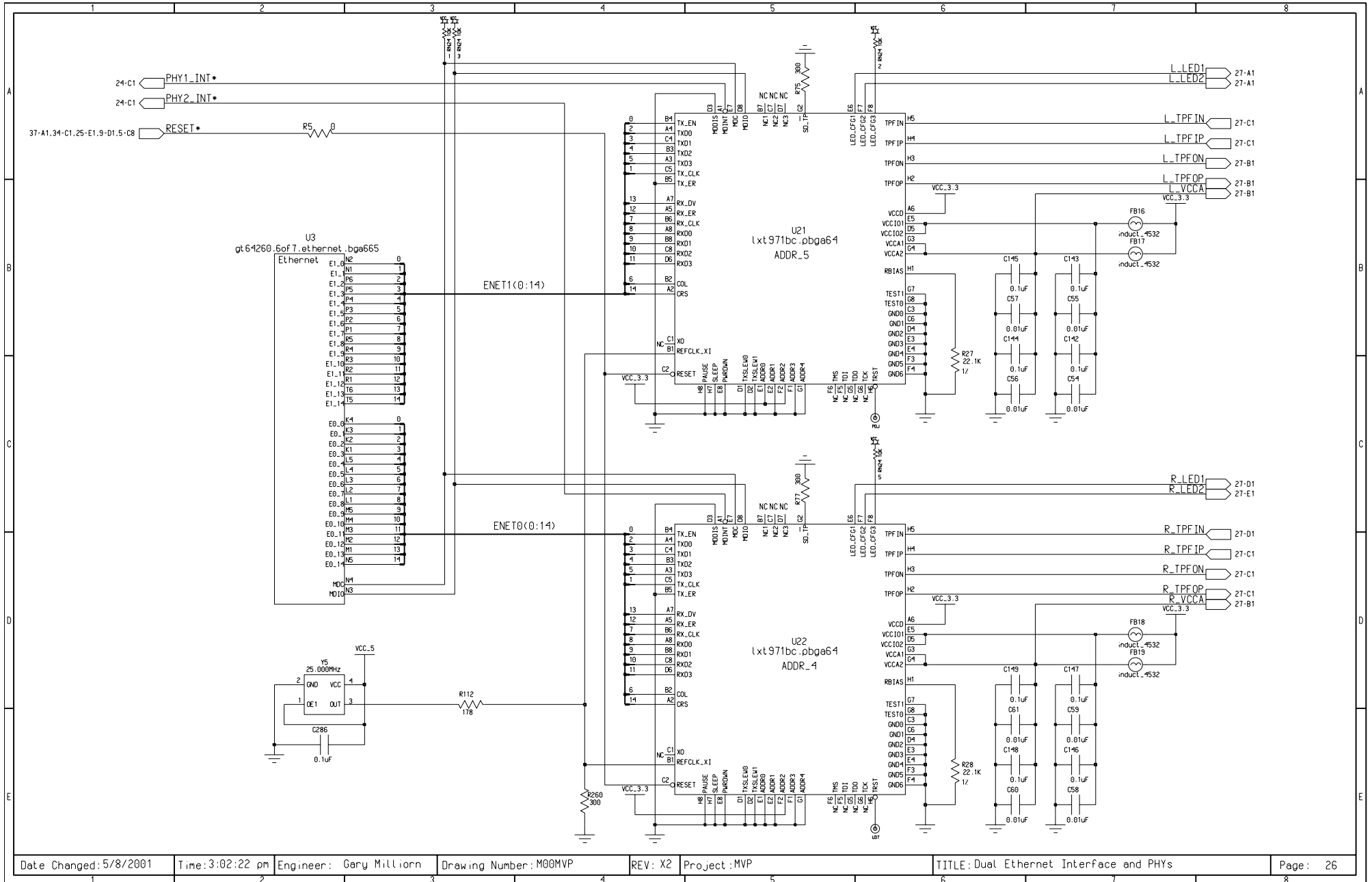


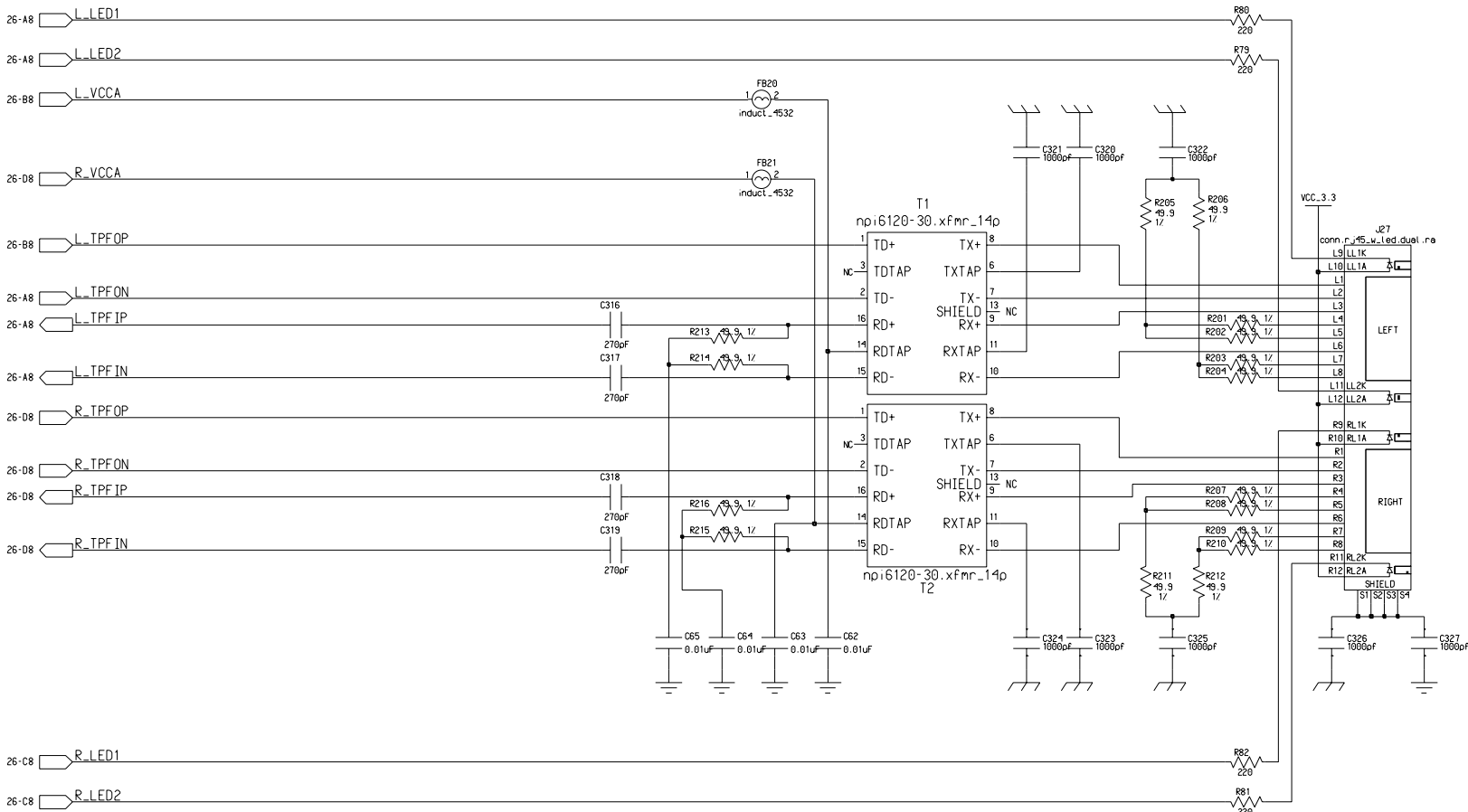


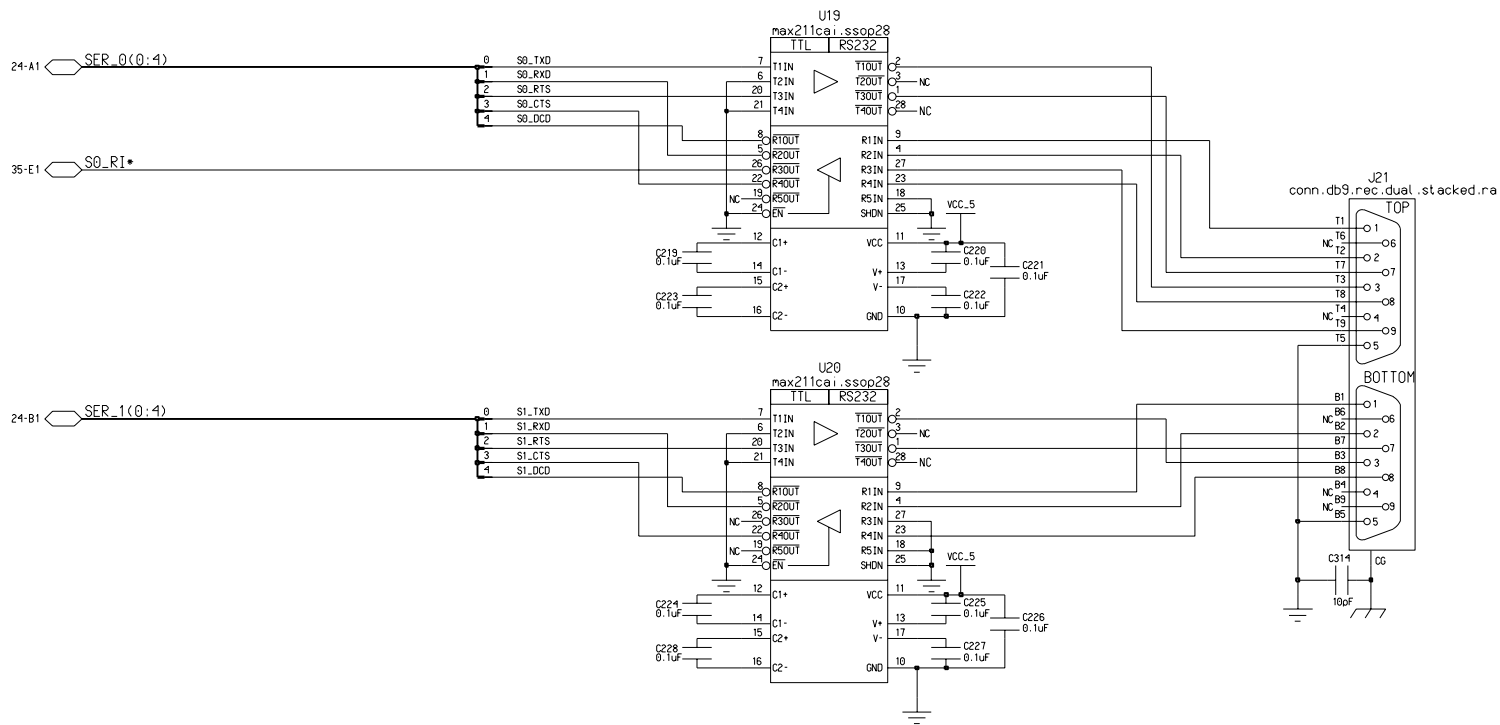




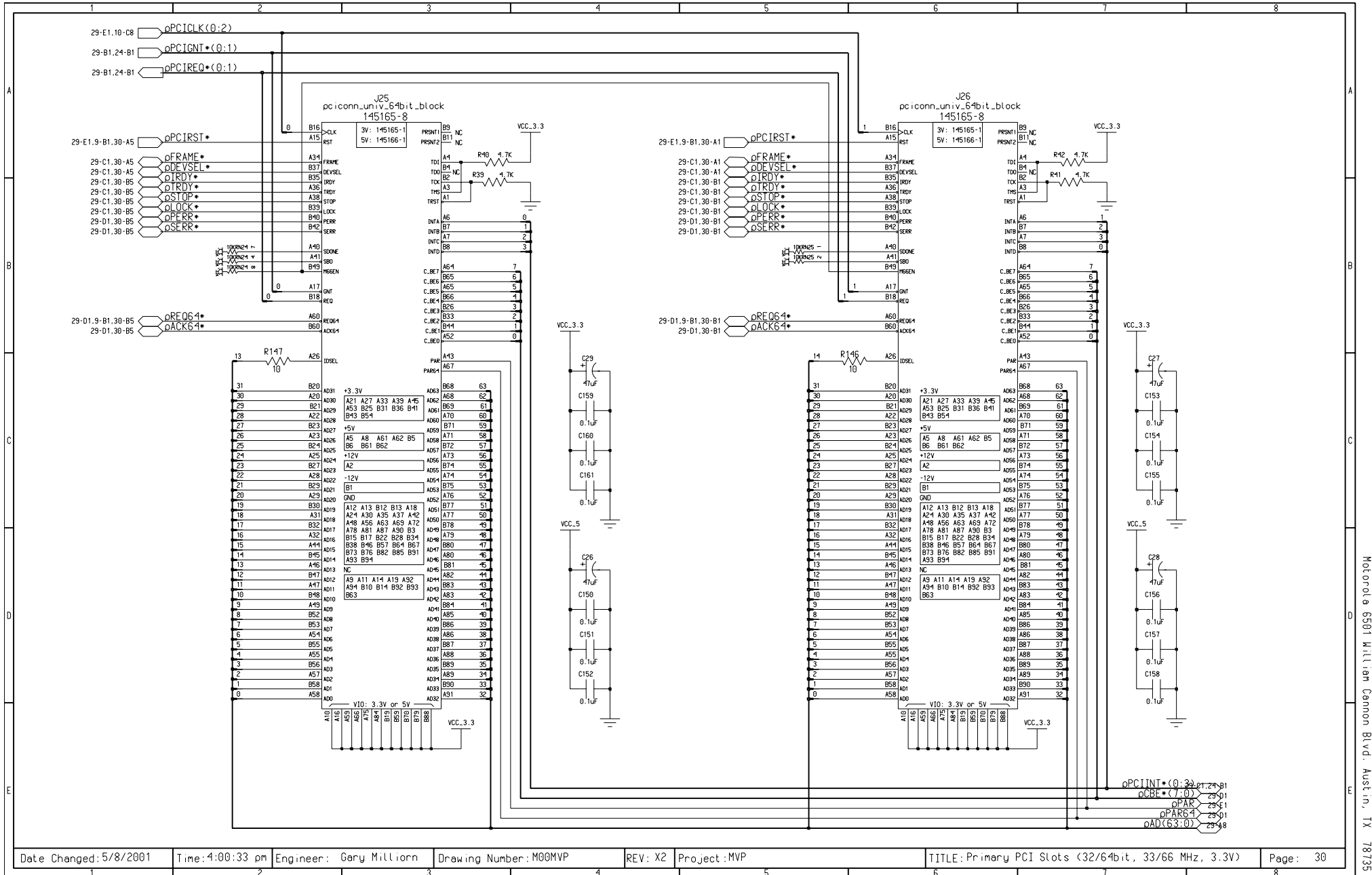












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A									A
B									B
C									C
D									D
E									E
<div><div>Date Changed: 5/8/2001</div><div>Time: 4:03:27 pm</div><div>Engineer: Gary Million</div><div>Drawing Number: M00MVP</div><div>REV: X2</div><div>Project: MVP</div><div>TITLE: Cryptographic Engine</div><div>Page: 31</div></div>									
	1	2	3	4	5	6	7	8	

