1 - TITLE PAGE

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COLOR LEGEND

NOTE:
NOTES IN GREEN TEXT ARE GENERAL DESIGN OR SCHEMATIC NOTES

LAYOUT NOTE:
NOTES IN VIOLET TEXT ARE PCB LAYOUT RECOMMENDATIONS OR GUIDLINES

NOTES IN BLACK TEXT INDICATE A PARTICULAR FUNCTIONALITY OF A SPECIFIC PART OF THE SCHEMATIC FOR CLARIFICATION OF THE FUNCTIONALITY.

NOTE: DNA IS AN ABBREVIATION FOR "DO NOT ASSEMBLE", WHICH APPLIES TO COMPONENTS THAT ARE NOT MEANT TO BE POPULATED ON THE BOARD.

THIRD ANGLE PROJECTION

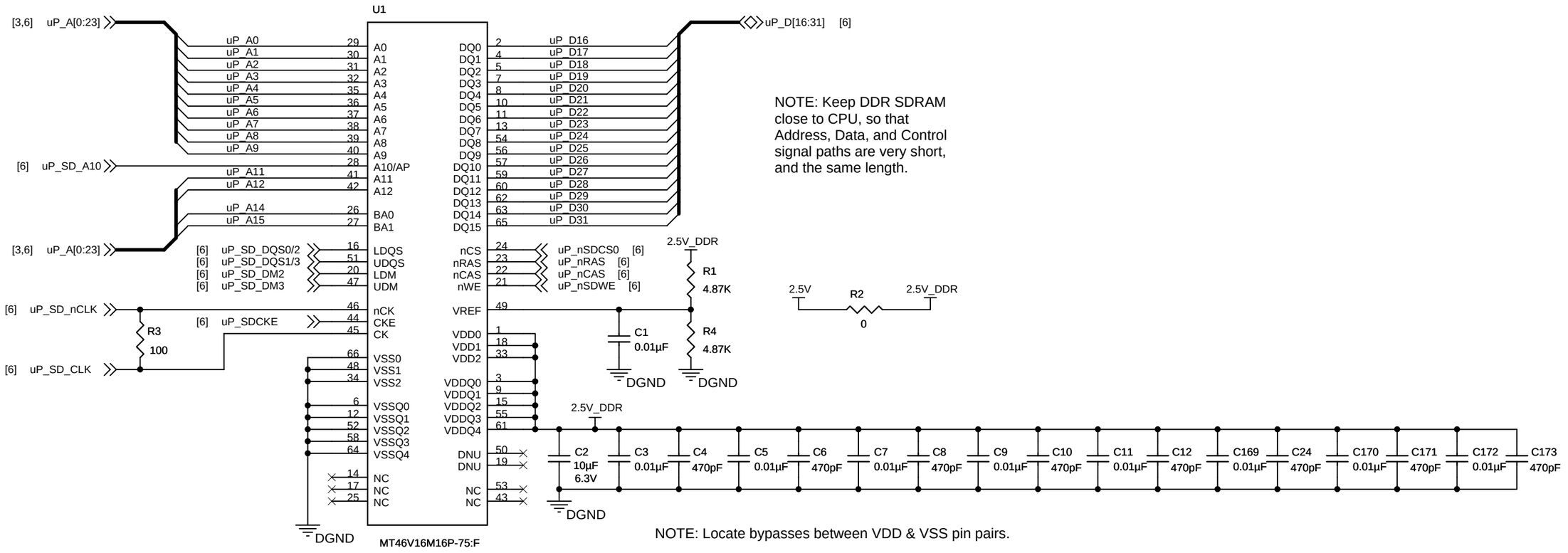
FEATURES AND DIMENSIONS NOT SHOWN SHALL BE VERIFIED IN THE DATABASE. DRAWING SHOULD NOT BE SCALED

DRAWING TITLE: 5329 / QG8 REFERENCE DESIGN

PROJECT NAME: FREESCALE POS TERMINAL

ENGR: J. P. KELL	SIZE	DATE	DRAWING NO.	REV
DRAWN: M. J. KIDD	B	5-15-06	117E04	P4
		SCALE: NO SCALE	SHEET 1 OF 10	

2 - DDR SDRAM



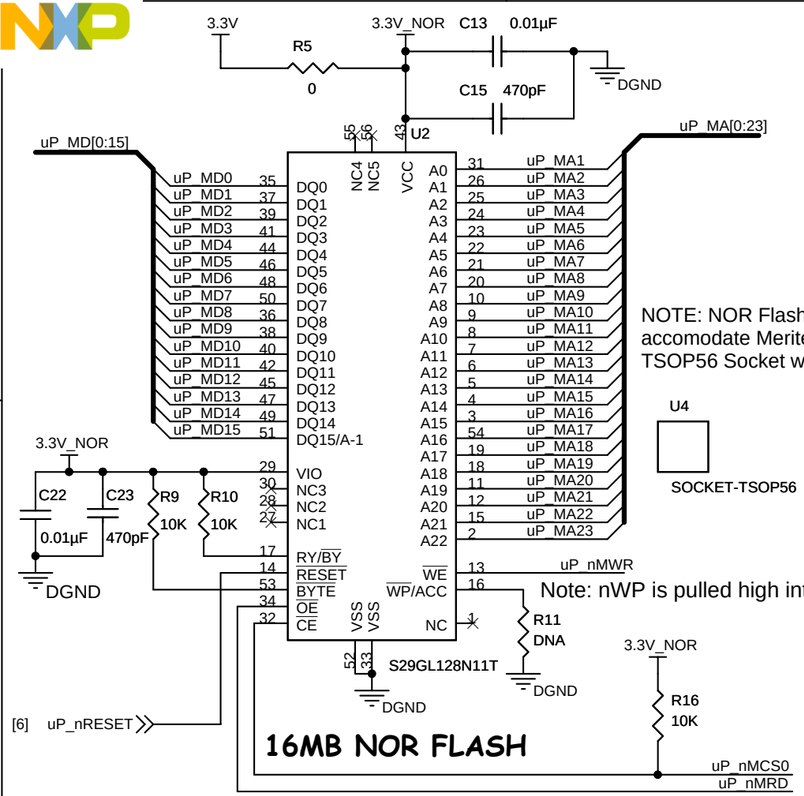
NOTE: Keep DDR SDRAM close to CPU, so that Address, Data, and Control signal paths are very short, and the same length.

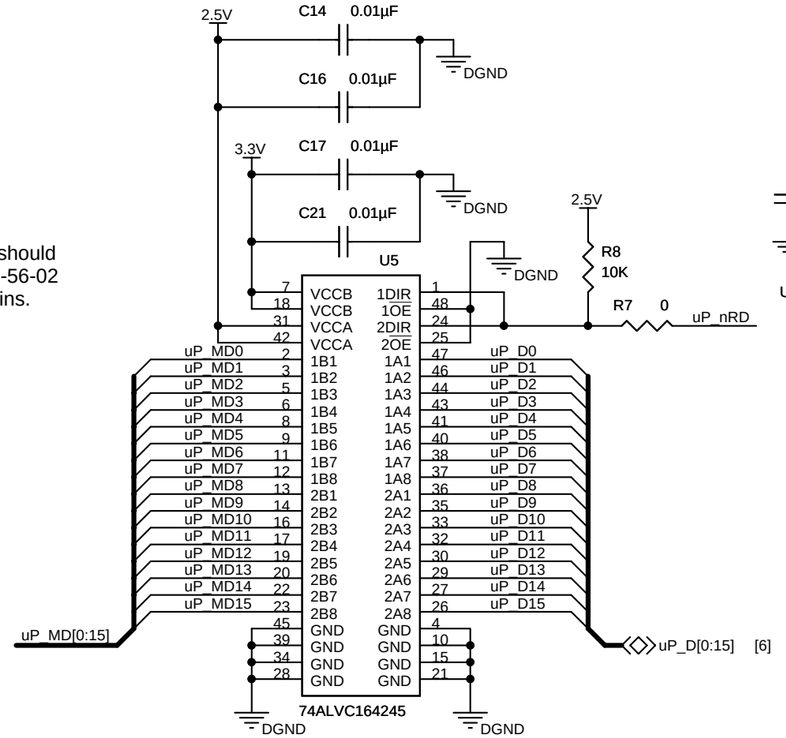
NOTE: Locate bypasses between VDD & VSS pin pairs.

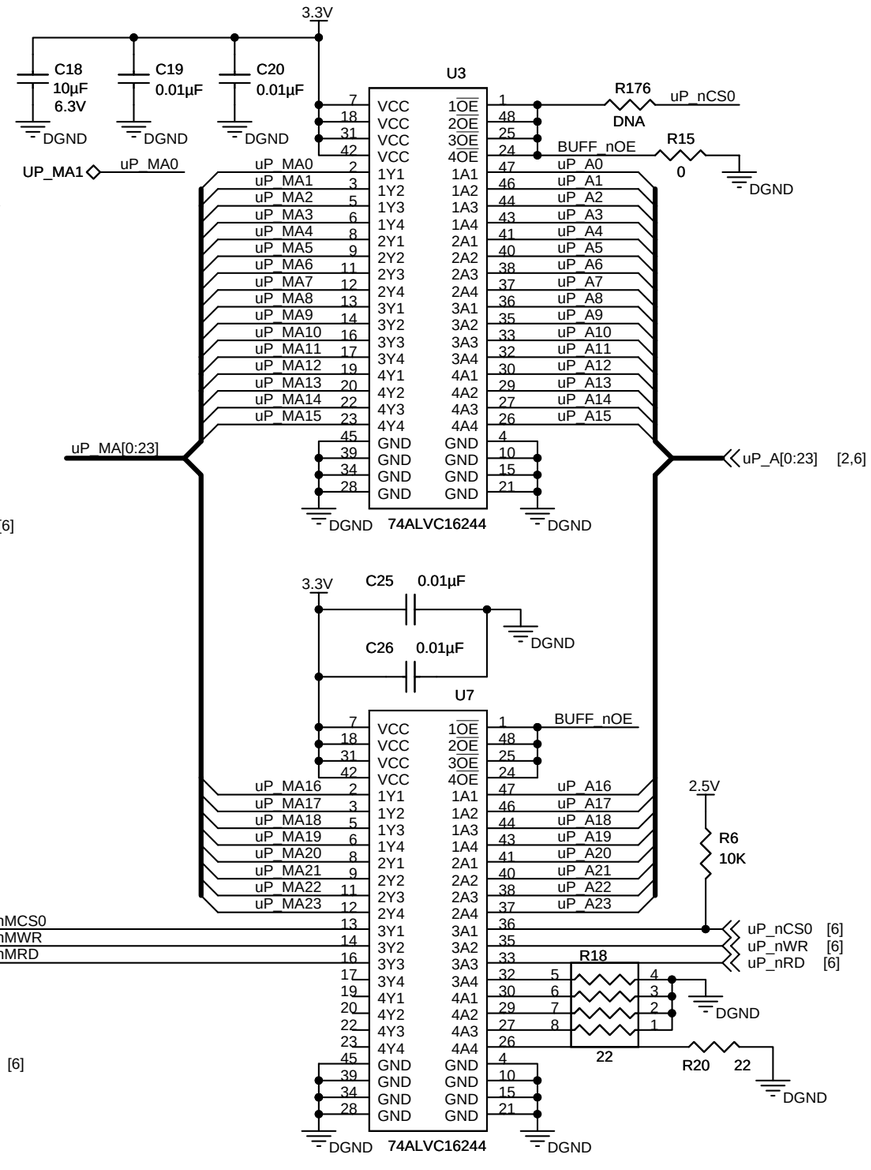
32MB DDR SDRAM

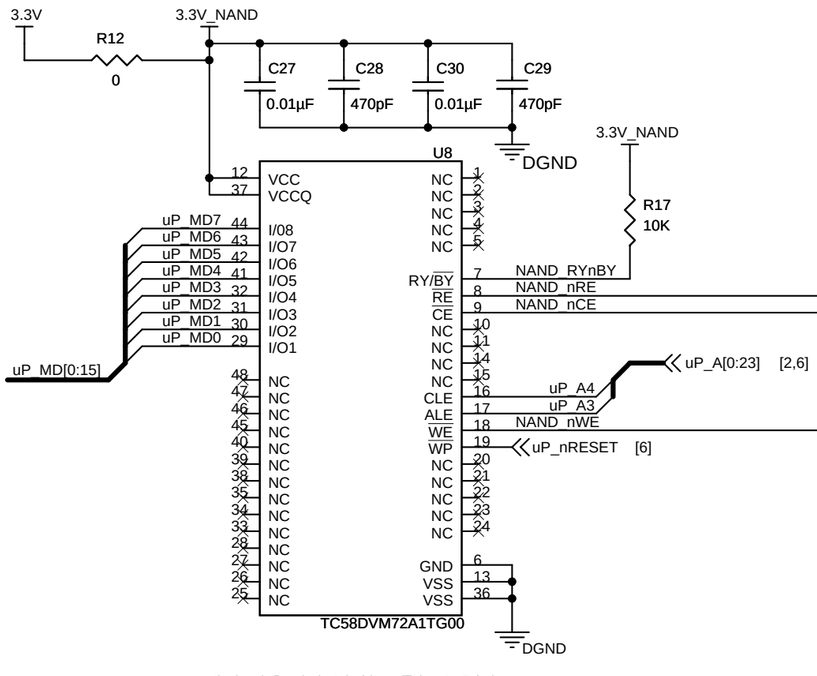
SIZE	DATE	DRAWING NO.	REV
B	5-15-06	117E04	P4
	SCALE: NO SCALE	SHEET 2 OF 10	

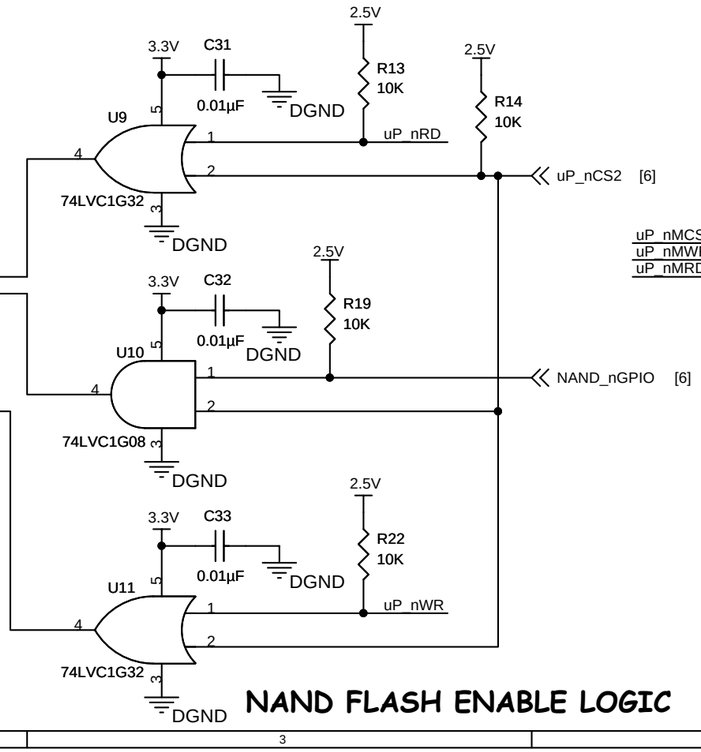
3 - NOR & NAND FLASH











SIZE	DATE	DRAWING NO.	REV
B	5-15-06	117E04	P4
	SCALE: NO SCALE	SHEET 3 OF 10	

4 - ETHERNET PHY & RS-232 PORT

[5,6,8] MSTR_nRESET
[6] uP_MDIO
[6] uP_MDC

R23 1.5K 3.3V_PHY
R24 0 3.3V 3.3V_PHY

NOTE: Minimize trace lengths between crystal & DP83848

C34 0.01µF 3.3V_PHY DGND

R25 270
R27 270
R26 470

Y1 25.0000MHz P
C35 27pF DGND
C36 27pF DGND

ETHERNET PHY

NOTE: PHY ADDRESS = 00001 BY DEFAULT

3.3V_PHY
R34 DNA (2.2K)

C38 0.1µF DGND
DGND

U12

		36	DGND
		35	IOGND
		34	X1
		33	X2
		32	IOVDD33
		31	MDC
		30	MDIO
		29	RESET_N
		28	LED_LINK/AN0
		27	LED_SPEED/AN1
		26	LED_ACT/COL/AN_EN
		25	25MHz_OUT
[6] uP_RX_CLK	PFB	37	PFBIN2
[6] uP_RX_DV		38	RX_CLK
[6] uP_CRS		39	RX_DV/MII_MODE
[6] uP_RX_ER		40	CRS/CRS_DV/LED_CFG
[6] uP_COL		41	RX_ER/MDIX_EN
uP_RXD0		42	COL/PHYAD0
uP_RXD1		43	RXD_0/PHYAD1
uP_RXD2		44	RXD_1/PHYAD2
uP_RXD3		45	RXD_2/PHYAD3
		46	RXD_3/PHYAD4
		47	IOGND
		48	IOVDD33
		24	RBIAS
		23	PFBOUT
		22	AVDD33
		21	RESERVED1
		20	RESERVED
		19	AGND
		18	PFBIN1
		17	TD +
		16	TD -
		15	AGND
		14	RD +
		13	RD -
		1	TX_CLK
		2	TX_EN
		3	TXD_0
		4	TXD_1
		5	TXD_2
		6	TXD_3/SNI_MODE
		7	PWR_DOWN/INT
		8	TCK
		9	TDO
		10	TMS
		11	TRST#
		12	TDI

DP83848CVV

R28 4.87K PFB DGND
C37 0.1µF
C41 10µF 6.3V DGND
3.3V_PHY
C42 0.01µF DGND
R35 2.2K
R36 2.2K
PFB
C43 0.1µF DGND

C39 0.1µF DGND
C40 0.1µF DGND
3.3V_PHY
R30 49.9
R31 49.9
R32 49.9
R33 49.9

[6] uP_RXD[0:3]
R37 DNA (2.2K) DGND
R38 DNA (2.2K) DGND

MII, LED, & MDIX STRAPPING OPTIONS

3.3V_PHY
C44 10µF 6.3V DGND
C45 0.01µF DGND

TEST PINS HAVE INTERNAL PULL UPS/DOWNS

[6] uP_TX_CLK
[6] uP_TX_EN
[6] uP_TXD[0:3]
[6] PHY_nIRQ

uP_TXD0 uP_TXD1 uP_TXD2 uP_TXD3

RJ-45 ETHERNET PORT

U13

1	TDP
2	TDN
3	RDP
4	TDC
5	RDC
6	RDN
7	NC
8	CAP
11	YEL_C
12	YEL_A
10	GR_C
9	GR_A
13	CHASSIS
14	CHASSIS

Mod 8P8C

R39 0 DGND
C46 0.1µF DGND
C47 0.1µF DGND
3.3V_PHY
3.3V_PHY
3.3V_PHY

NOTE: Place Caps close to XFMR center taps.

RS-232 TRANSCEIVER

3.3V
C48 470pF
C49 0.1µF
DGND

U14

1		20	FORCEOFF
2	READY	19	VCC
3	C1+	18	GND
4	V+	17	T1OUT
5	C1-	16	R1IN
6	C2+	15	R1OUT
7	C2-	14	FORCEON
8	V-	13	T1IN
9	T2OUT	12	T2IN
10	R2IN	11	INVALID
	R2OUT		

MAX3225E

C50 0.1µF
C51 0.1µF
C52 0.1µF DGND
C53 0.1µF DGND
DGND

R180 0
R181 0
R182 0
R183 0
R179 0 DGND

J1

5	
9	
4	
8	
3	
7	
2	
6	
1	
10	
11	

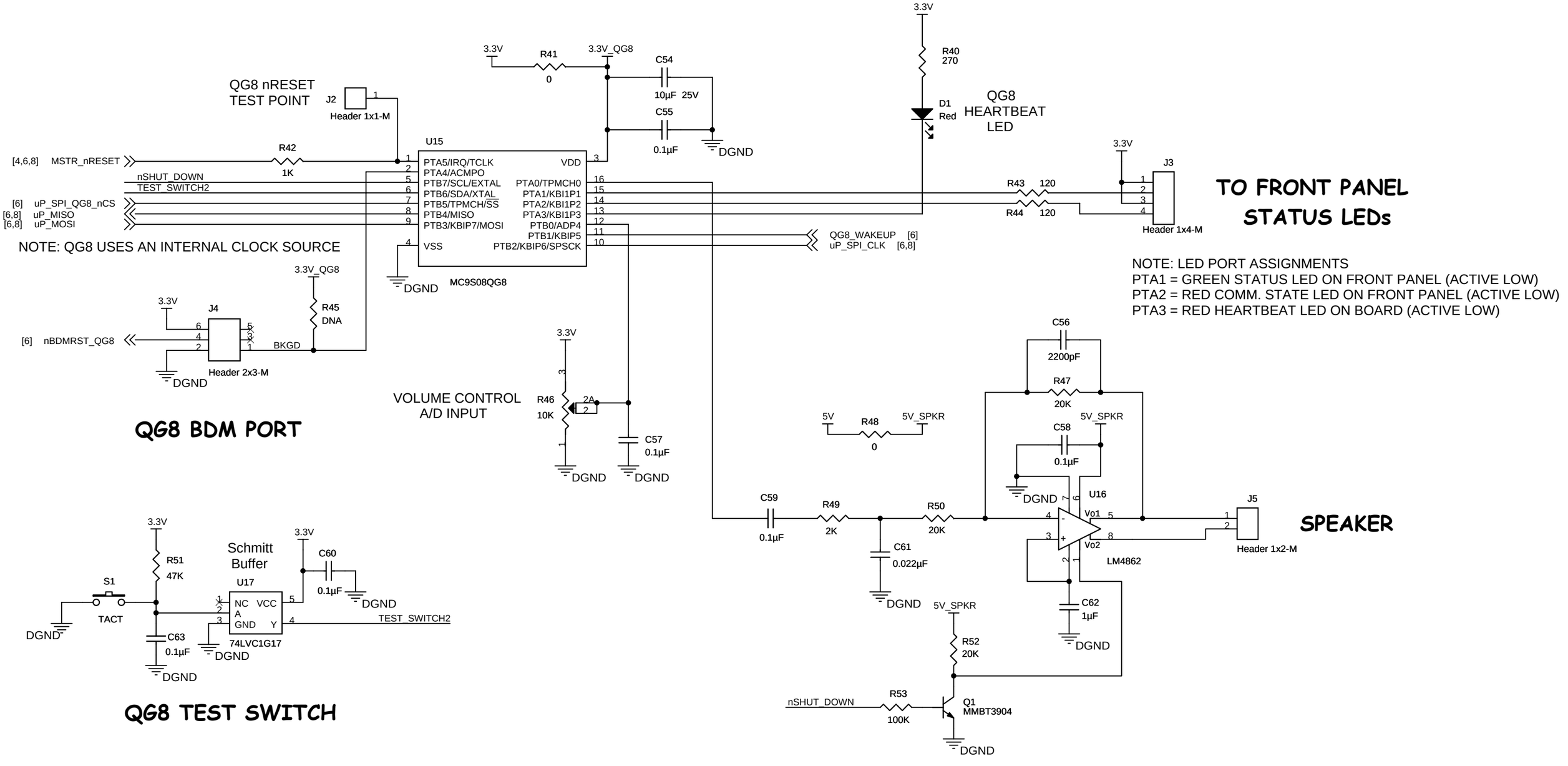
D-Sub 9-F

RS-232 PORT (WIRED AS DCE - USE STANDARD MODEM CABLE)

[6] uP_UARTA_RX
[6] uP_UARTA_TX
[6] uP_UARTA_RTS
[6] uP_UARTA_CTS

SIZE	DATE	DRAWING NO.	REV
B	5-15-06	117E04	P4
	SCALE: NO SCALE	SHEET 4 OF 10	

5 - MC9S08QG8 PROCESSOR



SIZE	DATE	DRAWING NO.	REV
B	5-15-06	117E04	P4
	SCALE: NO SCALE	SHEET 5 OF 10	

6 - COLDFIRE MCF5329 PROCESSOR

RESET CIRCUIT

RESET BUTTON

SCHMITT BUFFER

RESET LED

RESET INPUT FROM Q68 BDM PORT

Power Fail Interrupt is generated when 12V Supply decreases to 10V.

5329 BDM/JTAG PORT

NOTE: Place near Board Edge with Pin 1 on outside. Confirm that sufficient clearance exists for BDM Pod & Cable.

NOTE: Keep BDM signal path lengths (DDATA & PST) the same and less than 3" long.

NOTE: R161 is normally populated

NOTE: R160 is normally populated and R159 is not.

NOTE: ONLY 3.3V BDM debugging cables can be used with MCF532x processors.

5329 HEARTBEAT LED

5329 TEST LEDS

5329 IRQ SWITCH

5329 TEST SWITCH

5329 TEST SWITCHES

CPU REGISTER CONFIGURATION SETTINGS UPON RESET

PLL Mode uP_D1	Mode
LOW	180MHz/60MHz
HIGH	240MHz/80MHz *

Encoded Boot Device (Port Size) uP_D3	uP_D4	Mode
LOW	LOW	32-bit port
LOW	HIGH	8-bit port
HIGH	LOW	16-bit port*
HIGH	HIGH	32-bit port

Limp Mode Selection uP_D6	Mode
LOW	Normal PLL mode *
HIGH	Limp mode

CPU Register Configuration RCON_b	Mode
LOW	Enabled*
HIGH	Disabled

Oscillator Mode uP_D2	Mode
LOW	Crystal oscillator *
HIGH	Oscillator bypass

Output Pad Drive Strength uP_D5	Mode
LOW	Low drive
HIGH	High drive *

Encoded Address/Chip Select Configuration uP_D8	uP_D9	Mode
LOW	LOW	A[23:22] = A[23:22]*
LOW	HIGH	A23 = FB_CS5_b, A22 = A22
HIGH	LOW	Reserved
HIGH	HIGH	A[23:22] = FB_CS[5:4]_b

TEST POINTS

Note: Place Signal Names in silkscreen next to Test Point Pin.

NOTE: Keep BDM signal path lengths (DDATA & PST) the same and less than 3" long.

NOTE: Place 1.5V_PLL filter circuit as close as possible to Pins J12 (VDD_A_PLL) and K13 (VSS_PLL) on the MCF5329 CPU.

NOTE: Place USB_3.3V filter circuit as close as possible to Pin L14 on the MCF5329 CPU.

NOTE: Place OSC_3.3V filter circuit as close as possible to Pins K12 (VDD_OSC) and L12 (VSS_OSC) on the MCF5329 CPU.

Freescale ColdFire(R) Microprocessor MCF5329

MCF5329CVM240

NOTE: please place the resistor packs below as close to CPU as possible.

INTERFACE TO SHARP LQ084S3DG01 8.4" TFT SVGA LCD

TEST POINTS

SPI PORT TO Q68 & ZIGBEE

USB PORTS

NOTE: there should be a 90ohm differential phase impedance between signals uP_USBx_D- & uP_USBx_D+. Please couple these traces as soon as they leave the CPU through to the USB jacks.

TO 5329 JTAG/BDM CONNECTOR

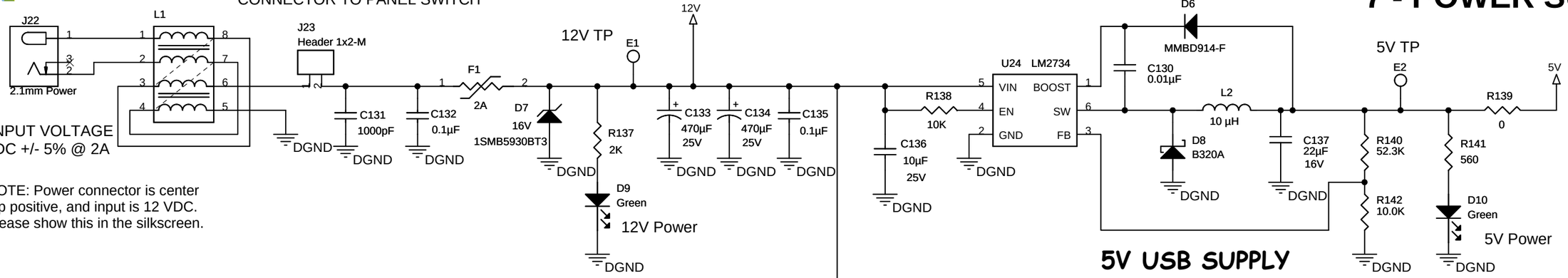
5329 JTAG/BDM SELECTION JUMPER

JTAG/BDM Configuration Jumper Position	Mode
1-2	JTAG
2-3	BDM

PROPRIETARY USE PURSUANT TO COMPANY INSTRUCTIONS

SIZE	DATE	DRAWING NO.	REV
D	5-15-06	117E04	P4
	SCALE: NO SCALE	SHEET 6 OF 10	

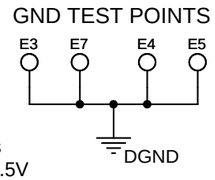
7 - POWER SUPPLIES



NOTE: Power connector is center tap positive, and input is 12 VDC. Please show this in the silkscreen.

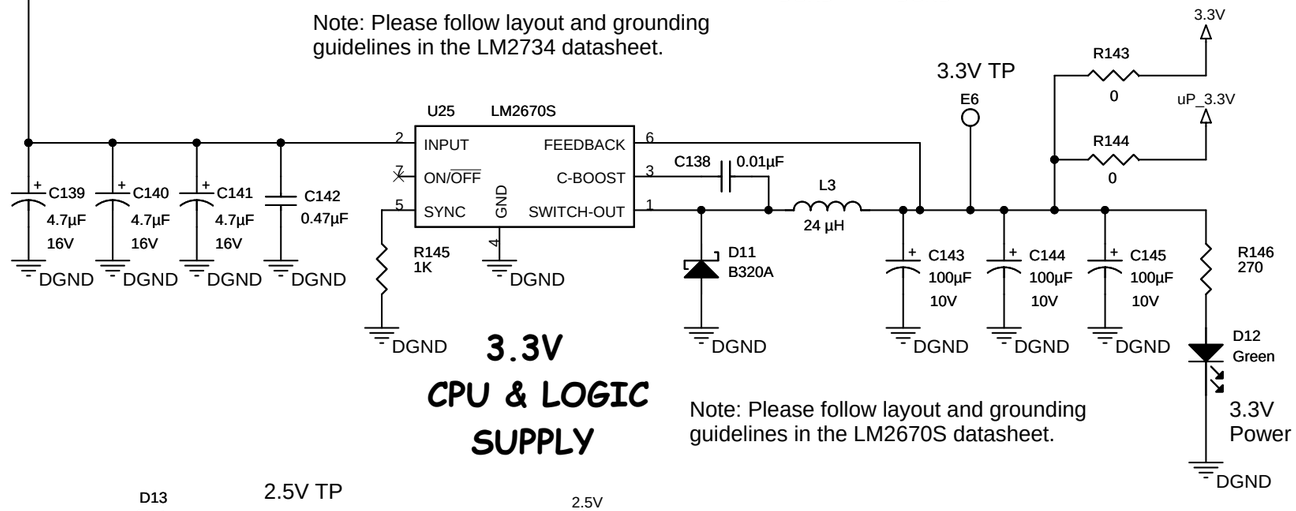
5V USB SUPPLY

Note: Please follow layout and grounding guidelines in the LM2734 datasheet.



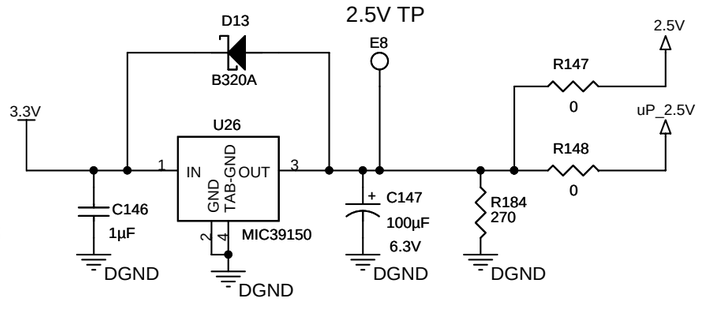
Note: Place GND Test Points in four corners of board and add Silkscreen Labels.

Also add Silkscreen Labels for 12V, 5V, 3.3V, 2.5V, & 1.5V Test Points.



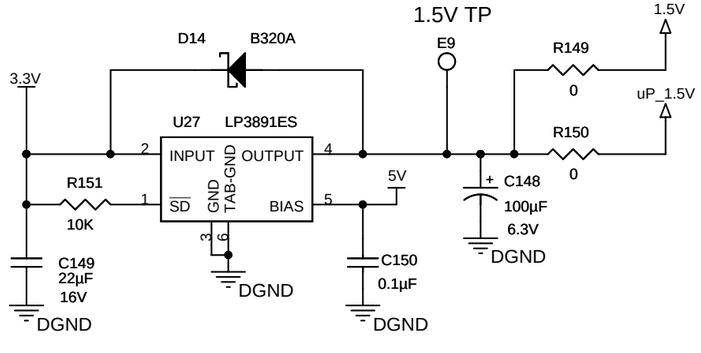
3.3V CPU & LOGIC SUPPLY

Note: Please follow layout and grounding guidelines in the LM2670S datasheet.



Note: For heatsinking, connect LM2937ES tab to approx. 1 sq. in. of copper plane.

2.5V DDR SDRAM SUPPLY

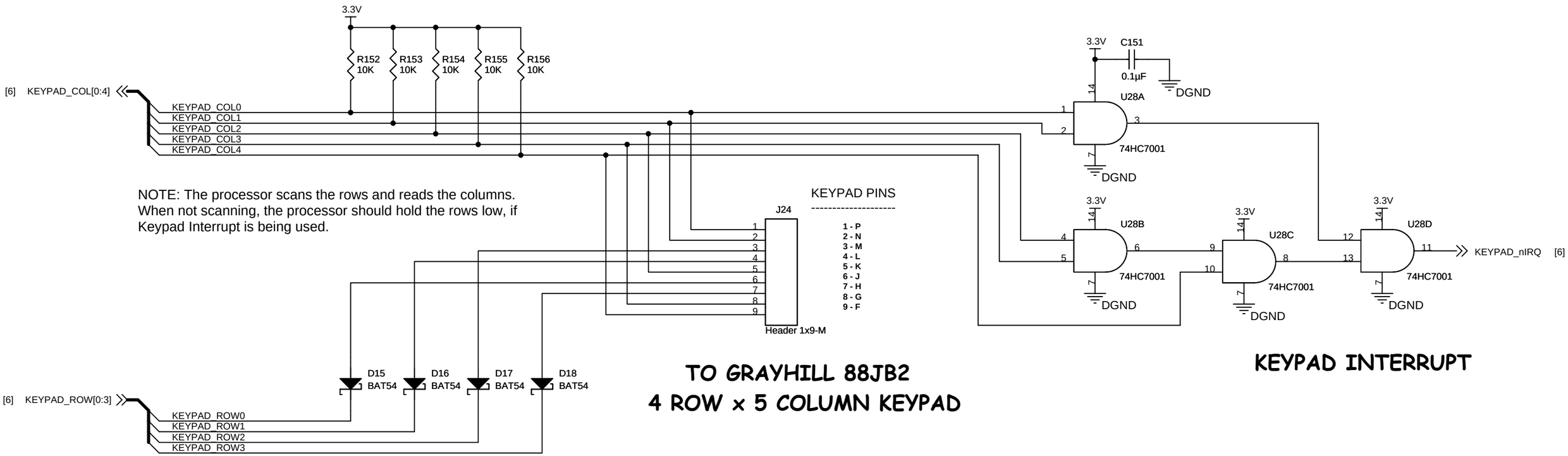


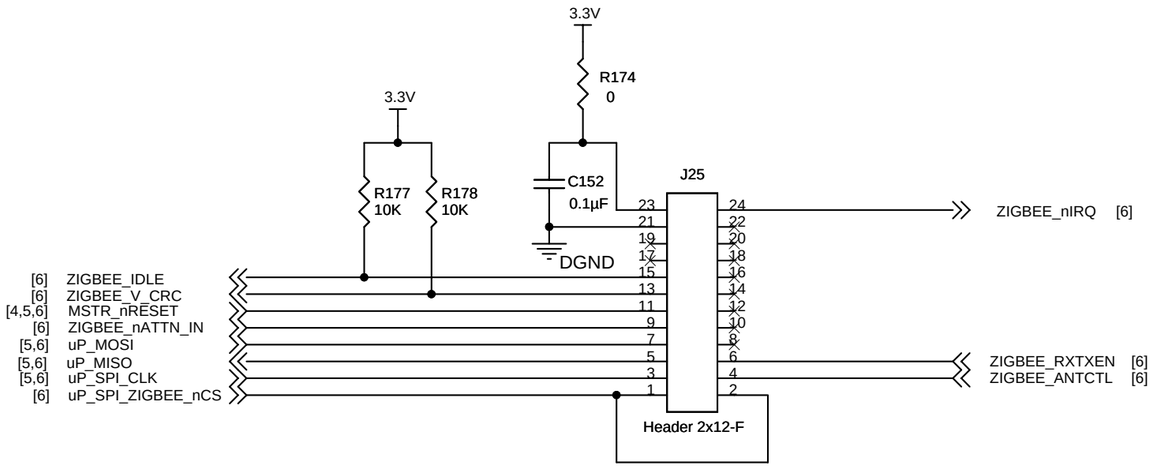
Note: For heatsinking, connect LM3981ES tab to approx. 1 sq. in. of copper plane.

1.5V CORE SUPPLY

SIZE	DATE	DRAWING NO.	REV
B	5-15-06	117E04	P4
	SCALE: NO SCALE	SHEET 7 OF 10	

8 - KEYPAD & ZIGBEE INTERFACES





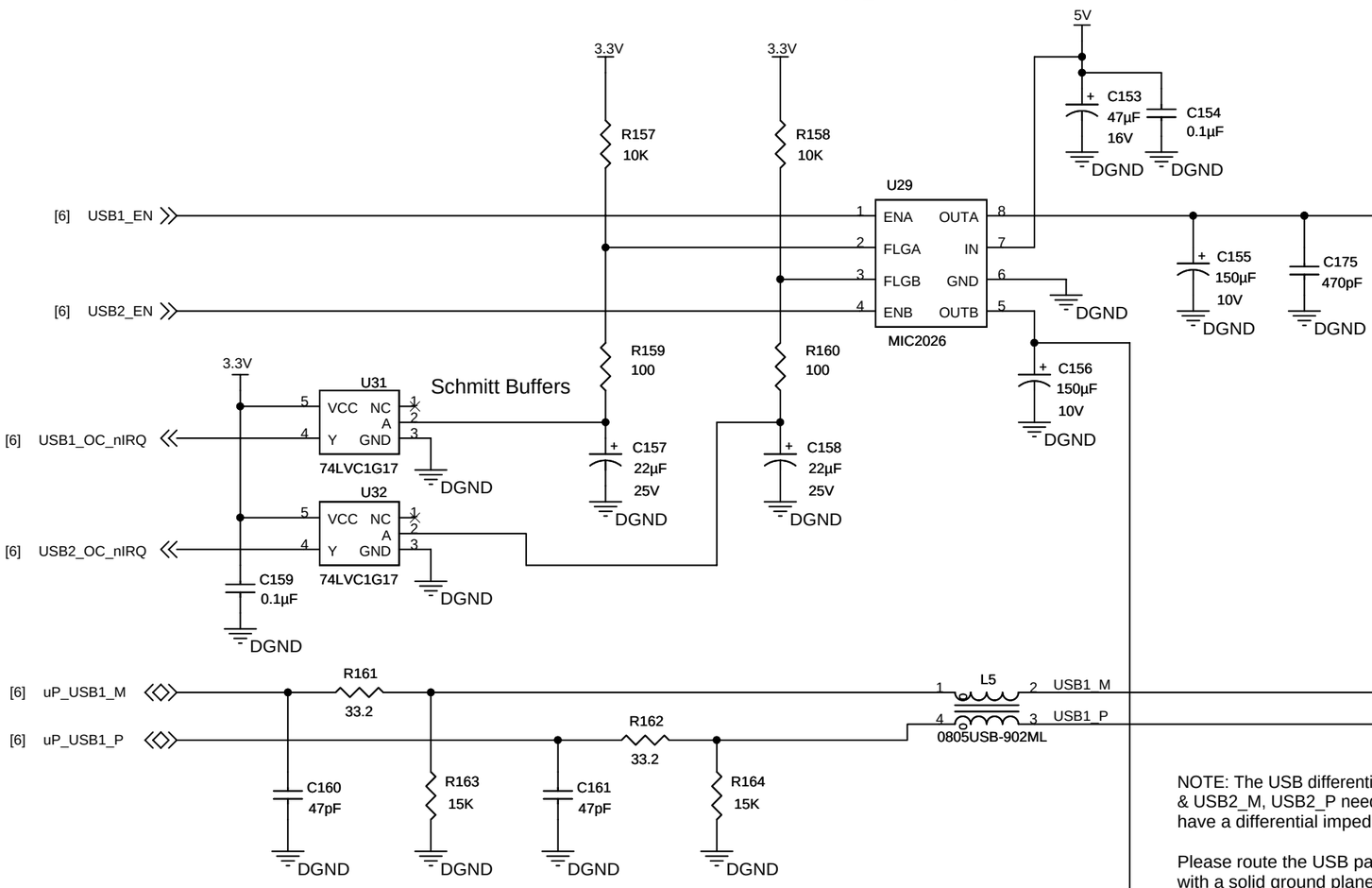
TO FREESCALE MC13192U
ZIGBEE TRANSCEIVER MODULE

SIZE	DATE	DRAWING NO.	REV
B	5-15-06	117E04	P4

SCALE: NO SCALE | SHEET 8 OF 10

9 - USB HOST INTERFACES

USB PORT POWER SWITCH



NOTE: The USB differential pairs USB1_M, USB1_P, & USB2_M, USB2_P need to be routed such that they have a differential impedance of 90 ohms.

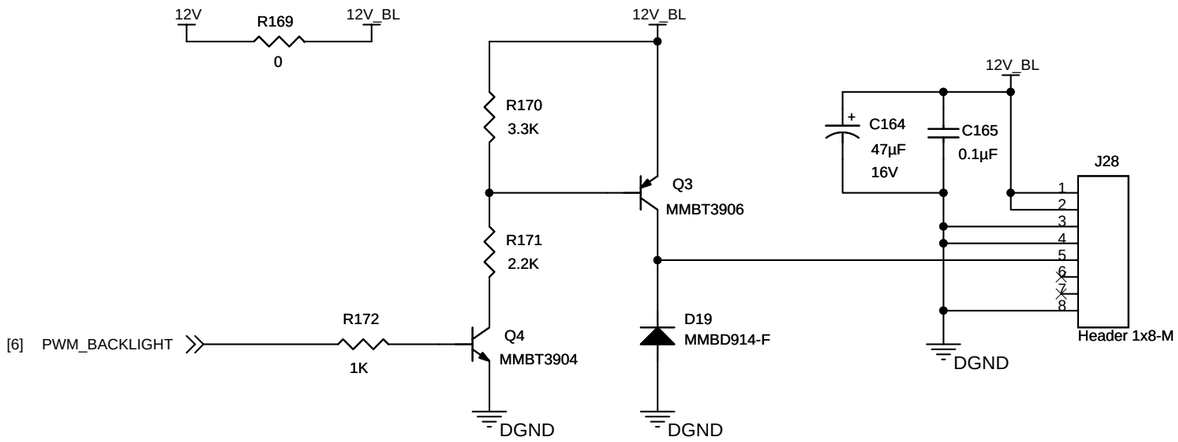
Please route the USB pairs on the top signal layer with a solid ground plane underneath.

BARCODE SCANNER PORT (EXTERNALLY ACCESSIBLE)

MAG CARD / SMART CARD PORT (INTERNALLY ACCESSIBLE)

SIZE	DATE	DRAWING NO.	REV
B	5-15-06	117E04	P4
	SCALE: NO SCALE	SHEET 9 OF 10	

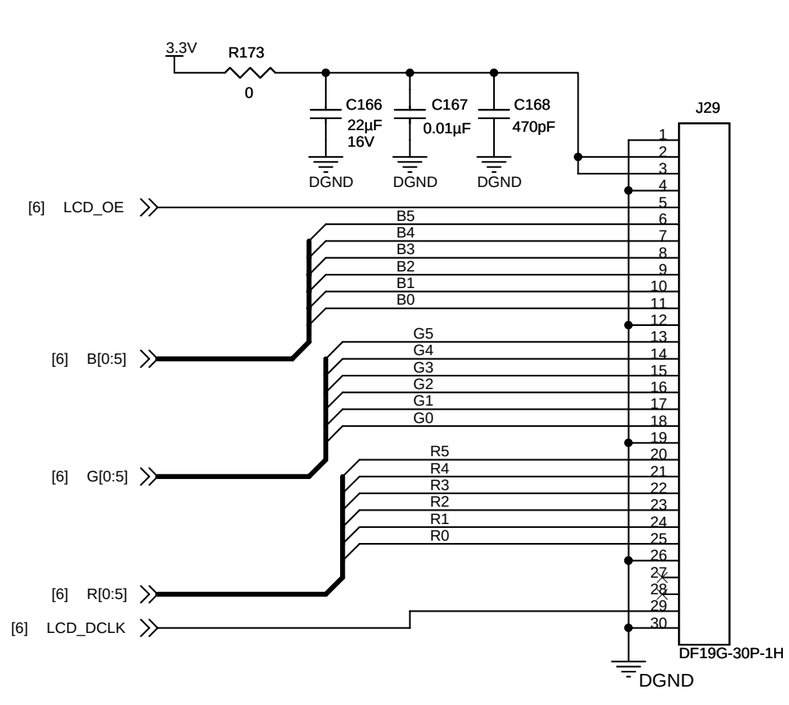
10 - LCD INTERFACE



PWM LEVEL SHIFT

POWER & PWM BRIGHTNESS CONTROL FOR ERG 8mA23003 BACKLIGHT INVERTER

NOTE: The "C" Jumper needs to be removed from the ERG 8mA23003 Board, to enable the Backlight PWM Control.



INTERFACE TO SHARP LQ084S3DG01 8.4" TFT SVGA LCD

SIZE	DATE	DRAWING NO.	REV
B	5-15-06	117E04	P4
	SCALE: NO SCALE	SHEET 10 OF 10	