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Notes:
- All components and board processes are to be ROHS compliant
- All connectors and headers are denoted Jx/Px and are 2.54mm pitch unless otherwise stated
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin Jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

3 Different test points used in design:
- TPVx - Through Hole Pad small
- TPx - Through Hole Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)
- TPX - Surface Mount Wire Loop

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS
OpenSDA Interface
CMOS FLASH Memory 64M-BIT

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Designer: Drawn by: Approved:

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ICAP Classification: CP: IUO: PUBI:

X-S32K148EVB-Q144

Date: Monday, August 07, 2017
Sheet 7 of 11