



MPC5604E -64 LQFP Customer Evaluation Board

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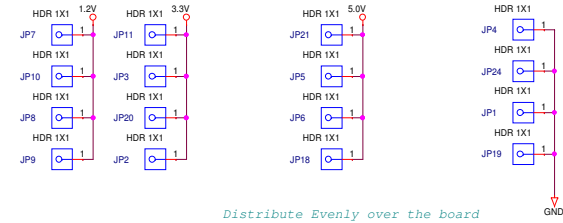
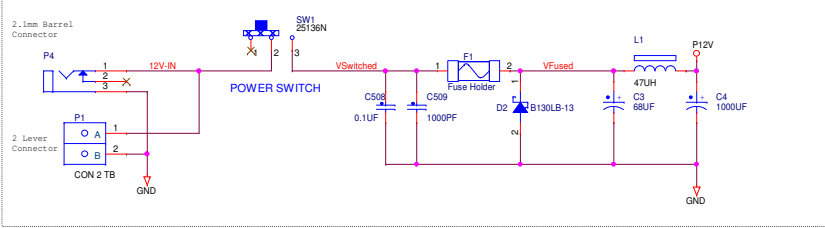
Revisions

Rev	Description	Date	Designer
X1	Initial Draft	03/04/2011	Shanu Gupta
A	Release to A085	07/04/2011	Shanu Gupta /Antony
A1	At JTAG interface : DNP R501 Populate R500	24/05/2011	Shanu Gupta /Antony

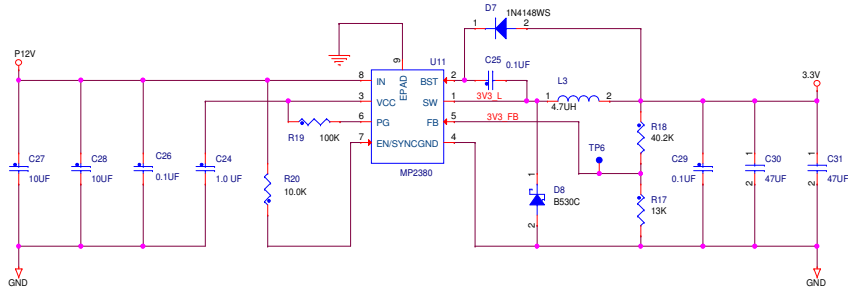
		Microcontroller Solutions Group 6501 William Cannon Drive West Austin, TX 78758-6598	
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Designer: Shanu Gupta	Drawing Title: MPC5604-EVB	ICAP Classification:	FOP: FLUQ: PUBI: X
Drawn by: Shanu Gupta	Page Title: TITLE PAGE	Size C	Document Number SCH-27073 PDF: SPF-27073
Approved:	Date: Wednesday, October 12, 2011	Sheet 1 of 13	Rev A1



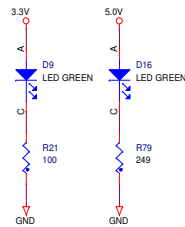
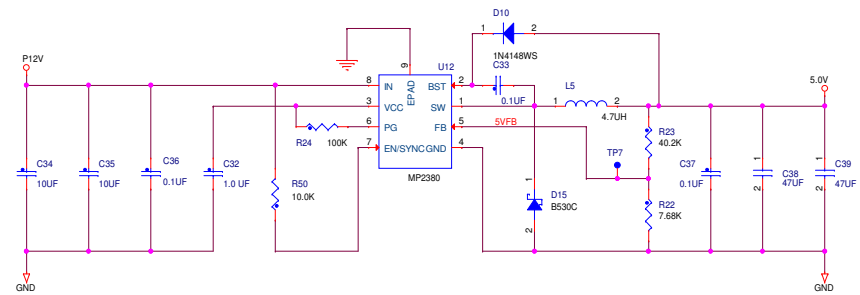
Power supply input and filter



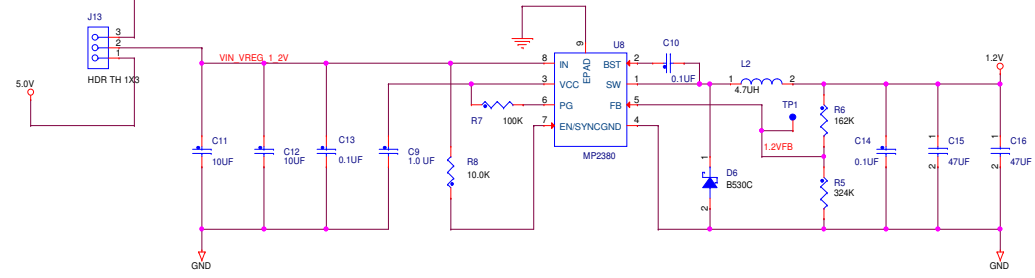
Power Supply 3.3V



Power Supply 5.0 V



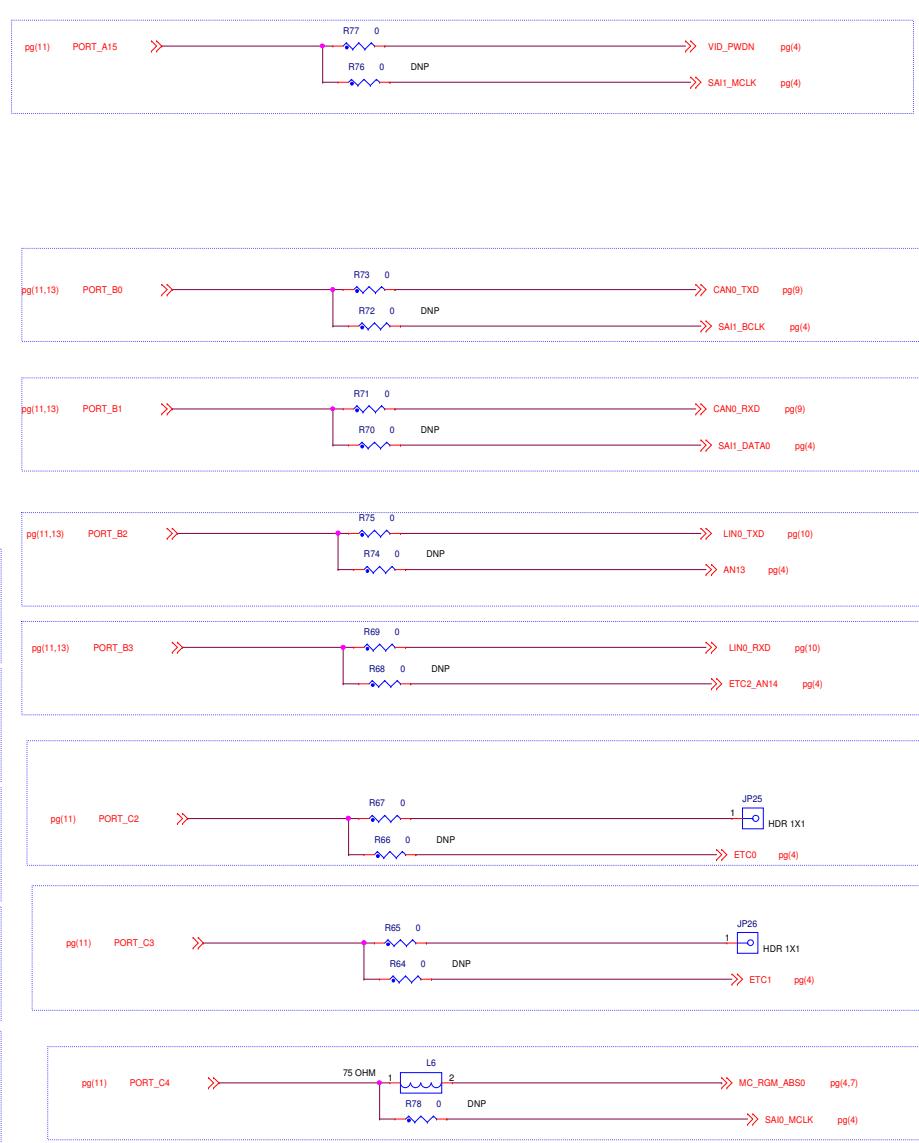
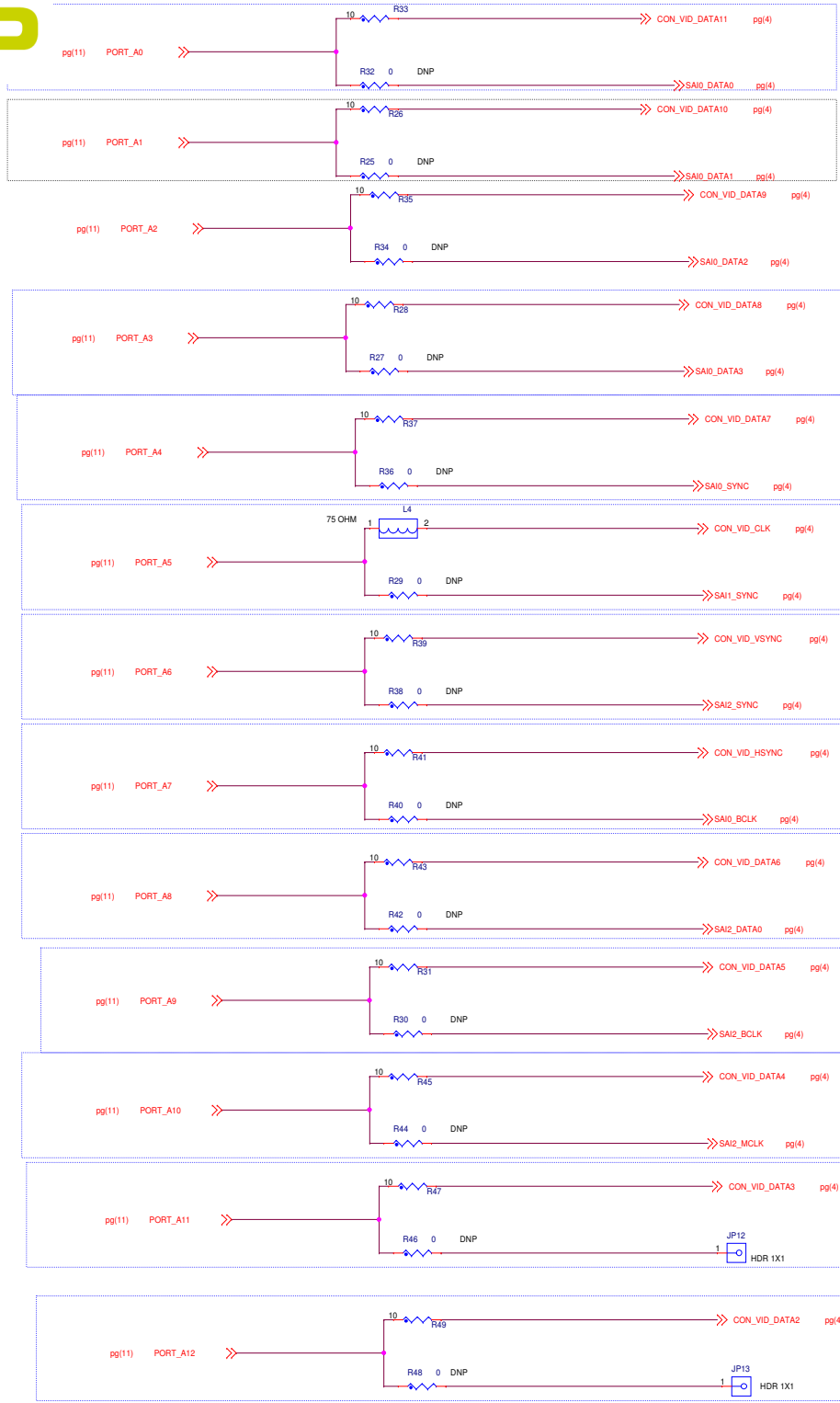
Power Supply 1.2V



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Page Title: **POWER SECTION**

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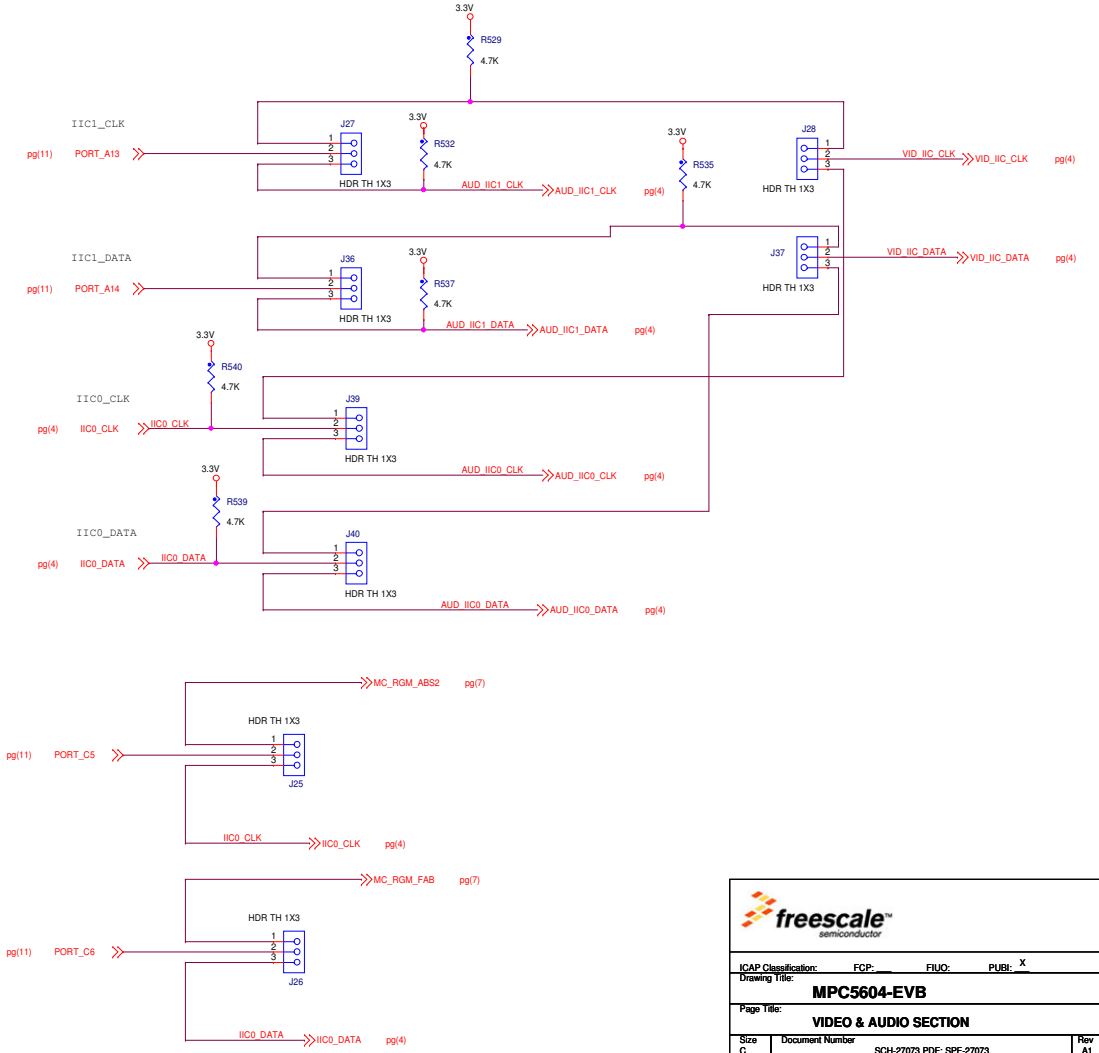
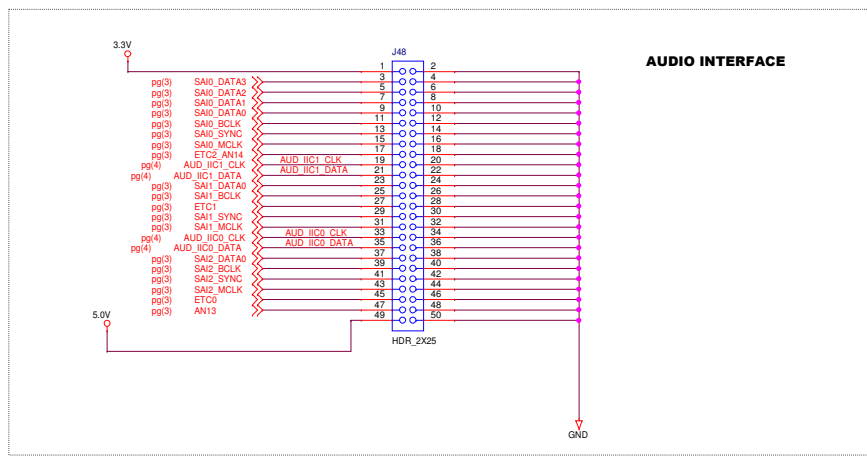
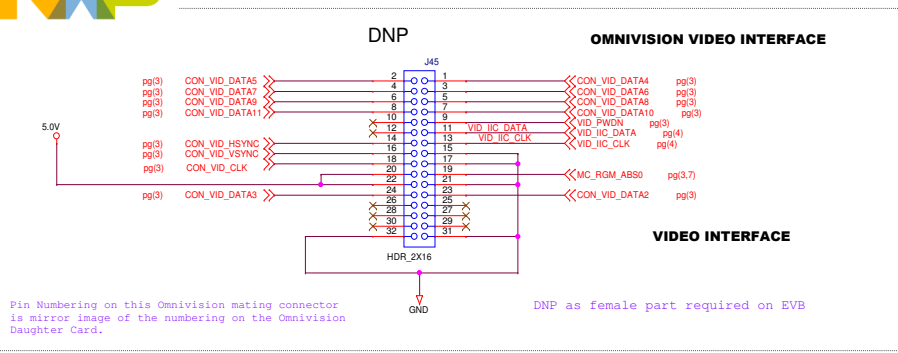


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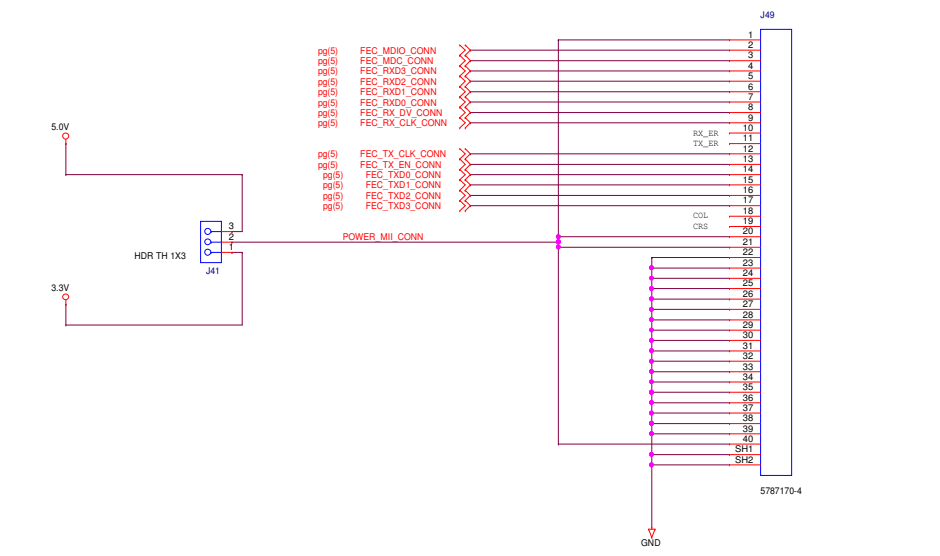
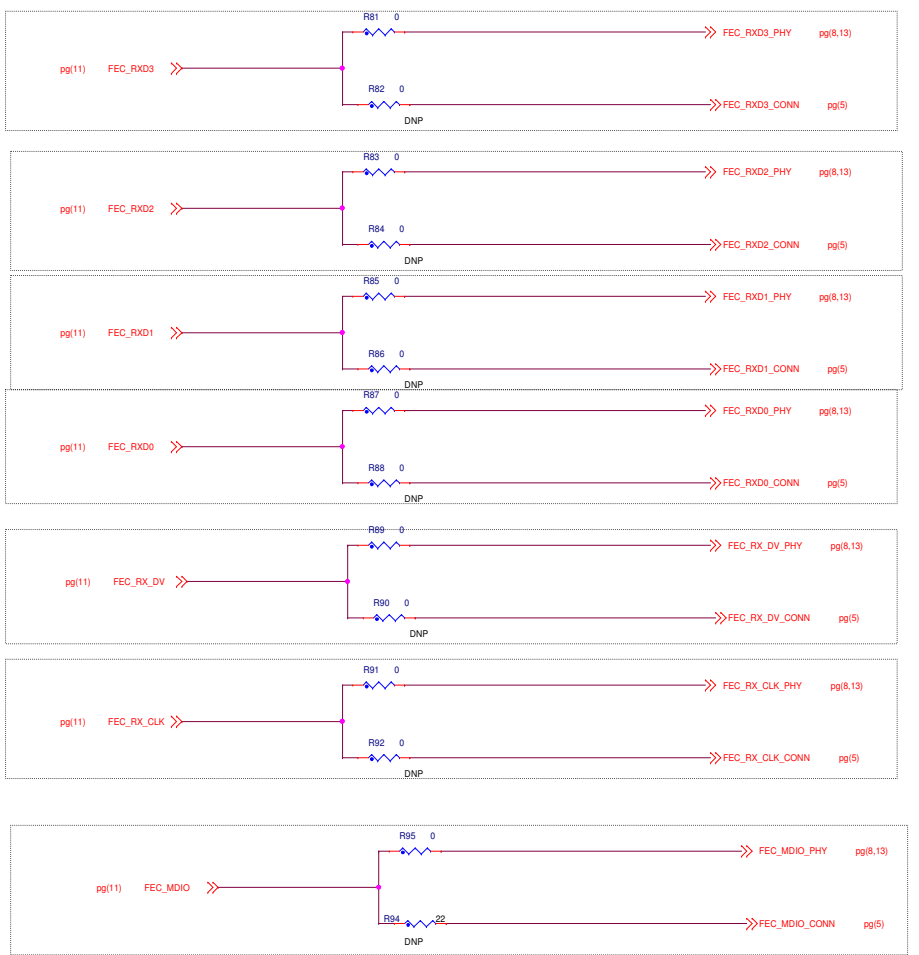
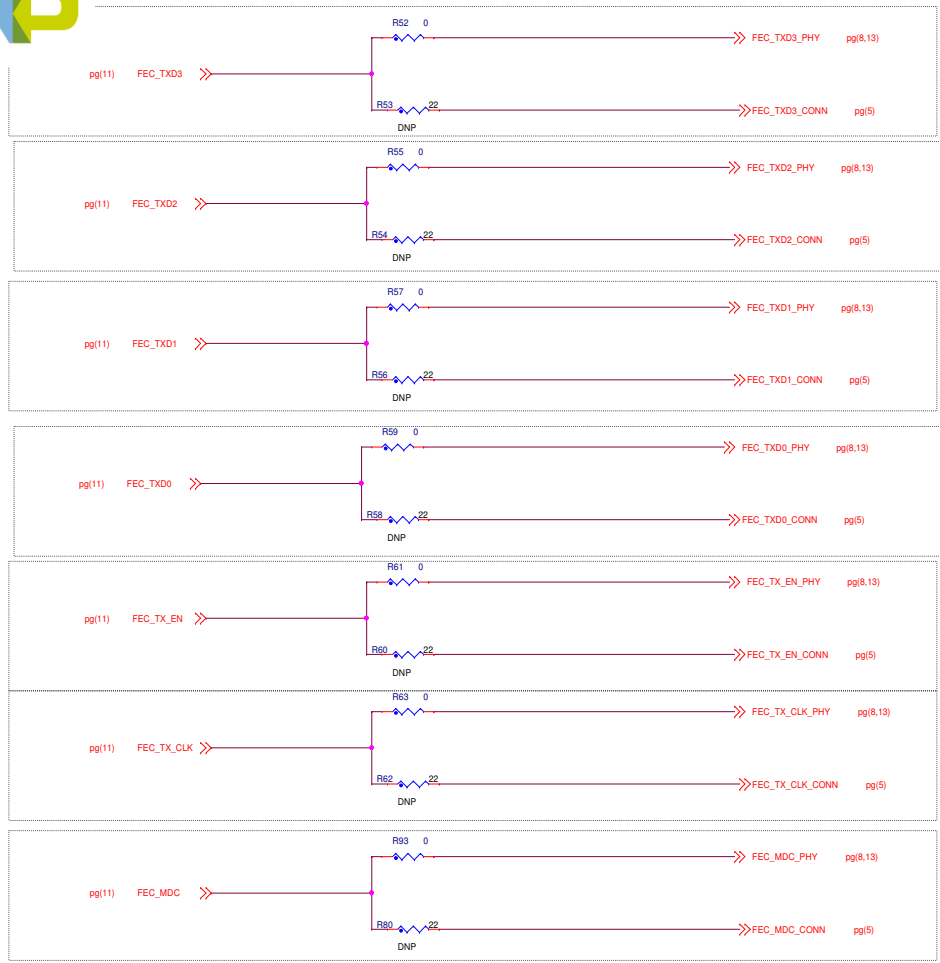
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Page Title: **RESISTOR MUX**

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VIDEO & AUDIO SECTION			
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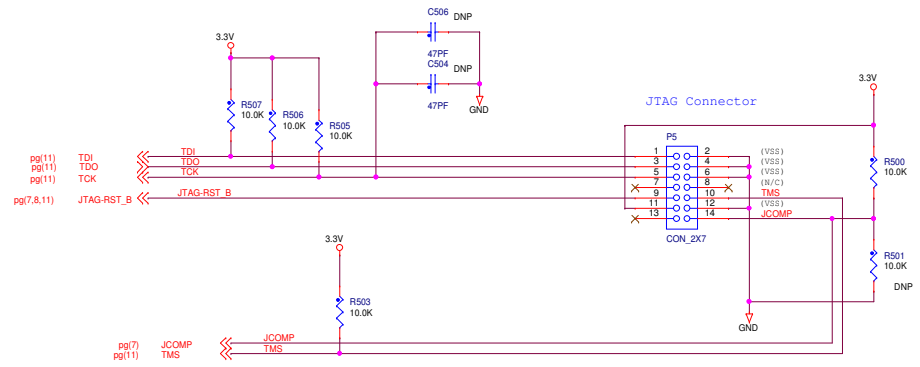
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JTAG INTERFACE

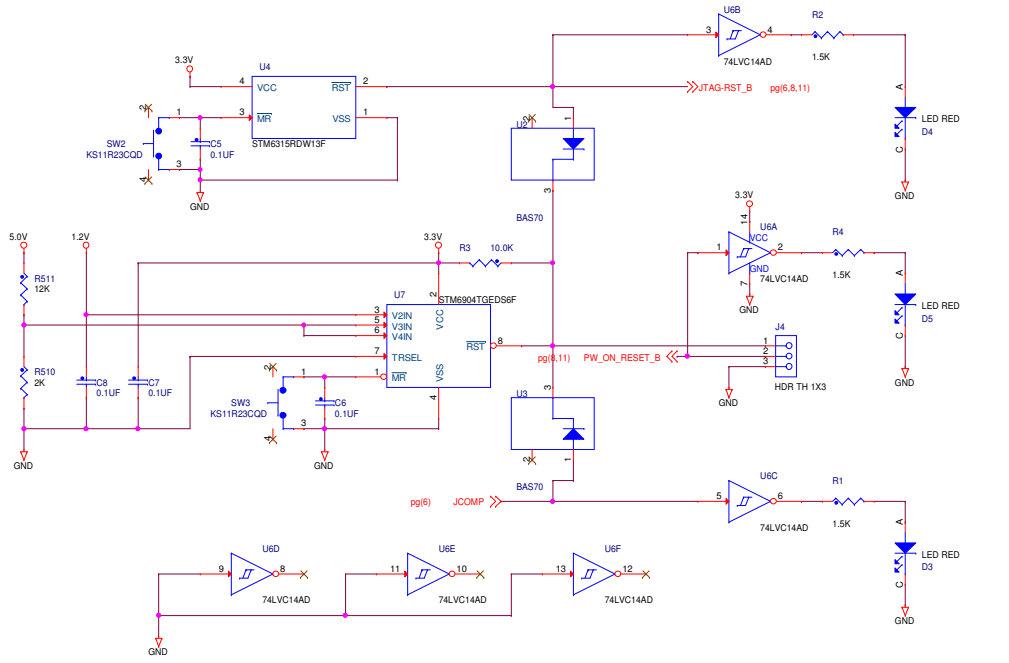
Place CAPS as close to connector pins as possible but do NOT fit caps at board assembly.



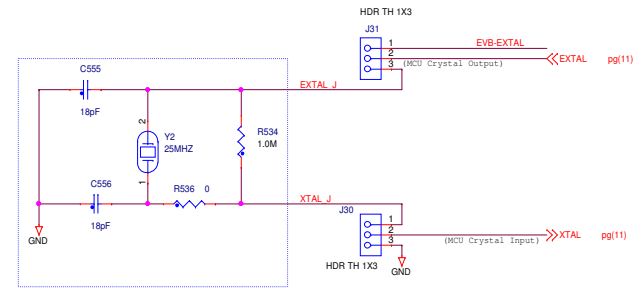


REMOVE XTAL jumper when driving EXTAL from Oscillator Module or External Source

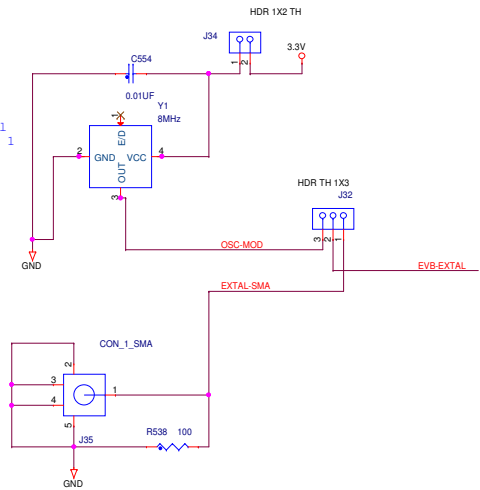
Power On Reset



Clock Circuit

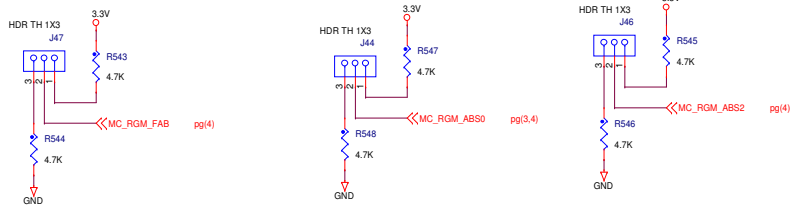


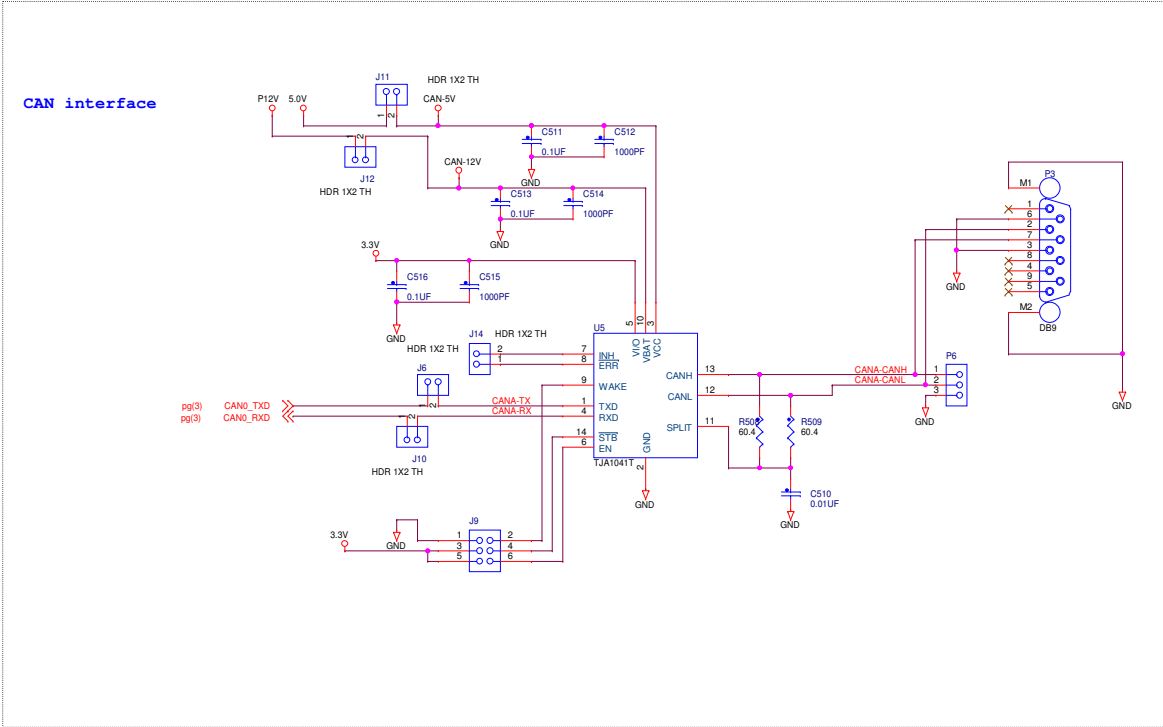
Note - Internal Pull-Up on Pin 1

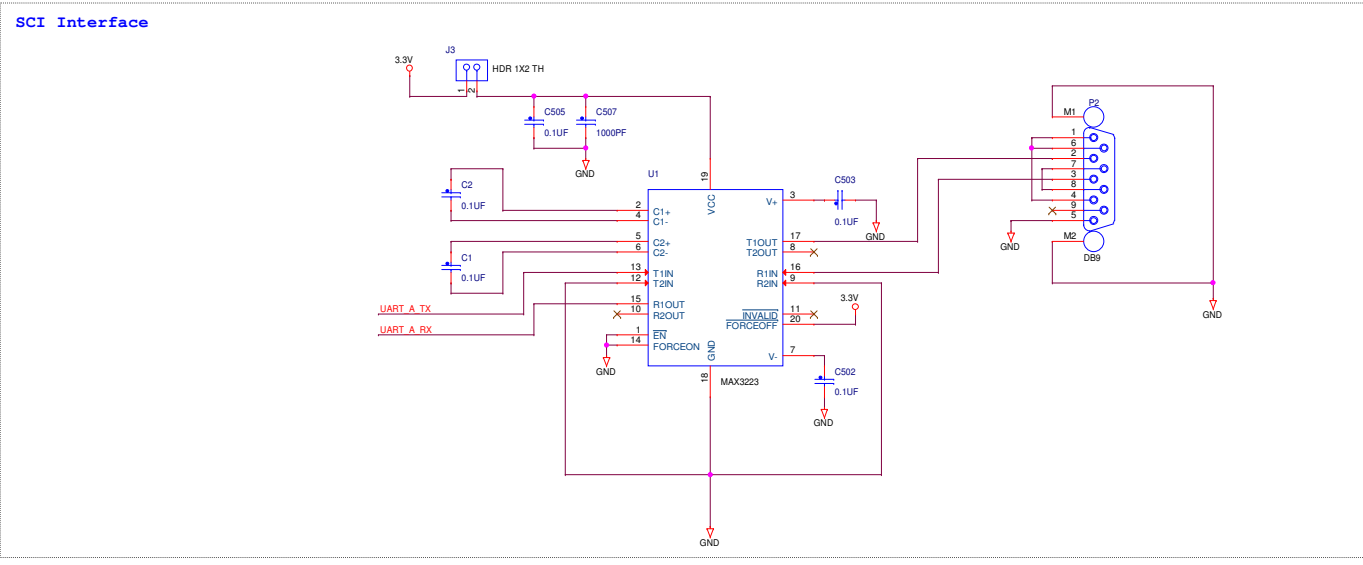
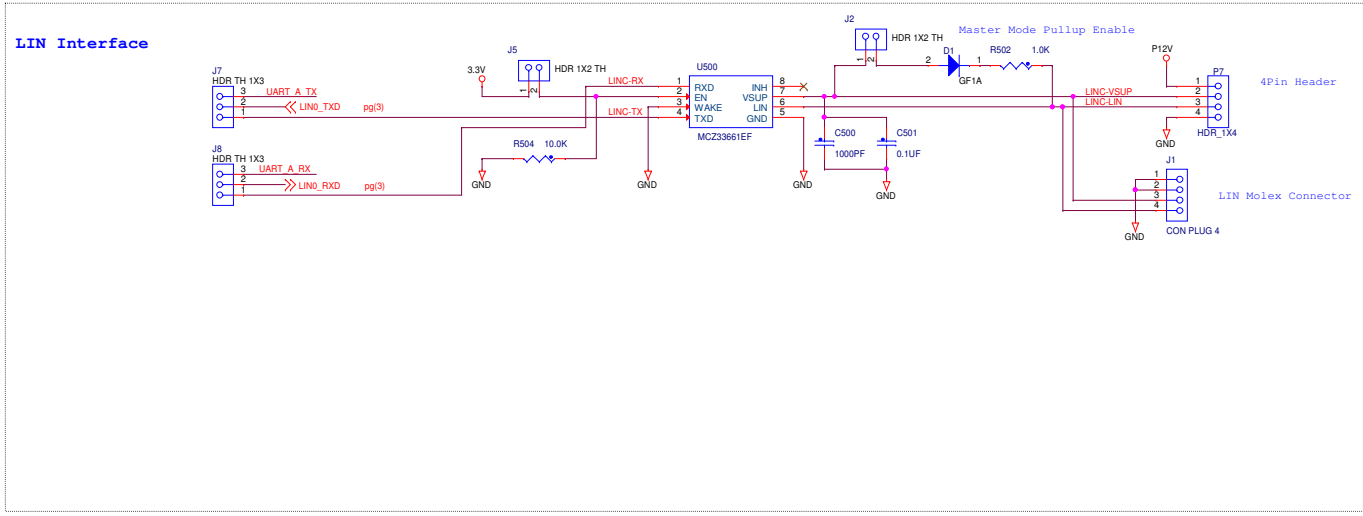


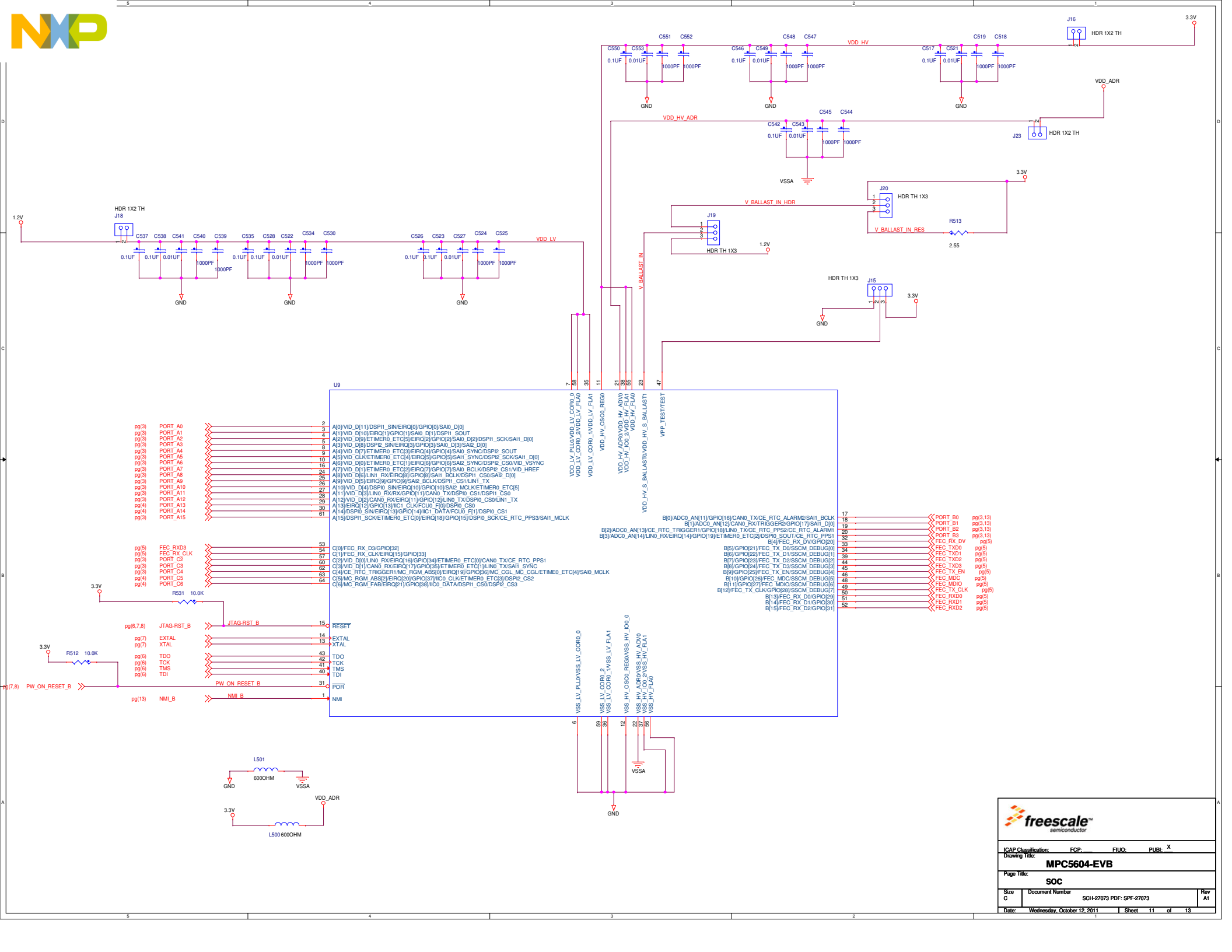
STRAIGHT SMA CONNECTOR , PLACE NEAR TO SOC

Boot Config









pg(3) PORT_A0	2	A[0]VID_D[11]DSP1_SIN/EIRQ[0]GPIO[0]SA0_D[0]
pg(3) PORT_A1	3	A[1]VID_D[10]EIRQ[1]GPIO[1]SA0_D[1]DSP1_SOUT
pg(3) PORT_A2	4	A[2]VID_D[9]ETIMER0_ETC[5]EIRQ[2]GPIO[2]SA0_D[2]DSP1_SCK/SA1_D[0]
pg(3) PORT_A3	5	A[3]VID_D[8]DSP2_SIN/EIRQ[3]GPIO[3]SA0_D[3]SA2_D[0]
pg(3) PORT_A4	6	A[4]VID_D[7]ETIMER0_ETC[3]EIRQ[4]GPIO[4]SA0_SYNC_DSP2_SOUT
pg(3) PORT_A5	7	A[5]VID_CLK/ETIMER0_ETC[4]EIRQ[5]GPIO[5]SA1_SYNC_DSP2_SCK/SA1_D[0]
pg(3) PORT_A6	8	A[6]VID_D[0]ETIMER0_ETC[1]EIRQ[6]GPIO[6]SA2_SYNC_DSP2_CS0/VID_VSYNC
pg(3) PORT_A7	9	A[7]VID_D[1]ETIMER0_ETC[2]EIRQ[7]GPIO[7]SA0_BCLK_DSP2_CS1/VID_HREF
pg(3) PORT_A8	10	A[8]VID_D[5]LINA_RX/EIRQ[8]GPIO[8]SA1_BCLK_DSP1_CS0/SA2_D[0]
pg(3) PORT_A9	11	A[9]VID_D[5]EIRQ[9]GPIO[9]SA2_BCLK_DSP1_CS1/LINA_TX
pg(3) PORT_A10	12	A[10]VID_D[4]DSP0_SIN/EIRQ[10]GPIO[10]SA2_MCLK/ETIMER0_ETC[5]
pg(3) PORT_A11	13	A[11]VID_D[5]LINA_RX/EIRQ[11]GPIO[11]CAN0_TX/DSP0_CS1/DSP1_CS0
pg(3) PORT_A12	14	A[12]VID_D[2]CAN0_RX/EIRQ[12]GPIO[12]LINA_TX/DSP0_CS0/LINA_TX
pg(3) PORT_A13	15	A[13]EIRQ[12]GPIO[13]IC1_CLK/FCU0_F[0]DSP0_CS0
pg(4) PORT_A14	16	A[14]DSP0_SIN/EIRQ[13]GPIO[14]IC1_DATA/FCU0_F[1]DSP0_CS1
pg(4) PORT_A15	17	A[15]DSP1_SCK/ETIMER0_ETC[0]EIRQ[18]GPIO[15]DSP0_SCK/CE_RTC_PPS3/SA1_MCLK
pg(5) FEC_RXD3	53	B[0]FEC_RX_D3/GPIO[32]
pg(5) FEC_RX_CLK	54	C[1]FEC_RX_CLK/EIRQ[15]GPIO[33]
pg(3) PORT_C2	57	C[2]VID_D[0]LINA_RX/EIRQ[16]GPIO[34]ETIMER0_ETC[0]CAN0_TX/CE_RTC_PPS1
pg(3) PORT_C3	60	C[3]VID_D[1]CAN0_RX/EIRQ[17]GPIO[35]ETIMER0_ETC[1]LINA_TX/SA1_SYNC
pg(3) PORT_C4	62	C[4]CE_RTC_TRIGGER1/MC_RGM_ABS[0]EIRQ[19]GPIO[36]MC_CGL_MCLK/ETIMER0_ETC[4]SA0_MCLK
pg(4) PORT_C5	63	C[5]MC_RGM_ABS[2]EIRQ[20]GPIO[37]IC0_CLK/ETIMER0_ETC[3]DSP2_CS2
pg(4) PORT_C6	64	C[6]MC_RGM_FAB/EIRQ[21]GPIO[38]IC0_DATA/DSP1_CS0/DSP2_CS3
pg(5) JTAG_RST_B	15	B[0]ADCO_AN[11]GPIO[16]CAN0_TX/CE_RTC_ALARM2/SA1_BCLK
pg(7) XTAL	14	B[1]ADCO_AN[12]CAN0_RX/TRIGGER2/GPIO[17]SA1_D[0]
pg(6) TDO	42	B[2]ADCO_AN[13]CE_RTC_TRIGGER1/GPIO[18]LINA_TX/CE_RTC_PPS/CE_RTC_ALARM1
pg(6) TCK	41	B[3]ADCO_AN[14]LINA_RX/EIRQ[14]GPIO[19]ETIMER0_ETC[2]DSP0_SOUT/CE_RTC_PPS1
pg(6) TMS	40	B[4]FEC_RX_DIV/GPIO[20]
pg(6) TDI	39	B[5]GPIO[21]FEC_TX_D0/SSCM_DEBUG[0]
pg(13) NMI_B	1	B[6]GPIO[22]FEC_TX_D1/SSCM_DEBUG[1]
		B[7]GPIO[23]FEC_TX_D2/SSCM_DEBUG[2]
		B[8]GPIO[24]FEC_TX_D3/SSCM_DEBUG[3]
		B[9]GPIO[25]FEC_TX_EN/SSCM_DEBUG[4]
		B[10]GPIO[26]FEC_MDC/SSCM_DEBUG[5]
		B[11]GPIO[27]FEC_MDIO/SSCM_DEBUG[6]
		B[12]FEC_TX_CLK/GPIO[28]SSCM_DEBUG[7]
		B[13]FEC_RX_D0/GPIO[29]
		B[14]FEC_RX_D1/GPIO[30]
		B[15]FEC_RX_D2/GPIO[31]

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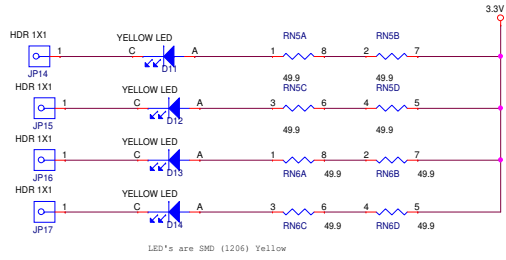
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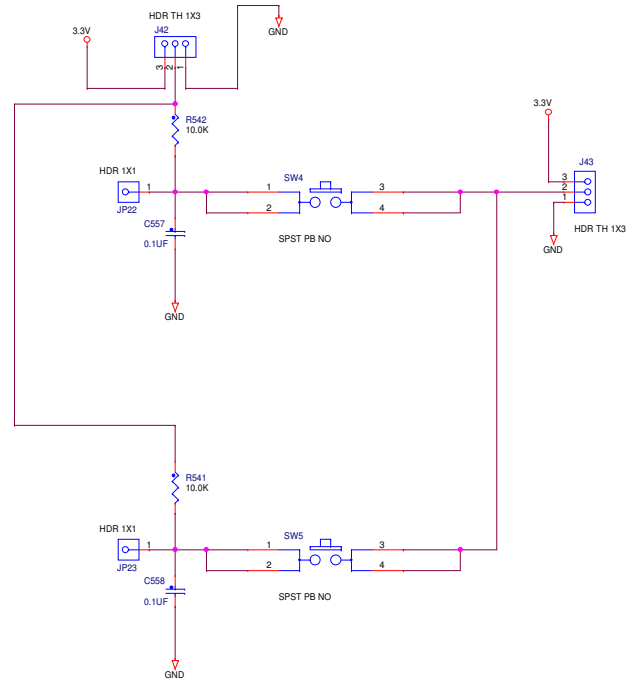
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User LEDs



User switches



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