MPC5604E -64 LQFP Customer Evaluation Board

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Revisions

Rev	Description	Date	Designer
X1	Initial Draft	03/04/2011	Shanu Gupta
A	Release to A085	07/04/2011	Shanu Gupta /Antony
A1	At JTAG interface : DNP R501 Populate R500	24/05/2011	Shanu Gupta /Antony

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Microcontroller Solutions Group

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ICAP Classification: FCP: FIUO: PUBI: X

Designer: Shanu.Gupta	Drawing Title: MPC5604-EVB		
Drawn by: Shanu.Gupta	Page Title: TITLE PAGE		
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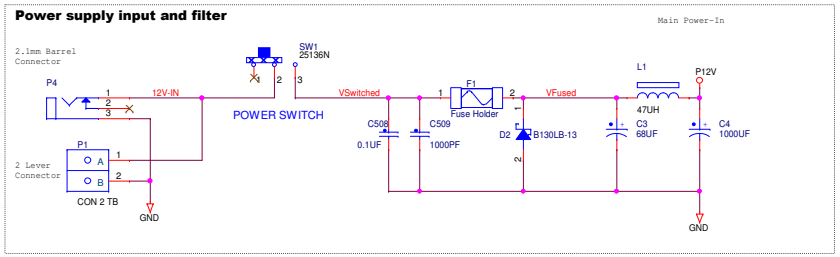
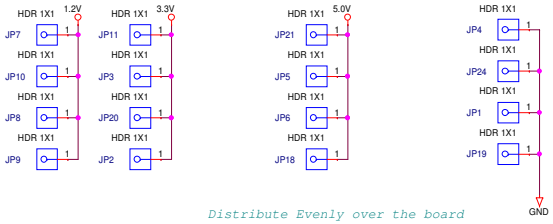
Power supply input and filter





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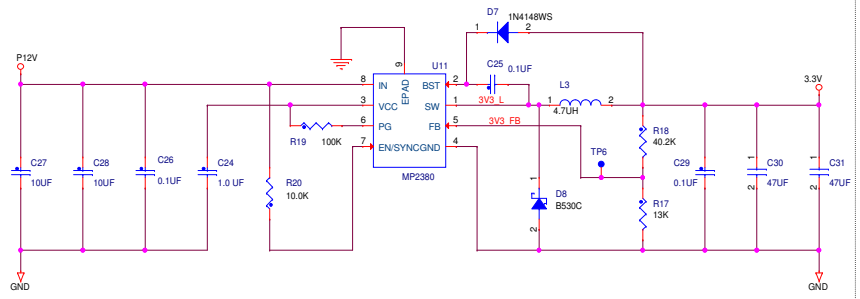
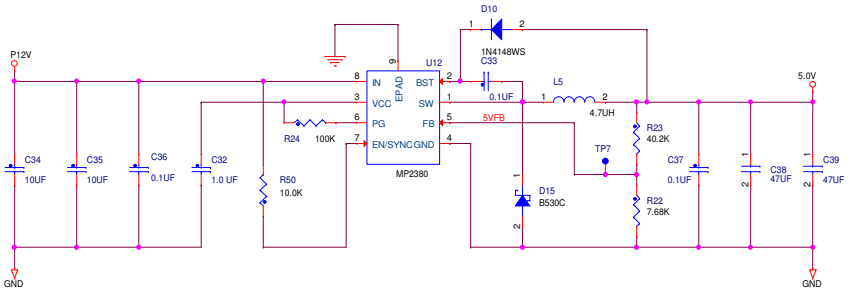
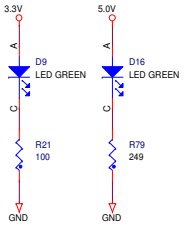


Power Supply 5.0 V





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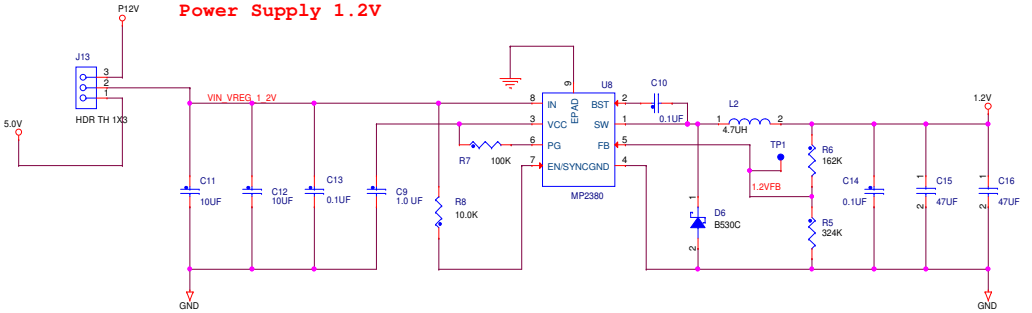

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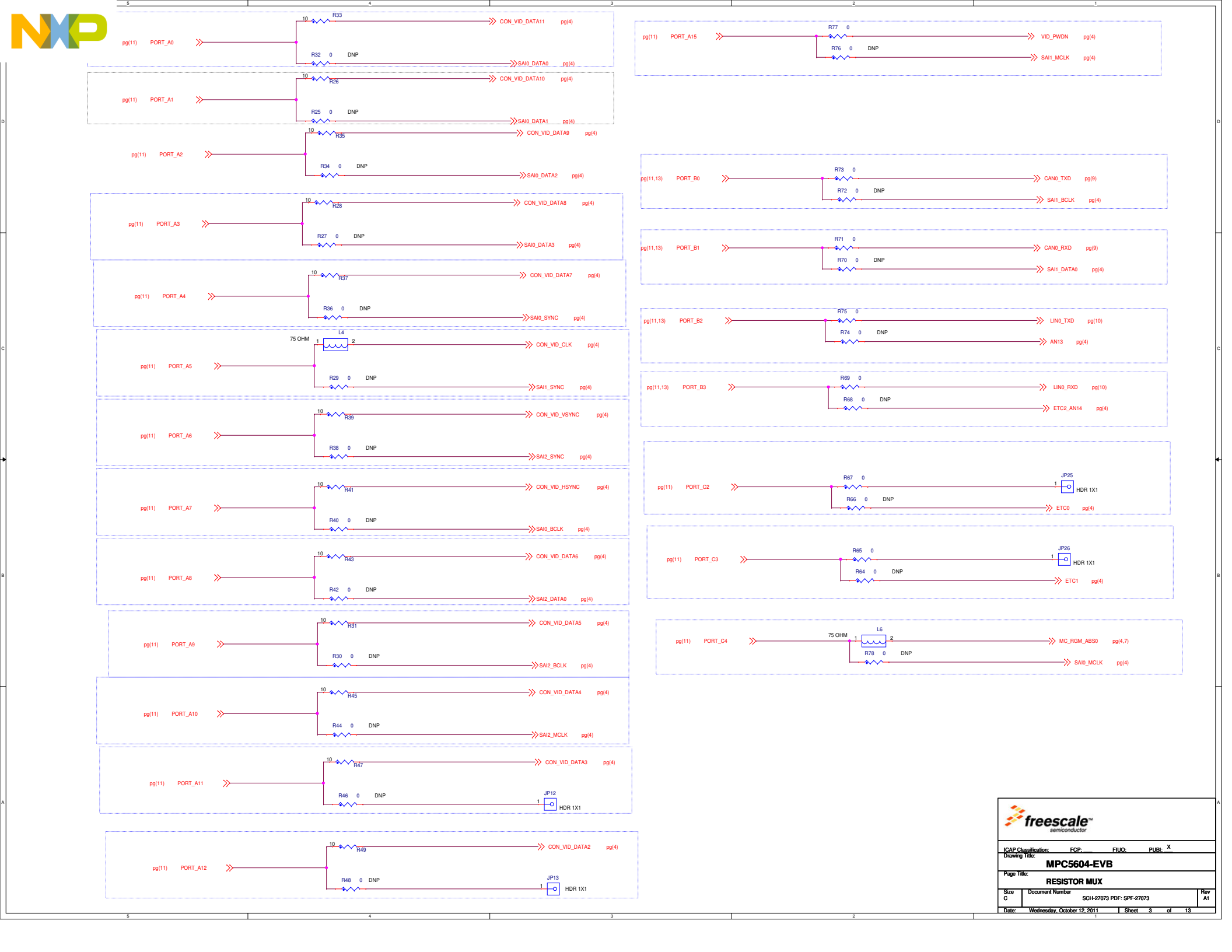
pg(11) PORT_A0
10 R33 CON_VID_DATA11 pg(4)
R32 0 DNP SAI0_DATA0 pg(4)
pg(11) PORT_A1
10 R26 CON_VID_DATA10 pg(4)
R25 0 DNP SAI0_DATA1 pg(4)
pg(11) PORT_A2
10 R35 CON_VID_DATA9 pg(4)
R34 0 DNP SAI0_DATA2 pg(4)
pg(11) PORT_A3
10 R28 CON_VID_DATA8 pg(4)
R27 0 DNP SAI0_DATA3 pg(4)
pg(11) PORT_A4
10 R37 CON_VID_DATA7 pg(4)
R36 0 DNP SAI0_SYNC pg(4)
pg(11) PORT_A5
75 OHM L4 CON_VID_CLK pg(4)
R29 0 DNP SAI1_SYNC pg(4)
pg(11) PORT_A6
10 R39 CON_VID_VSYNC pg(4)
R38 0 DNP SAI2_SYNC pg(4)
pg(11) PORT_A7
10 R41 CON_VID_HSYNC pg(4)
R40 0 DNP SAI0_BCLK pg(4)
pg(11) PORT_A8
10 R43 CON_VID_DATA6 pg(4)
R42 0 DNP SAI2_DATA0 pg(4)
pg(11) PORT_A9
10 R31 CON_VID_DATA5 pg(4)
R30 0 DNP SAI2_BCLK pg(4)
pg(11) PORT_A10
10 R45 CON_VID_DATA4 pg(4)
R44 0 DNP SAI2_MCLK pg(4)
pg(11) PORT_A11
10 R47 CON_VID_DATA3 pg(4)
R46 0 DNP JP12 HDR 1X1
pg(11) PORT_A12
10 R49 CON_VID_DATA2 pg(4)
R48 0 DNP JP13 HDR 1X1
pg(11) PORT_A15
R77 0 VID_PWDN pg(4)
R76 0 DNP SAI1_MCLK pg(4)
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R73 0 CAN0_TXD pg(9)
R72 0 DNP SAI1_BCLK pg(4)
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R71 0 CAN0_RXD pg(9)
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R75 0 LIN0_TXD pg(10)
R74 0 DNP AN13 pg(4)
pg(11,13) PORT_B3
R69 0 LIN0_RXD pg(10)
R68 0 DNP ETC2_AN14 pg(4)
pg(11) PORT_C2
R67 0 JP25 HDR 1X1
R66 0 DNP ETC0 pg(4)
pg(11) PORT_C3
R65 0 JP26 HDR 1X1
R64 0 DNP ETC1 pg(4)
pg(11) PORT_C4
75 OHM L6 MC_RGM_ABS0 pg(4,7)
R78 0 DNP SAI0_MCLK pg(4)
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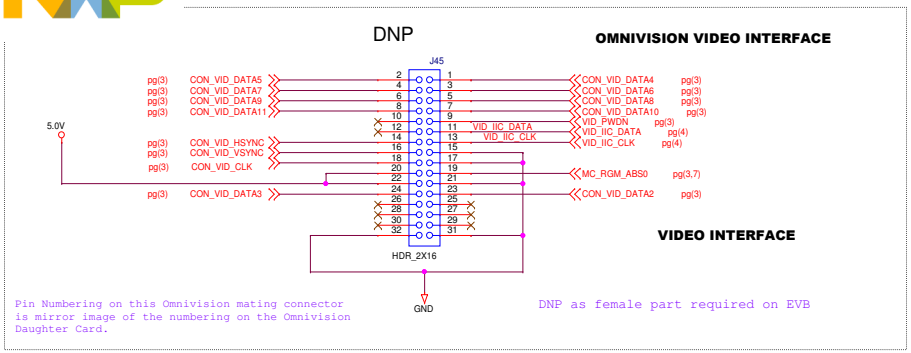

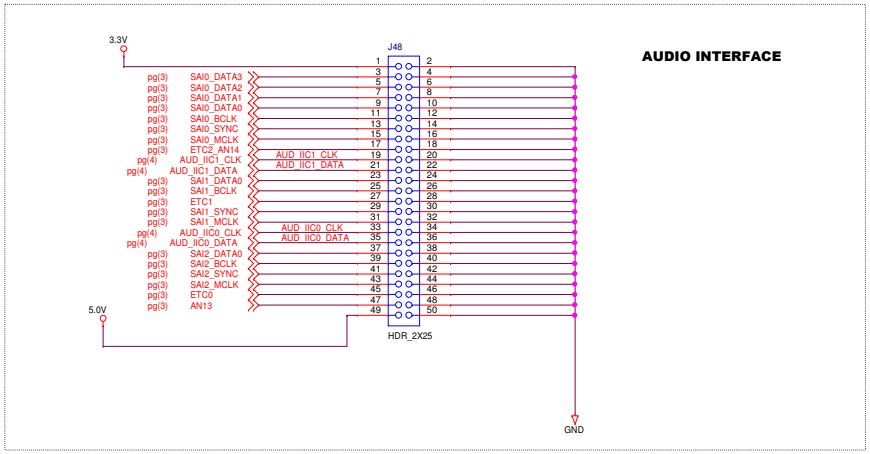

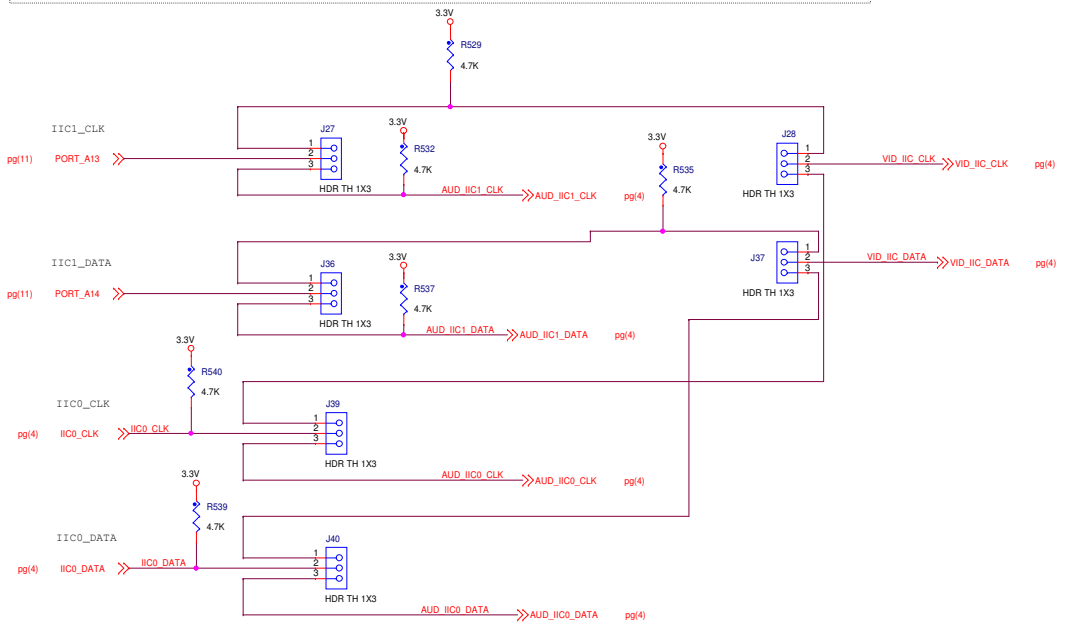

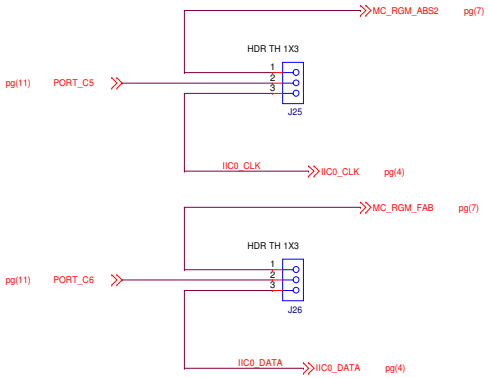

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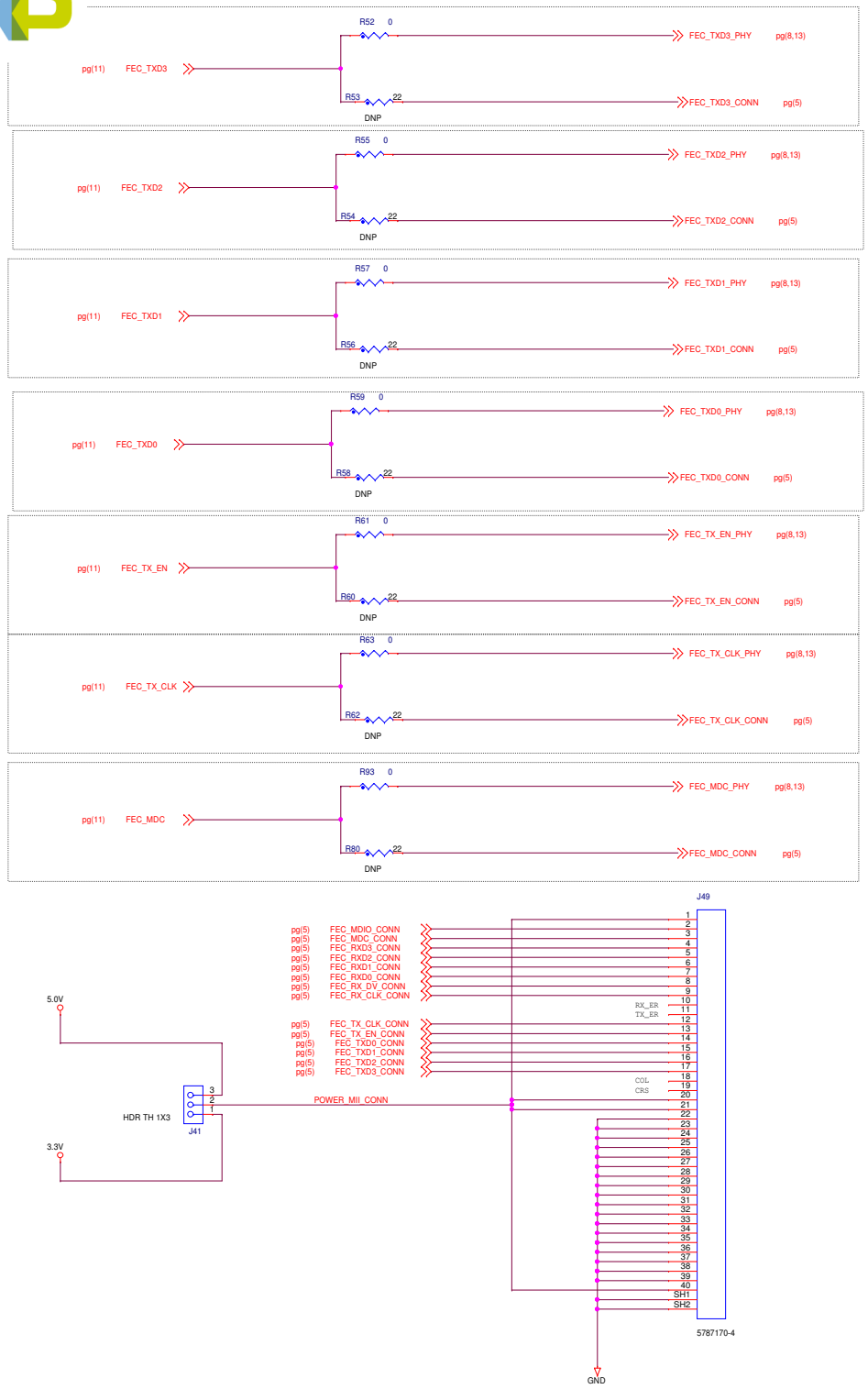

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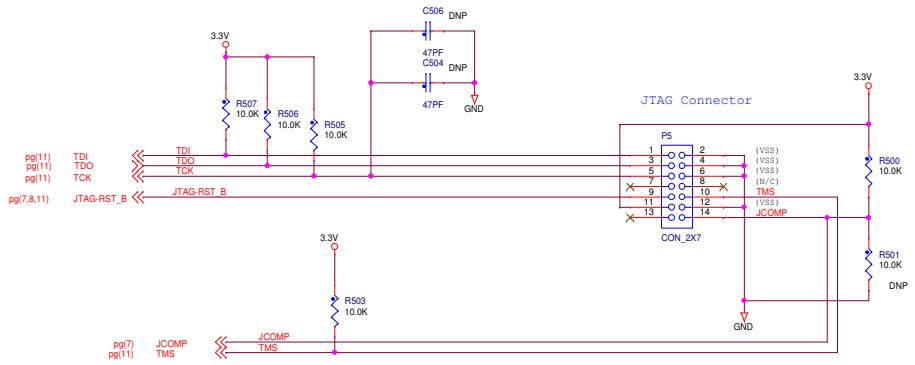
JTAG INTERFACE

Place CAPS as close to connector pins as possible but do NOT fit caps at board assembly.



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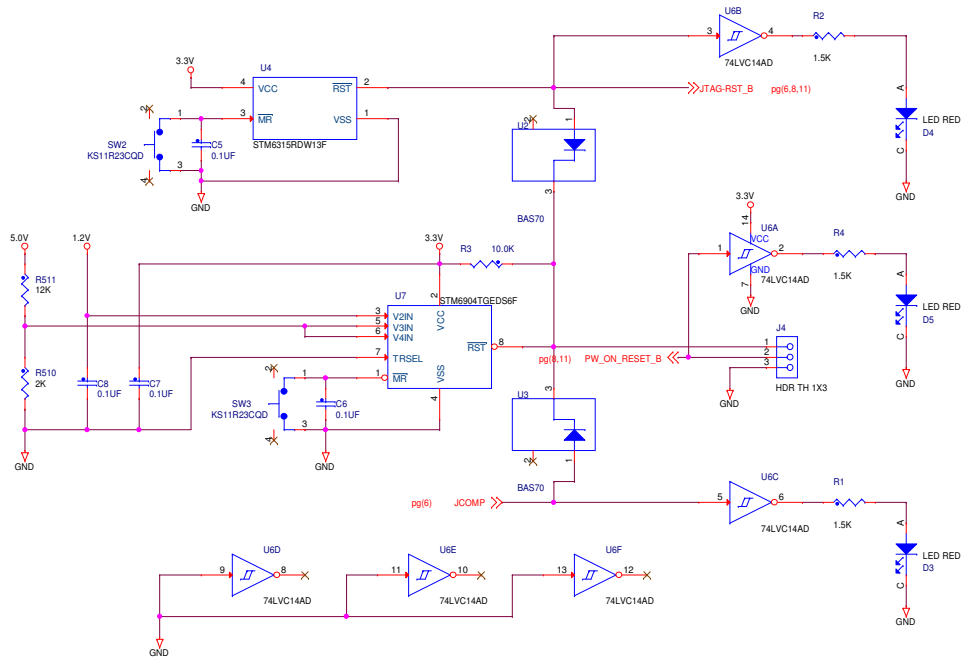
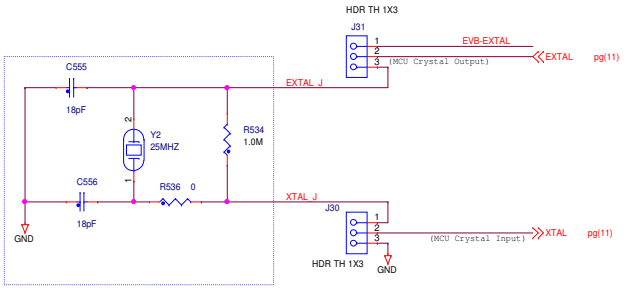
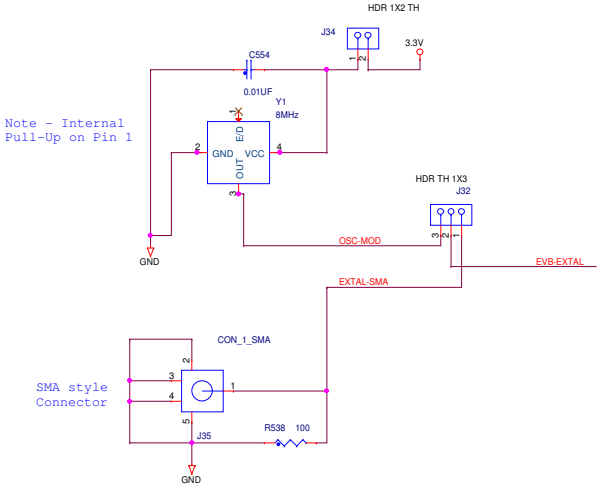
REMOVE XTAL jumper when driving EXTAL from
Oscillator Module or External Source

Power On Reset



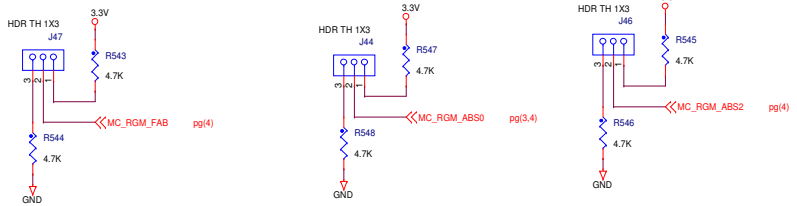
Clock Circuit





STRAIGHT SMA CONNECTOR ,PLACE NEAR TO SOC

Boot Config



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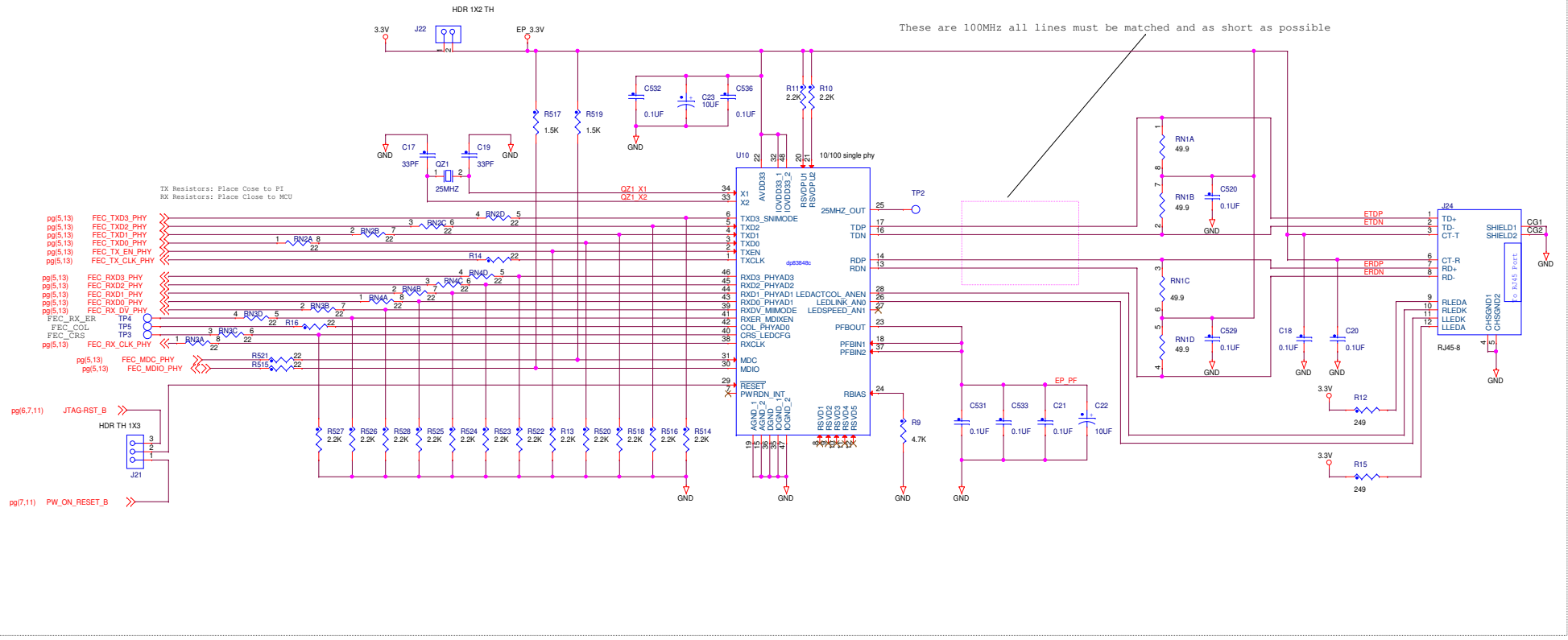
Ethernet Section



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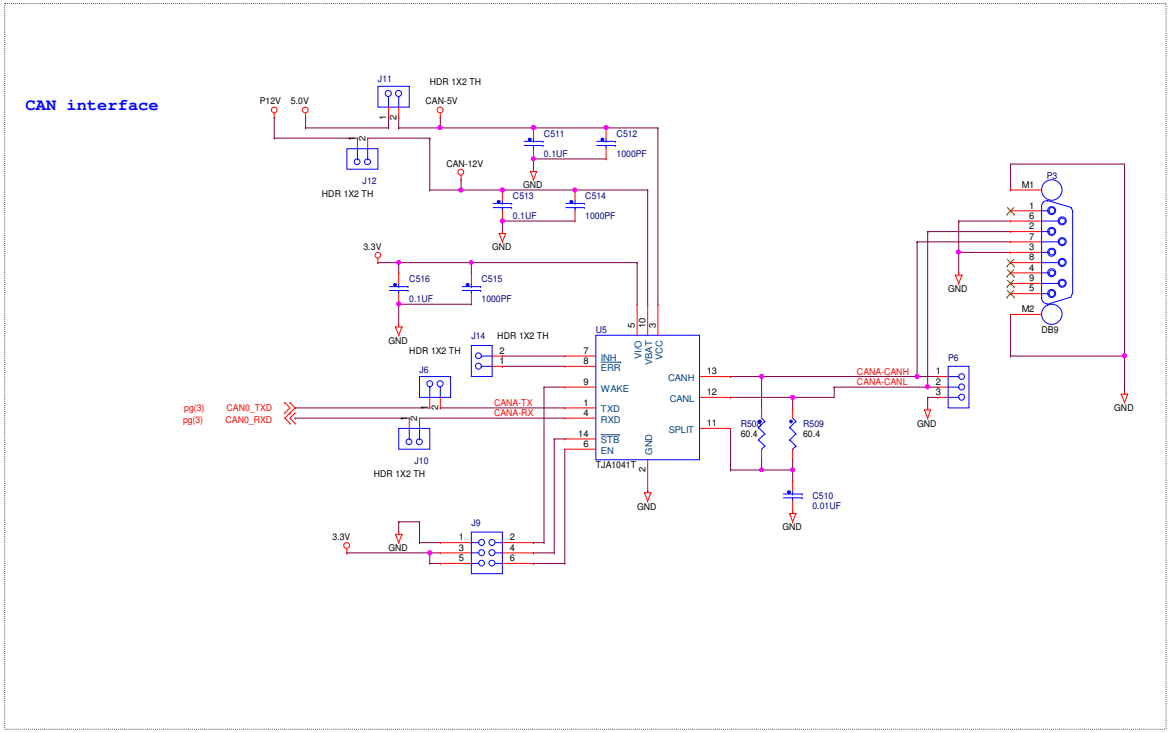
CAN interface



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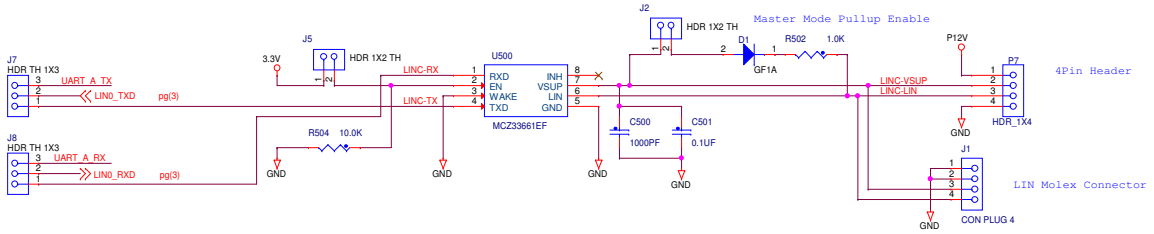
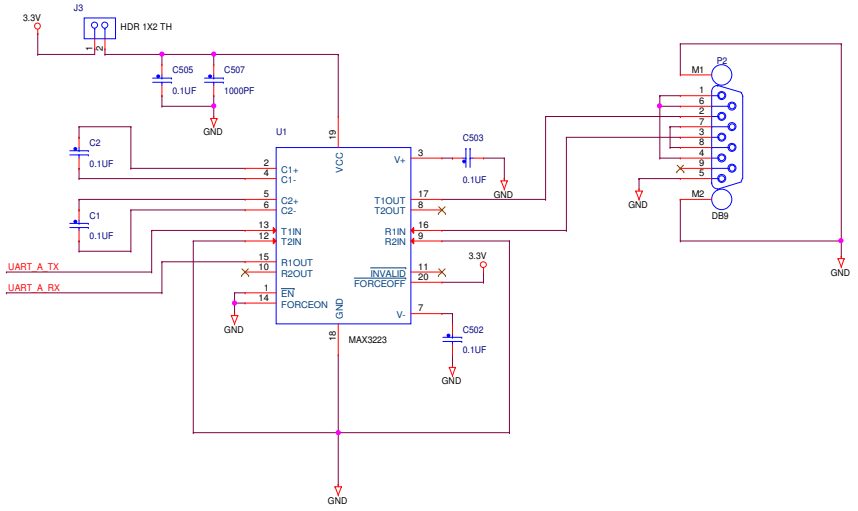
LIN Interface



SCI Interface



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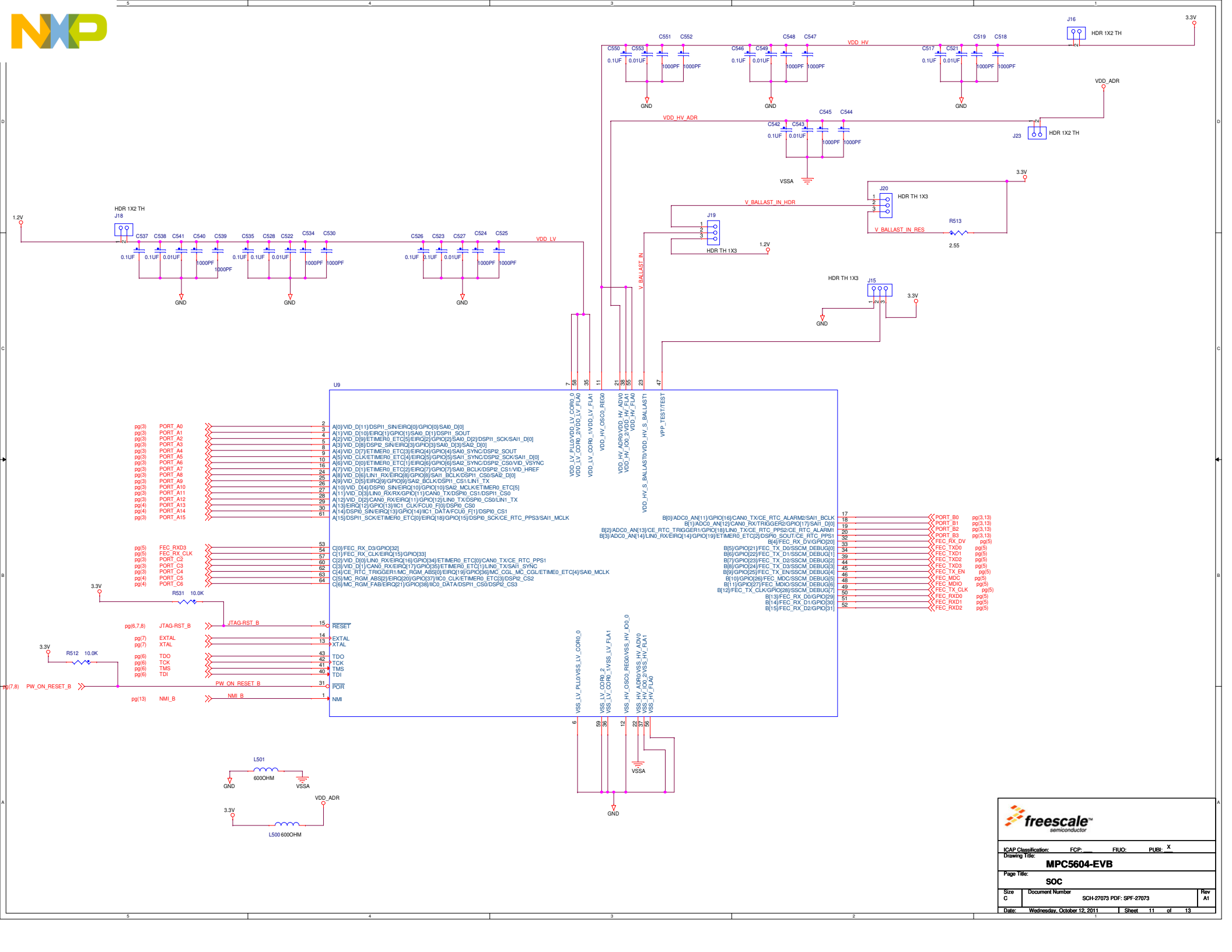

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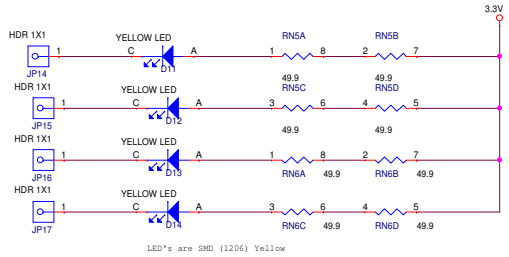
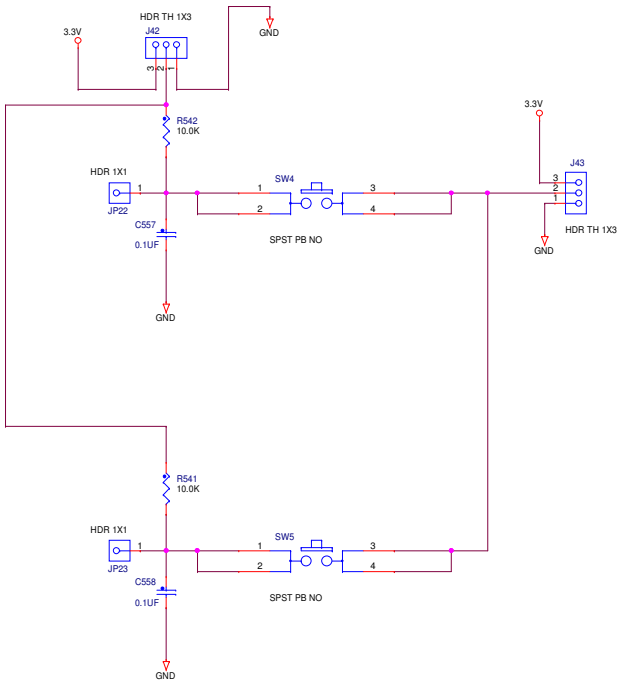
User LED's



User switches



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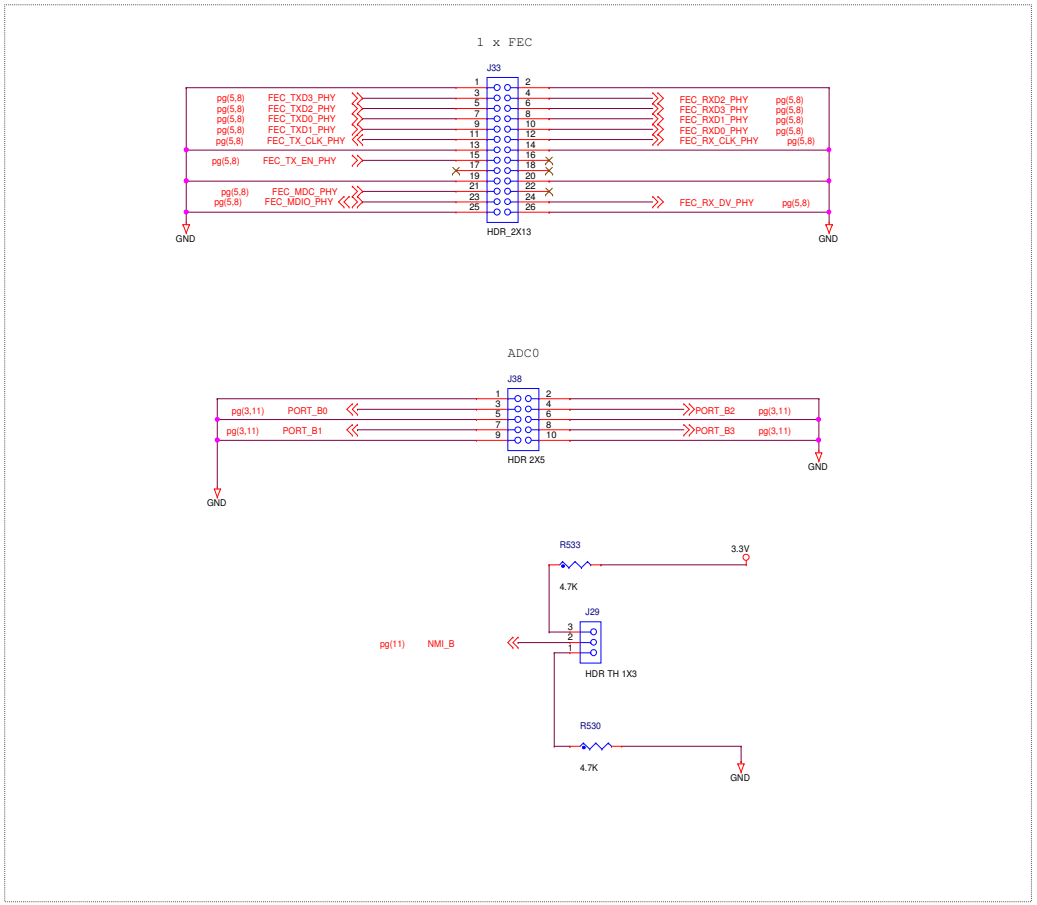

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USER I/O CONNECTORS

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