## Notes:
- All components and board processes are to be RoHS compliant.
- All capacitors are 10% tolerance unless otherwise stated.
- All resistors are 5% tolerance unless otherwise stated.
- All zero ohm links are 0603.
- All connectors and headers are denoted Fx and are 2.54mm pitch unless otherwise stated.
- All jumpers are denoted Jx. Jumpers are 2mm pitch.
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always po...en pin 1.
- All switches are denoted SWx.
- All test points (SMT wire loop style) are denoted TPx.
- Test point Vias (just through hole pads) are denoted TPVx.

### Specific PCB LAYOUT notes are detailed in ITALICS

## Caution:
These schematics are provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.
Board Power Block

Board supply selection

1-2 -> SBC Power Supply for analog circuit
2-3 -> USB/UART Power Supply for analog circuit

1-2 -> SBC Power Supply for digital circuit
2-3 -> USB/UART Power Supply for digital circuit

1-2 -> SBC Power Supply for Devkit Comm and Flexray
2-3 -> USB/UART Power Supply for Devkit Comm

USB Power Supply Connection

3.3V Switching Regulator with USB Power Supply

Layout note: follow IC datasheet recommendations for PCB layout and thermal dissipation

3.3V & 5V Power Decoupling

Test and reference points

Layout note: GND Test Points, Top Side

Layout note: Decoupling distributed uniformly
MCU Power Decoupling

Default Configuration:
- MCU supply voltages (VDD_HV_IO, VDD_HV_PMU, VDD_HV_OSC, VDD_HV_ADV, VDD_HV_FLA) are set to 3.3V
- MCU core voltage (VDD_LV_COREx, VDD_LV_PLLx) are set to 1.25V
- MCU analog reference voltage (VDD_HV_ADREx) are set to 3.3V default. Could be 5V, or from external J2 pin15 (3.15V~5.5V).

VDD_HV_ADRE0 and VDD_HV_ADRE1 cannot be operated at different voltages and need to be supplied by the same voltage source.

MCU Power

Layout notes: VDD_HV_PMU (3.3V) Decoupling.
Place 0.01uF caps close to VDD_HV_PMU pin.
Place the 0.1uF caps close to the jumper.

Layout notes: VDD_HV_PLL (1.25V) Decoupling.
Place 0.047uF caps close to VDD_HV_PLL pin.

Layout notes: VDD_HV_OSC (3.3V) Decoupling.
Place the 0.01uF caps close to VDD_HV_OSC pin.
Place the 0.1uF caps close to the jumper.

Layout notes: VDD_HV_FLA (3.3V) Decoupling.
Place the 0.01uF caps close to VDD_HV_FLA pin.
Place the 0.1uF caps close to the jumper.

Layout notes: VDD_HV_ADV (3.3V) Decoupling.
Place the 0.047uF and 0.01uF caps close to VDD_HV_ADV pin.
Place the 1uF caps close to the jumper.

Layout notes: VDD_HV_ARE1 (3.3V) Decoupling.
Place the 0.047uF and 0.01uF caps close to VDD_HV_ARE1 pin.
Place the 1uF caps close to the jumper.

Layout notes: VDD_HV_ARE0 (3.3V) Decoupling.
Place the 0.047uF and 0.01uF caps close to VDD_HV_ARE0 pin.
Place the 1uF caps close to the jumper.

VDD_AREF: ADC high reference voltage 3.3V
- 1-2 set jumper as 3.3V
- 2-3 set jumper as 5V
- from other boards set no jumper (and populate R81)
The scheme shown has the analogue and digital grounds connected to the same plane. This results in better ADC performance than using an analogue ground plane with single entry point (or ferrite) to digital ground plane.

Key to text colours:
- Purple - Comms Physical Interfaces
- Orange - Other Peripherals and I/O
- Blue - Debug (JTAG & Nexus)
- RED - I/O Matrix and other functions (eg. LED, BUTTON)
- Green - I/O Matrix (dedicated)
Boot, Reset & JTAG

**Pinball startup and reset states**

<table>
<thead>
<tr>
<th>Pinball</th>
<th>Startup state</th>
<th>State during reset</th>
<th>State after reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP0x</td>
<td>h-z</td>
<td>h-z</td>
<td>h-z</td>
</tr>
<tr>
<td>Analog inputs</td>
<td>h-z</td>
<td>h-z</td>
<td>h-z</td>
</tr>
<tr>
<td>JCOMP (TRST)</td>
<td>n-z</td>
<td>input, weak pull-down</td>
<td>input, weak pull-down</td>
</tr>
<tr>
<td>TDIO</td>
<td>h-z</td>
<td>output h-z</td>
<td>output h-z</td>
</tr>
<tr>
<td>TDO</td>
<td>h-z</td>
<td>input, weak pull-up</td>
<td>input, weak pull-up</td>
</tr>
<tr>
<td>TMS</td>
<td>h-z</td>
<td>input, weak pull-up</td>
<td>input, weak pull-up</td>
</tr>
<tr>
<td>TCK</td>
<td>h-z</td>
<td>input, weak pull-up</td>
<td>input, weak pull-up</td>
</tr>
<tr>
<td>XTAL/EXTAL</td>
<td>h-z</td>
<td>h-z</td>
<td>h-z</td>
</tr>
<tr>
<td>FOCU1 F0</td>
<td>h-z</td>
<td>input, hi-z</td>
<td>output/hi-z</td>
</tr>
<tr>
<td>FOCU1 F1</td>
<td>h-z</td>
<td>input, hi-z</td>
<td>output/hi-z</td>
</tr>
<tr>
<td>EXT POR.B</td>
<td>h-z</td>
<td>input, weak pull-down</td>
<td>input, weak pull-down</td>
</tr>
<tr>
<td>RESET_B</td>
<td>h-z</td>
<td>input, weak pull-down</td>
<td>input, weak pull-down</td>
</tr>
<tr>
<td>NWI_B</td>
<td>h-z</td>
<td>input, weak pull-up</td>
<td>input, weak pull-up</td>
</tr>
<tr>
<td>FAB</td>
<td>h-z</td>
<td>input, weak pull-down</td>
<td>input, weak pull-down</td>
</tr>
<tr>
<td>AB[5]</td>
<td>h-z</td>
<td>input, weak pull-down</td>
<td>input, weak pull-down</td>
</tr>
<tr>
<td>AB[4]</td>
<td>h-z</td>
<td>input, weak pull-down</td>
<td>input, weak pull-down</td>
</tr>
</tbody>
</table>

**JTAG Standard 14-pin Connector**

Layout Note: Clearly mark pin numbers 1, 2, 13 and 14. JTAG Connector

**BOOT CONFIGURATION**

J33, J34, J35 short in bottom layer default: Boot from Flash

Layout Note: Mark MC_RGM_ABS0, MC_RGM_ABS2, MC_RGM_FAB close to 028 pins
**Flexray_A, Flexray_B**

**FLEXRAY_A Physical Interface**

- Operational range is 4.45V to 60V
- Undervoltage detection is max 4.715V

On EVB this is supplied from 5V. In theory this should be to battery with 60uS delay between applying Vbat and I/O voltages. If necessary, 12V can be externally supplied by removing the resistor and connecting pad to 12V

**FLEXRAY_B Physical Interface**

- Operational range is 4.45V to 60V
- Undervoltage detection is max 4.715V

On EVB this is supplied from 5V. In theory this should be to battery with 60uS delay between applying Vbat and I/O voltages. If necessary, 12V can be externally supplied by removing the resistor and connecting pad to 12V.

**Notes on VBAT:**
- Operational range is 4.45V to 60V
- Undervoltage detection is max 4.715V

On EVB this is supplied from 5V. In theory this should be to battery with 60uS delay between applying Vbat and I/O voltages. If necessary, 12V can be externally supplied by removing the resistor and connecting pad to 12V.

**Bus voltage +/- 12V (VBAT = 12V)**

Components spec'd for 12V operation.

**Bus voltage +/- 12V (VBAT = 12V)**

Components spec'd for 12V operation.
The CSLEW pin is provided to increase control of the output voltage ramp at turn-on. The upper limit on the value of \( C_f \) is 4\,\text{nF}. Herein, \( C_f \) is DNP – only a footprint for further use.
User Peripherals

User Pushbutton Switches (Active High)

ADC Input Pot and Test Point

User RGB LED (Active Low)

LEVEL TRANSLATOR FOR FRDM+

1-2 → 3.3V
2-3 → 5V

NTB0102DP active HIGH
no jumper → ON
jumper on → OFF

1-2 → 3.3V
2-3 → 5V

MTB0104BQ active HIGH
no jumper → ON
jumper on → OFF

1-2 → 3.3V
2-3 → 5V

Alternative Arduino compatible pins
default PWM with jumper on J30
with no jumper on J27

Alternative Analog with jumper on J27
with no jumper on J30

When MCU_RSTx = HIGH, U25.4 as input/high impedance;
When MCU_RSTx = LOW, LT_MCU-RSTx is LOW.
NOTE:

Arduino UNO compatible headers:
J1, J2, J3, J4

FRDM+ MC SHIELD/DEVKIT-MOTORGD compatible headers:
J1, J2, J3, J4, J5

DEVKIT-COMM compatible headers:
J1, J2, J3, J4, J5, J6

Populate R81 for external ADC high reference voltage

Check external power before put on the shunt

Layout notes (at least):
EXT_HV_PWR: 20mil
EXT_AR_PWR: 20mil x2
EXT_LV_PWR: 40mil x2
5V0_SR: 20mil
3V3_SR: 20mil x3

FRDM+ I/O interface default 3.3V
Not all pins are compatible 5V
Net with prefix ‘LT’ for 5V option
Configuration of Power SBC:
- DFS Enabled
- VDDIO connected to Vcore
- FS0b on VDDIO
- Vcore regulator set to 3.3V
- Vcca regulator set to 3.3V
- Vcca regulator using external PMOS
- Vaux regulator set to 5V
- Vpre regulator configured in Buck or Boost mode

Layout note:
- ADD Graphical silk
- SH1
- SH2
- GREEN
- RED
- LED Signalling

Power SBC, CAN, LIN

Vcore

Vaux

DFS Mode
Select mode

CAN

LIN

Layout notes:
- Vcore (R126)
- Vpre (R126)
- Default: 1-2 shunt Default: No Shunts
- (RESET & NMI don't go to the SBC)