

DEVKIT-MPC5744P

Table Of Contents:

Block Diagram	Sheet 2
Board Power	Sheet 3
MCU Power	Sheet 4
MCU Pins	Sheet 5
Boot, Reset & JTAG	Sheet 6
Flexray, CAN, LIN	Sheet 7
OpenSDA	Sheet 8
User Peripherals	Sheet 9
FRDM+ Connectors	Sheet 10

Revision Information

Rev	Date	Designer	Comments
X1	6 July 2016	Jun Qiao	Initial
X2	12 July 2016	Jun Qiao	Update MCU decoupling, add boot section
X3	19 July 2016	Jun Qiao	Update MCU decoupling, update notes, rename nets
A	22 July 2016	Jun Qiao	Update J13 setting, update power to RV1, update notes
A1	26 Aug 2016	Jun Qiao	Update FRDM+ connection compatible to DEVKIT-MOTORGF
A2	5 Sept 2016	Jun Qiao	Add test points
A3	7 Sept 2016	Jun Qiao	Change U15 to NX5P2190UKZ, change R57 to 100K
A4	9 Sept 2016	Jun Qiao	Remove D8, add J39
A5	13 Sept 2016	Jun Qiao	Set power net 12V_IN at U1 pin 1, add R88
A6	20 Sept 2016	Jun Qiao	Change R56 from 10K to 20K, and connected to P3V3_SDA
A7	23 Sept 2016	Jun Qiao	Change U15 to MIC2005-0.8YM6, remove R57, change R56 to 10K, add C87
B	28 Sept 2016	Jun Qiao	Release

Notes:

- All components and board processes are to be ROHS compliant
- All capacitors are 10% tolerance unless otherwise stated
- All resistors are 5% tolerance unless otherwise stated
- All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2
- 2 Pin jumpers generally have the "source" on pin 1
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

3 Different test points used in design:

TPVx - Through Hole Pad small



TPHx - Through Hole Pad Large (for standard 0.1" header).
Also used on IO Matrix (IOMx)



TPX - Surface Mount Wire Loop



User notes are given throughout the schematics.

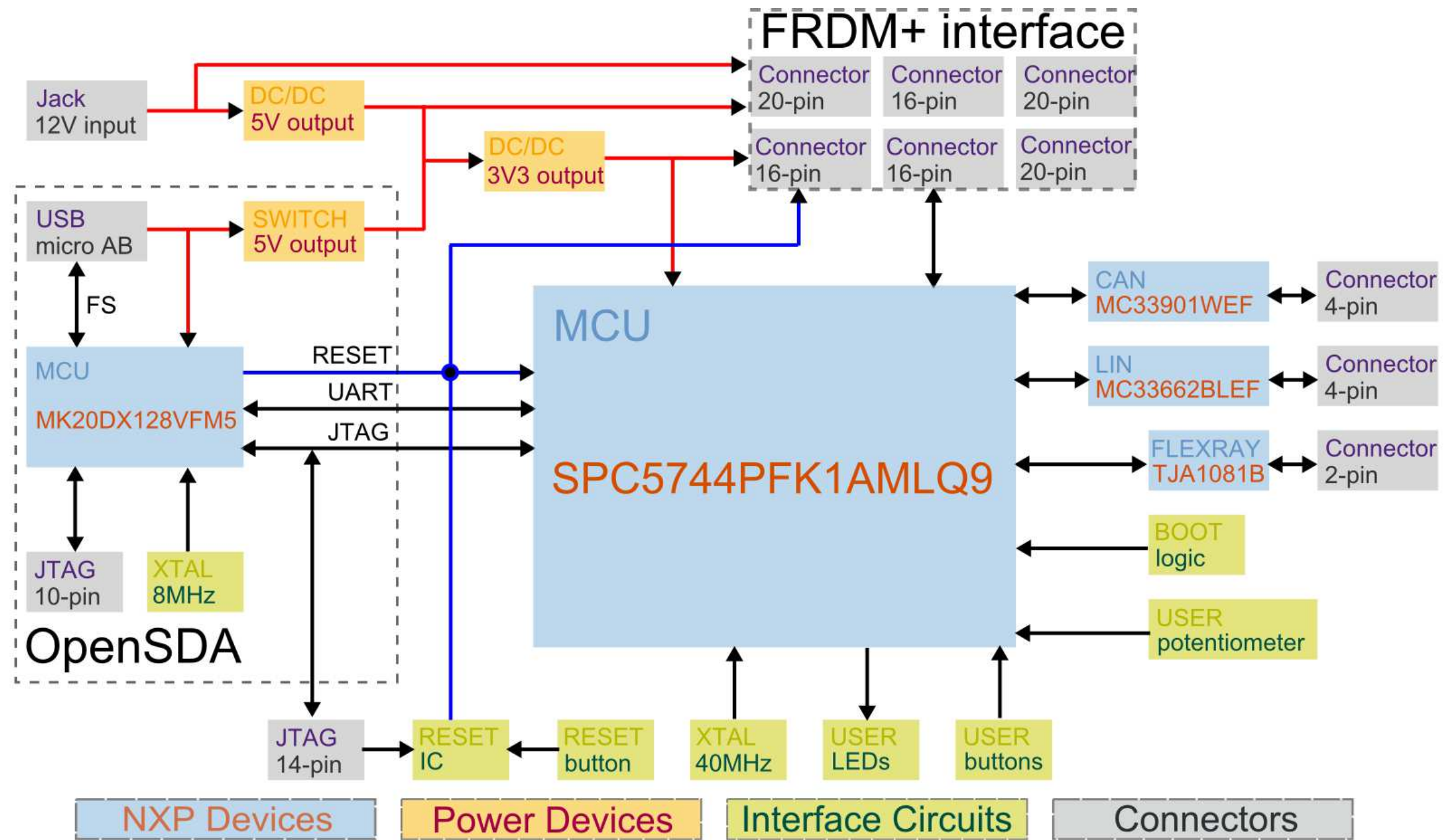
Specific PCB LAYOUT notes are detailed in *ITALICS*

Caution:

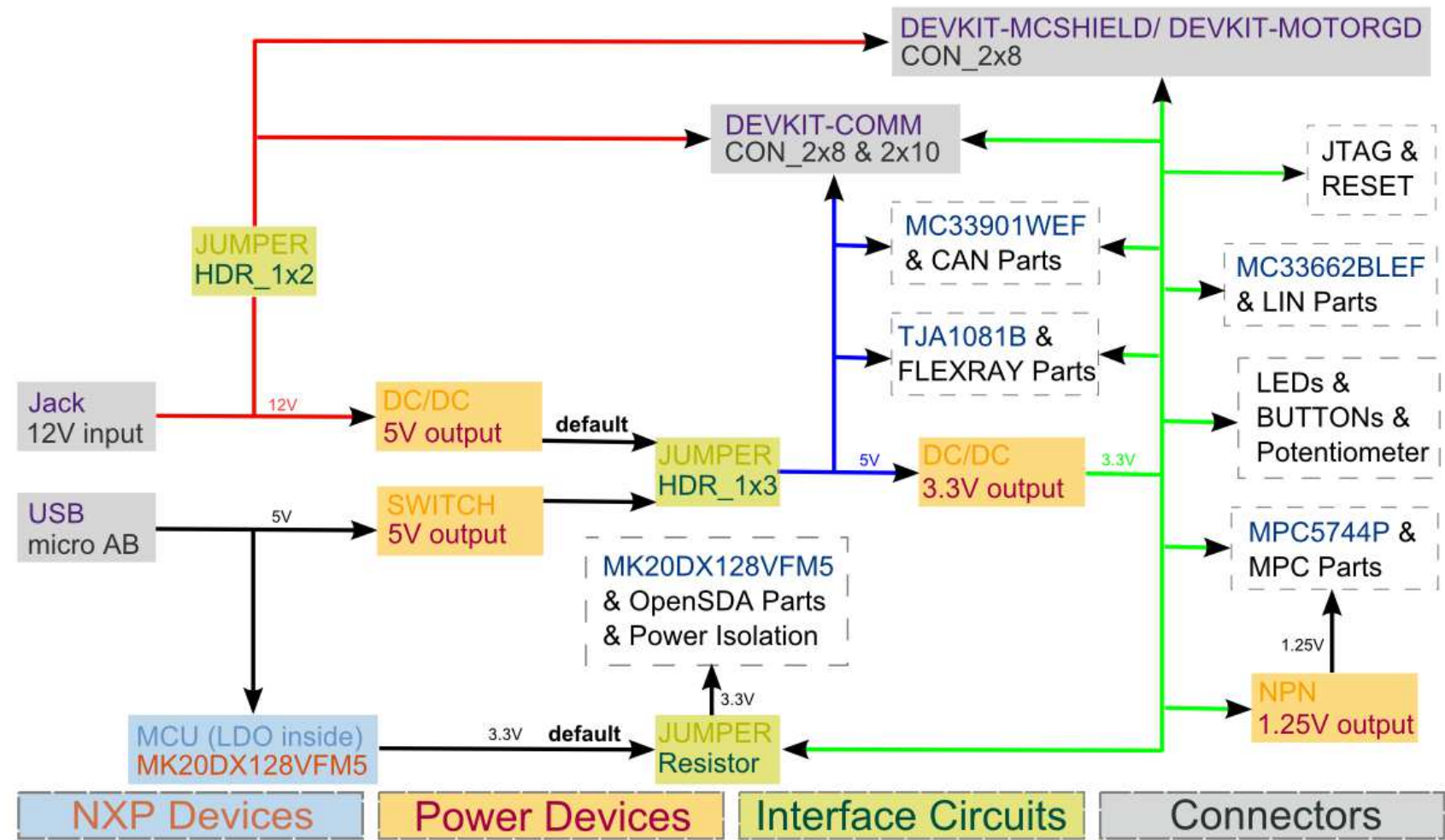
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ICAP Classification: CP:		IJO: X PUBL:	
Designer: Jun Qiao	Drawing Title: DEVKIT-MPC5744P		
Drawn by: Jun Qiao	Page Title: Index, Rev, Notes		
Approved: Pesses Philip	Size C	Document Number SCH-29333 PDF: SPF-29333	Rev B
Date: Wednesday, September 28, 2016		Sheet 1 of 10	

Block Diagram

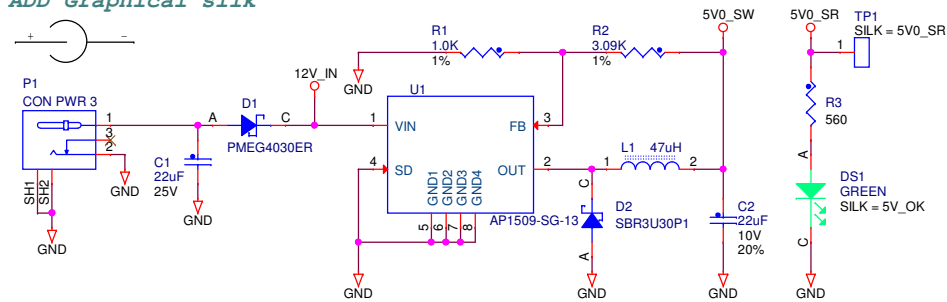


Board Power



5V Switching Regulator

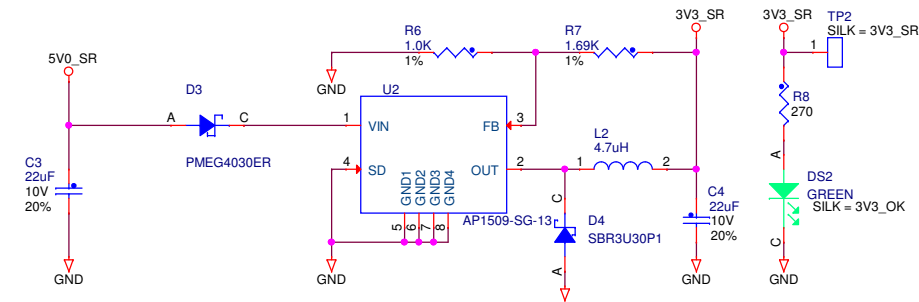
Layout note: Input Voltage 12V, Output 5V at 1800mA
ADD Graphical silk



Layout note: follow IC datasheet recommendations for PCB layout and thermal dissipation

3.3V Switching Regulator

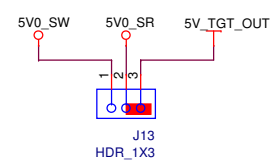
Input Voltage 5V, Output 3.3V at 1600mA



Layout note: follow IC datasheet recommendations for PCB layout and thermal dissipation

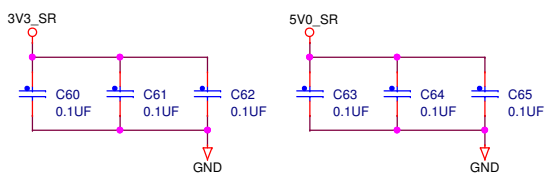
Board supply selection

Select between USB and external 12V



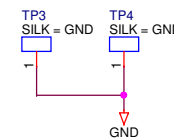
1-2 -> external 12V
2-3 -> USB/UART connector

3.3V & 5V Power Decoupling



Layout note: Decoupling distributed uniformly

Test and reference points



Layout note: GND Test Points, Top Side

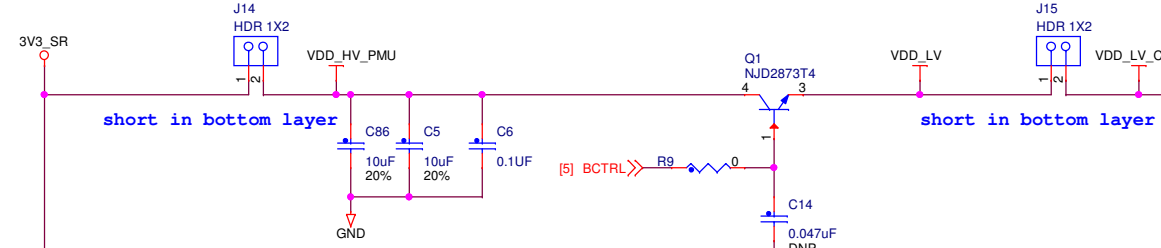


ICAP Classification: CP: IUC: X PUBL:			
Drawing Title: DEVKIT-MPC5744P			
Page Title: Board Power			
Size C	Document Number SCH-29333	PDF: SPF-29333	Rev B
Date: Wednesday, September 28, 2016 Sheet 3 of 10			

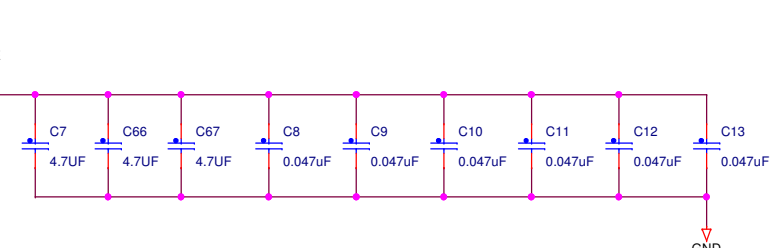
MCU Power

MCU Power Decoupling

Default Configuration:
 - MCU supply voltages (VDD_HV_IO, VDD_HV_PMU, VDD_HV_OSC, VDD_HV_ADV, VDD_HV_FLA) are set to 3.3V
 - MCU core voltage (VDD_LV_CORE, VDD_LV_PLL) are set to 1.25V
 - MCU analog reference voltage (VDD_HV_AREx) are set 3.3V default. Could be 5V, or from external J2 pin15 (3.15V~5.5V).
 VDD_HV_ADRE0 and VDD_HV_ADRE1 cannot be operated at different voltages and need to be supplied by the same voltage source.



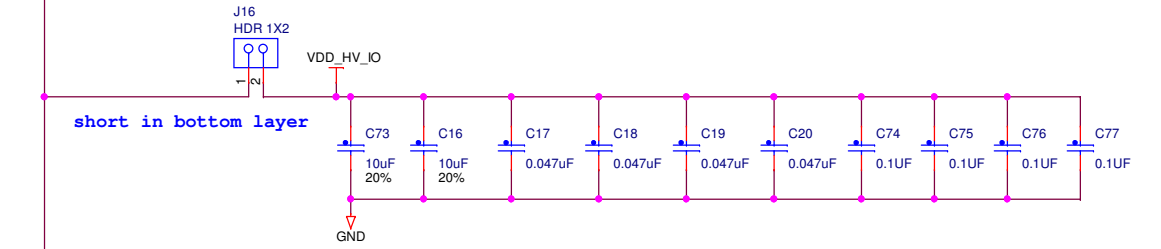
Layout notes: VDD_HV_PMU (3.3V) Decoupling.
 Place 0.01uF caps close to VDD_HV_PMU pin.
 Place the 10uF caps close to the jumper.



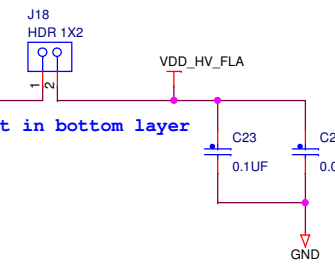
Layout notes: VDD_LV_CORE (1.25V) Decoupling.
 Place one of the 0.047uF caps close to each VDD_LV_CORE pin.
 Place the 4.7uF caps close to the jumper.



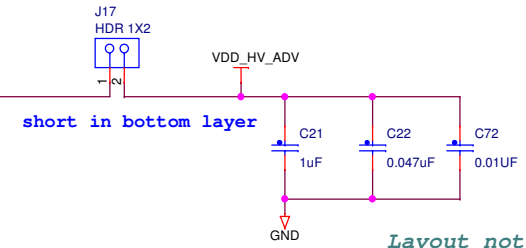
Layout notes: VDD_LV_PLL (1.25V) Decoupling.
 Place the 0.047uF caps close to VDD_LV_PLL pin.



Layout notes: VDD_HV_IO (3.3V) Decoupling.
 Place one of the 0.047uF and 0.01uF caps close to each VDD_HV_IO pin.
 Place the 10uF caps close to the jumper.

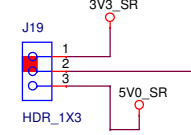


Layout notes: VDD_HV_FLA (3.3V) Decoupling.
 Place the 0.01uF caps close to VDD_HV_FLA pin.
 Place the 0.1uF caps close to the jumper.

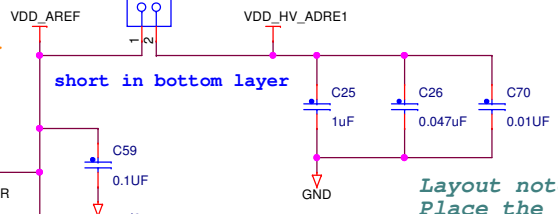


Layout notes: VDD_HV_ADV (3.3V) Decoupling.
 Place the 0.047uF and 0.01uF caps close to VDD_HV_ADV pin.
 Place the 1uF caps close to the jumper.

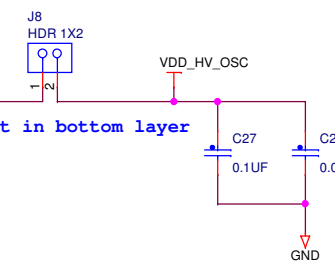
1-2 -> 3.3V
 2-3 -> 5V



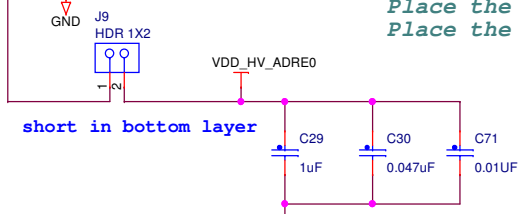
VDD_AREF: ADC high reference voltage
 3.3V set jumper as 1-2
 5V set jumper as 2-3
 from other boards set no jumper (and populate R81)



Layout notes: VDD_HV_ARE1 (3.3V) Decoupling.
 Place the 0.047uF and 0.01uF caps close to VDD_HV_ARE1 pin.
 Place the 1uF caps close to the jumper.



Layout notes: VDD_HV_OSC (3.3V) Decoupling.
 Place the 0.01uF caps close to VDD_HV_OSC pin.
 Place the 0.1uF caps close to the jumper.



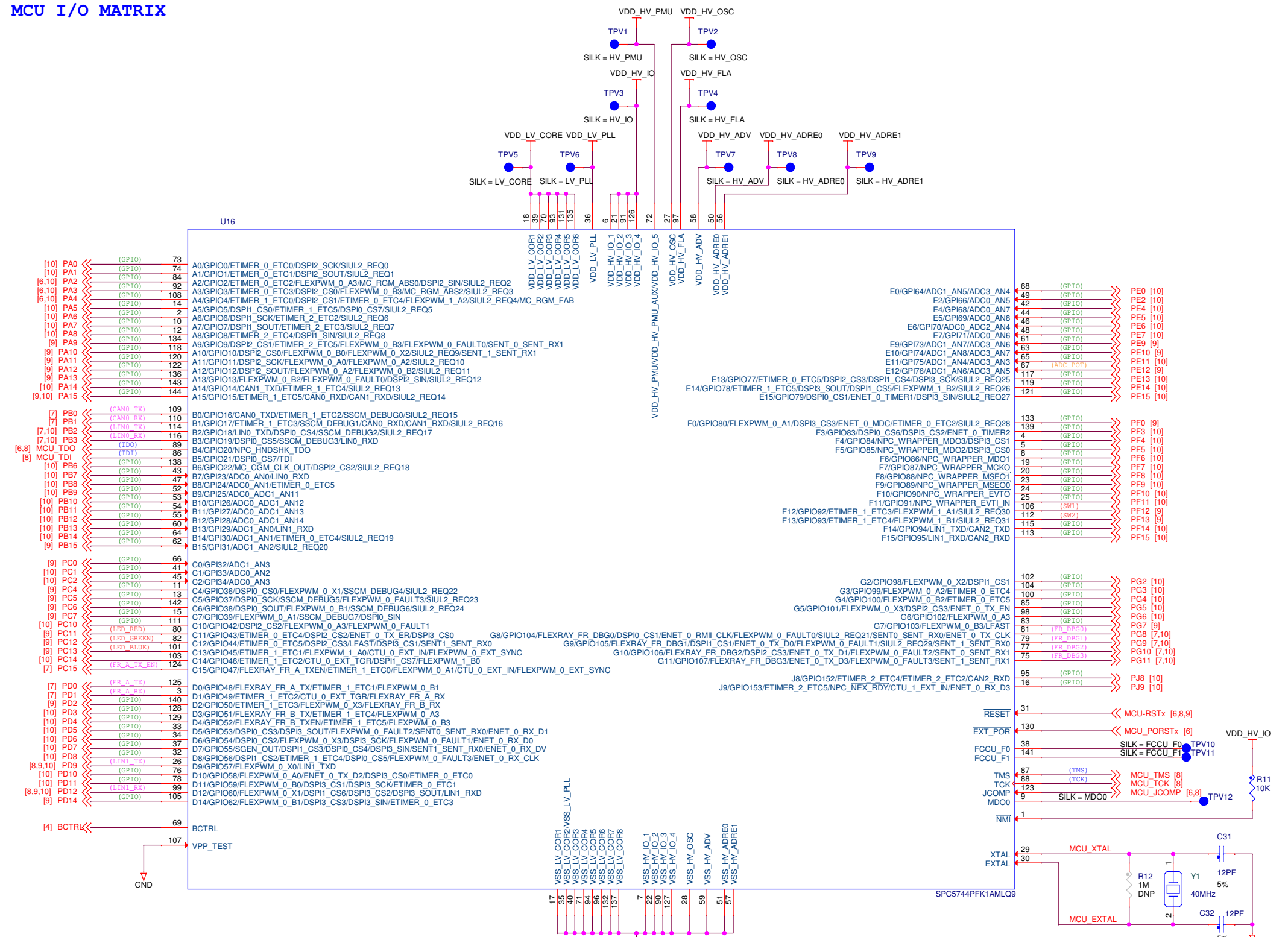
Layout notes: VDD_HV_ARE0 (3.3V) Decoupling.
 Place the 0.047uF and 0.01uF caps close to VDD_HV_ARE0 pin.
 Place the 1uF caps close to the jumper.



ICAP Classification: CP: IUC: X PUBL:			
Drawing Title: DEVKIT-MPC5744P			
Page Title: MCU Power			
Size C	Document Number SCH-29333	PDF: SPF-29333	Rev B
Date: Wednesday, September 28, 2016	Sheet 4	of 10	

MCU Pins

MCU I/O MATRIX




Layout notes on signal Grounds:

- The scheme shown has the analogue and digital grounds connected to the same plane
- This results in better ADC performance than using an analogue ground plane with single entry point (or ferrite) to digital ground plane.

CX3225GA4000D0PTVZ1
(Optimised for Automotive, 8pF Load capacitance)

Key to text colours:

- Purple** - Comms Physical Interfaces
- Orange** - Other Peripherals and I/O
- Blue** - Debug (JTAG & Nexus)
- Black** - Clock, Reset and Control
- RED** - I/O Matrix and other functions (eg. LED, BUTTON)
- Green** - I/O Matrix (dedicated)



ICAP Classification: CP: IUC: X PUBL:

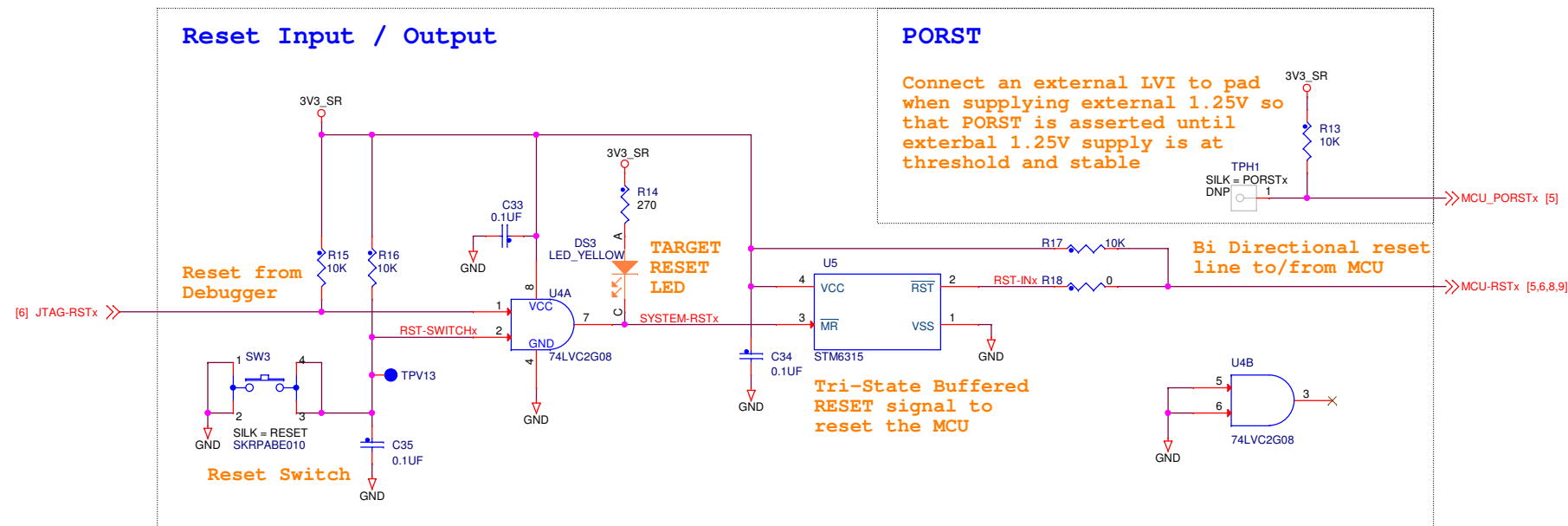
Drawing Title: **DEVKIT-MPC5744P**

Page Title: **MCU Pins**

Size C	Document Number	SCH-29333	PDF: SPF-29333	Rev B
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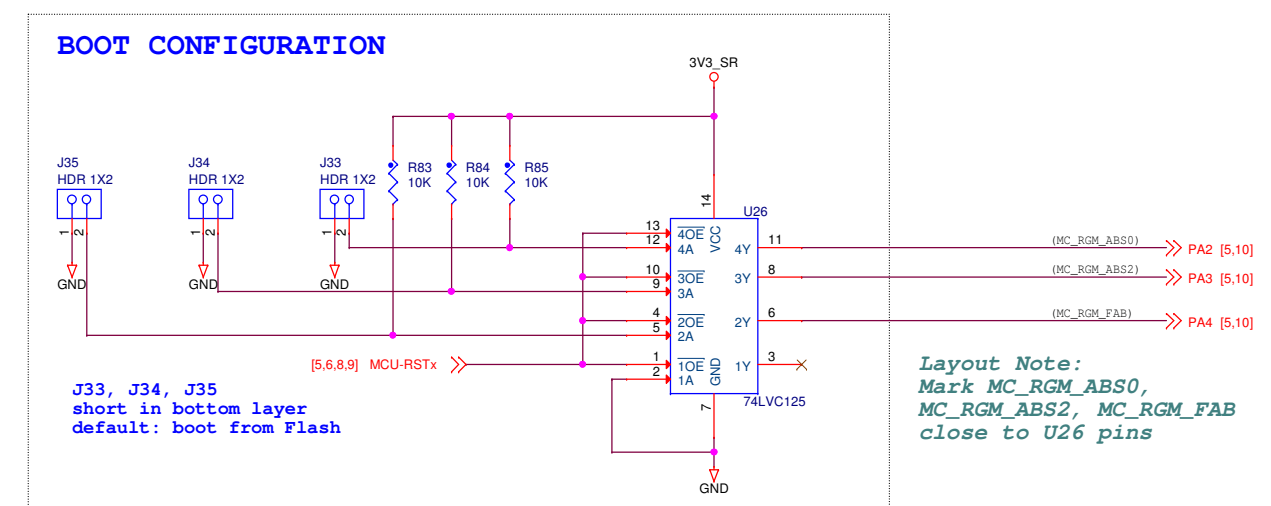
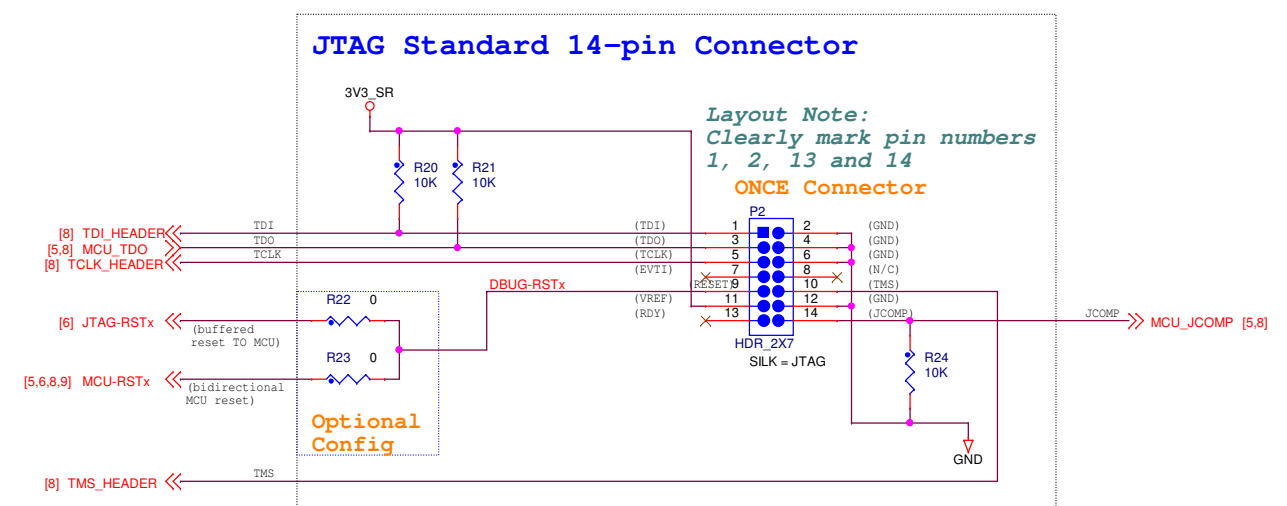
Date: Wednesday, September 28, 2016 Sheet 5 of 10

Boot, Reset & JTAG



Pin/ball startup and reset states

Pin/ball	Startup state	State during reset	State after reset
GPIOs	hi-z	hi-z	hi-z
Analog inputs	hi-z	hi-z	hi-z
JCOMP (TRST)	hi-z	input, weak pull-down	input, weak pull-down
TDI	hi-z	input, weak pull-up	input, weak pull-up
TDO	hi-z	output, hi-z	output, hi-z
TMS	hi-z	input, weak pull-up	input, weak pull-up
TCK	hi-z	input, weak pull-up	input, weak pull-up
XTAL/EXTAL	hi-z	hi-z	hi-z
FCCU_F[0]	hi-z	input, hi-z	output/input, hi-z
FCCU_F[1]	hi-z	input, hi-z	output/input, hi-z
EXT_POR_B	hi-z	input, weak pull-down	input, weak pull-down
RESET_B	hi-z	input, weak pull-down	input, weak pull-down
NMI_B	hi-z	input, weak pull-up	input, weak pull-up
FAB	hi-z	input, weak pull-down	input, weak pull-down
ABS[2]	hi-z	input, weak pull-down	input, weak pull-down
ABS[0]	hi-z	input, weak pull-down	input, weak pull-down



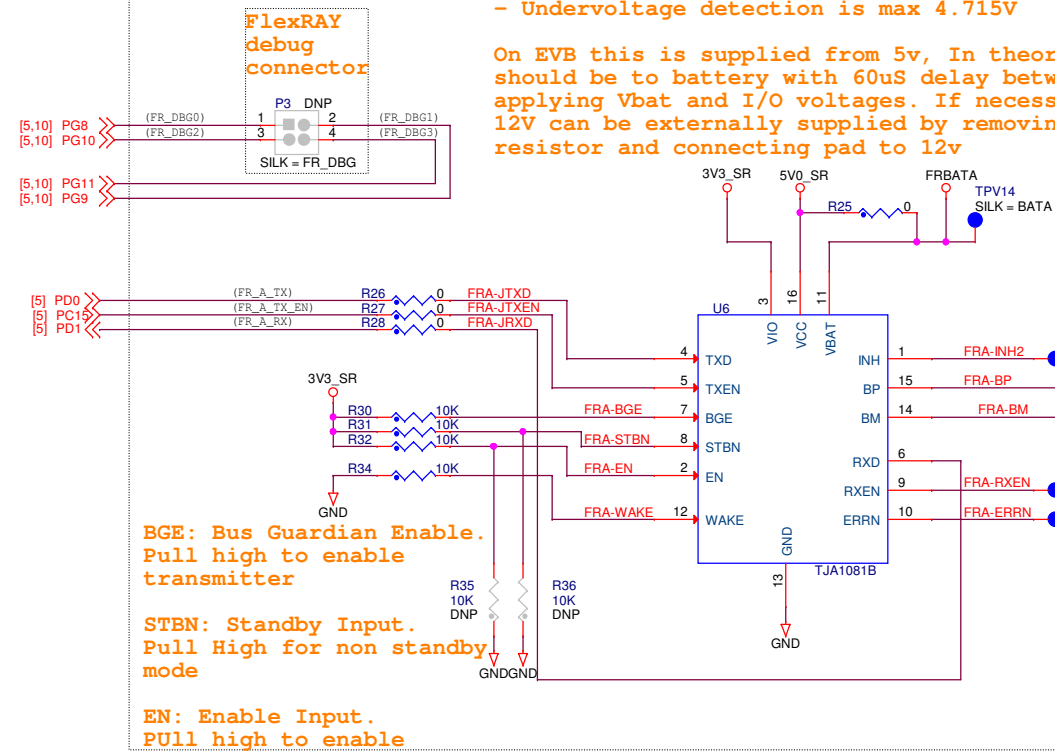
Flexray, CAN, LIN

State transitions forced by EN and STBN

→ indicates the action that initiates a transaction

Transition from mode	Direction to mode	Transition number	Pin	STBN	EN
Normal	Receive-only	1	H	→ L	
	Go-to-sleep	2	→ L	H	
	Standby	3	→ L	→ L	
Receive-only	Normal	4	H	→ H	
	Go-to-sleep	5	→ L	→ H	
	Standby	6	→ L	L	
Standby	Normal	7	→ H	→ H	
	Receive-only	8	→ H	L	
	Go-to-sleep	9	L	→ H	
Go-to-sleep	Normal	10	→ H	H	
	Receive-only	11	→ H	→ L	
	Standby	12	L	→ L	
Sleep	Normal	14	→ H	H	
	Receive-only	15	→ H	L	
	Standby	16	→ H	X	

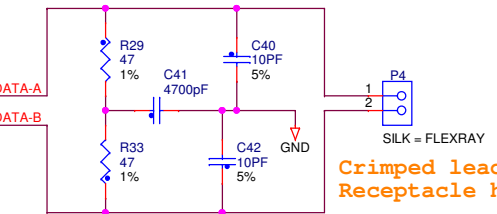
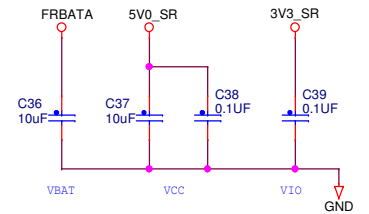
FLEXRAY_A Physical Interface



Note on VBAT:
 - Operational range is 4.45V to 60V
 - Undervoltage detection is max 4.715V

On EVB this is supplied from 5v, In theory this should be to battery with 60uS delay between applying Vbat and I/O voltages. If necessary, 12V can be externally supplied by removing the resistor and connecting pad to 12v

Layout notes: decoupling
 Place next to power pins.



Bus voltage +/- 12V (VBAT = 12v)
 Components spec'd for 12V operation

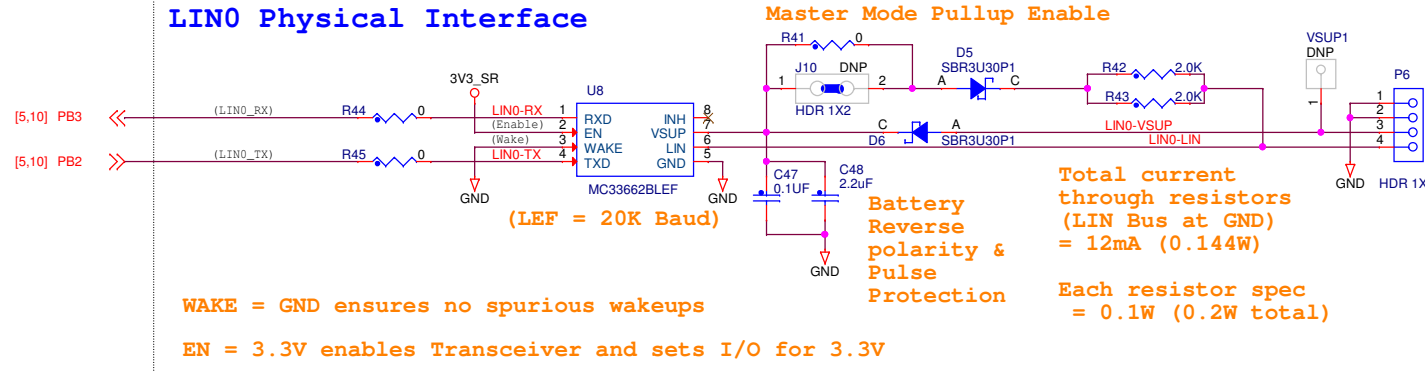
Crimped lead - 279-9522
 Receptacle housing - 279-9156

BGE: Bus Guardian Enable.
 Pull high to enable transmitter

STBN: Standby Input.
 Pull High for non standby mode

EN: Enable Input.
 Pull high to enable

LINO Physical Interface



MC33662LEF LIN transceiver is newer version of 33661 offering:

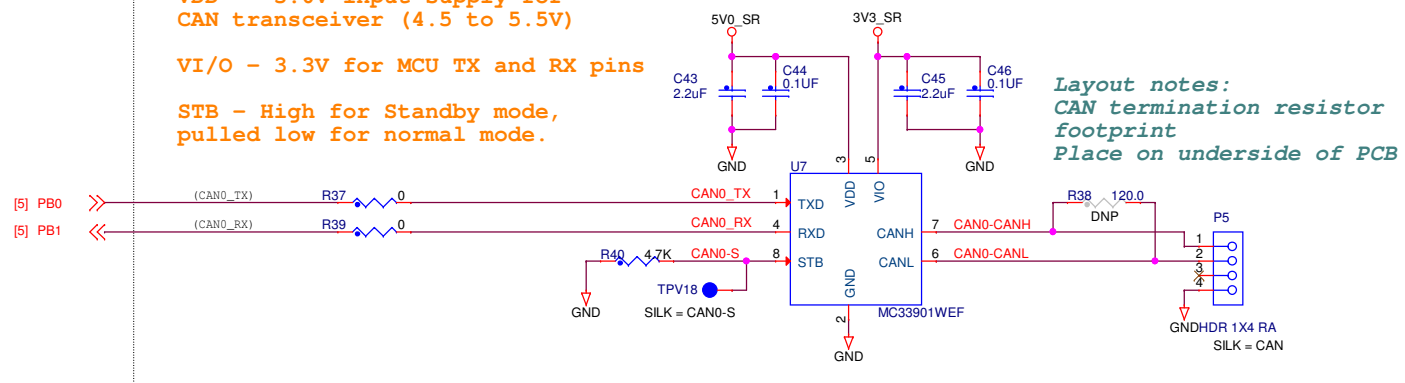
- Full LIN compliance (33661 no longer compliant)
 - Improved ESD protection on LIN pin up to 15KV
 - Improved ESD on Wake and VSUP Pins
 - Other EMC and performance improvements
- See www.nxp.com for more details

CAN0 Physical Interface

VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)

VI/O - 3.3V for MCU TX and RX pins

STB - High for Standby mode, pulled low for normal mode.



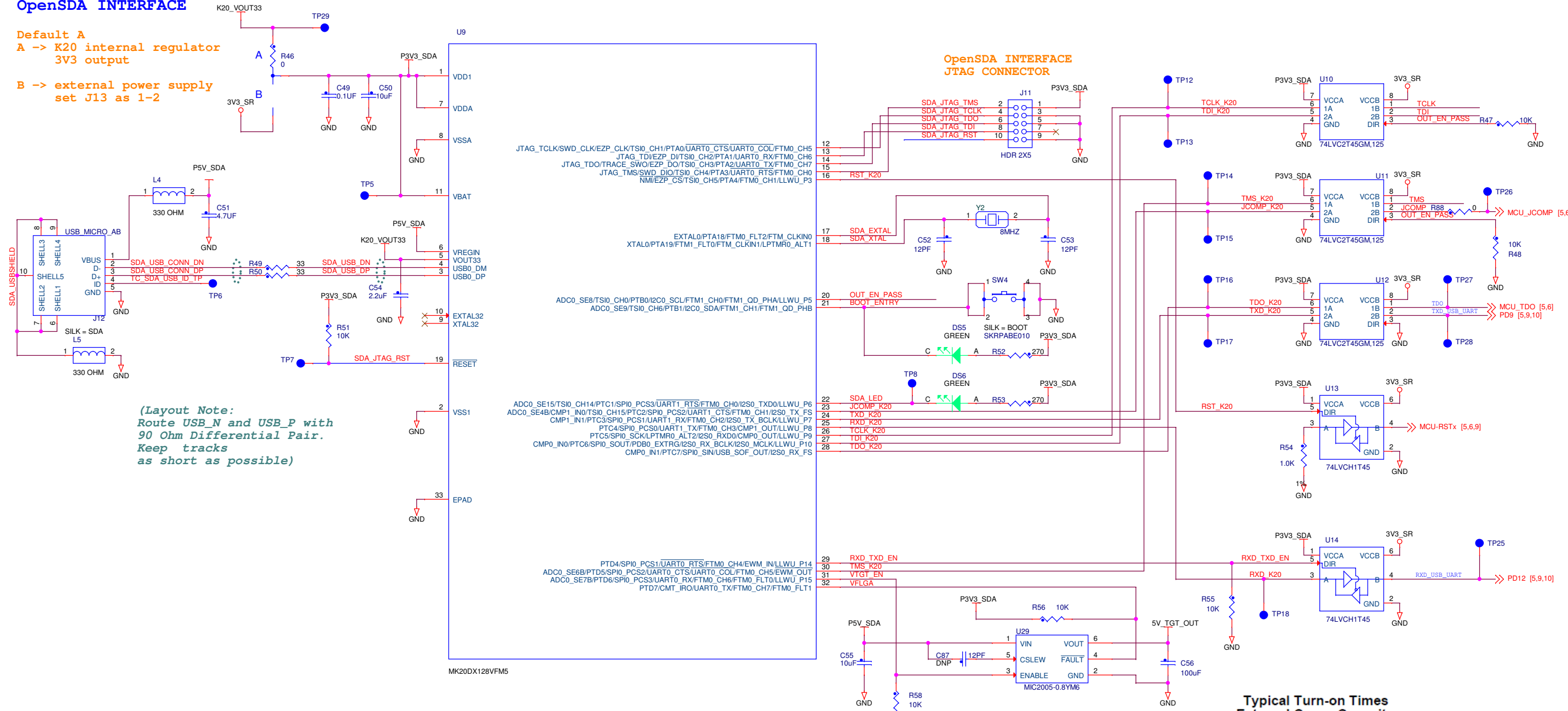
Layout notes:
 CAN termination resistor footprint
 Place on underside of PCB



OpenSDA

OpenSDA INTERFACE

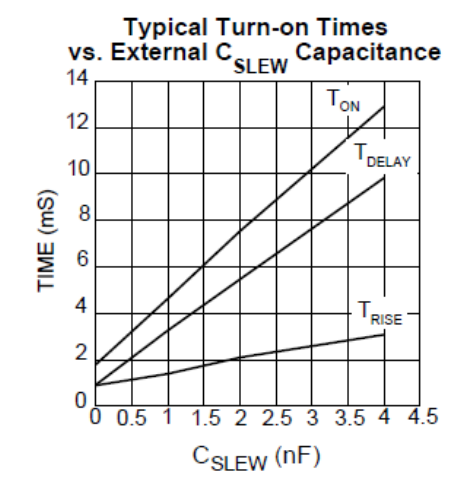
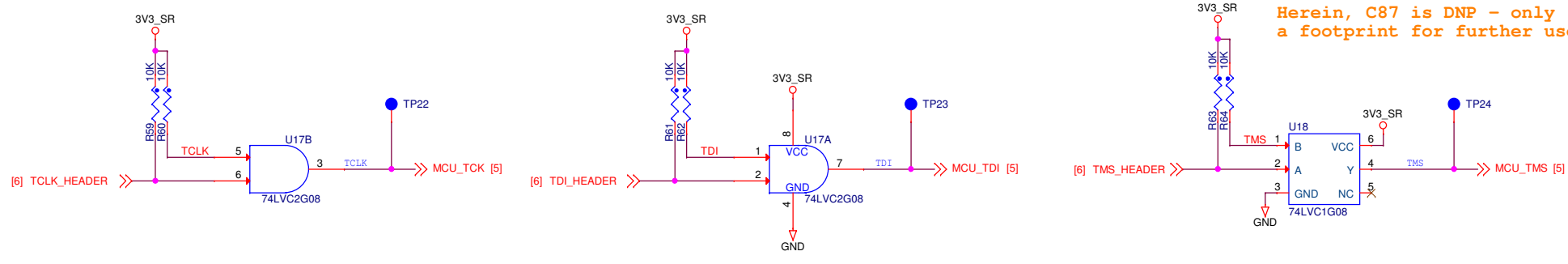
- Default A
- A -> K20 internal regulator 3V3 output
- B -> external power supply set J13 as 1-2



*(Layout Note:
Route USB_N and USB_P with
90 Ohm Differential Pair.
Keep tracks
as short as possible)*

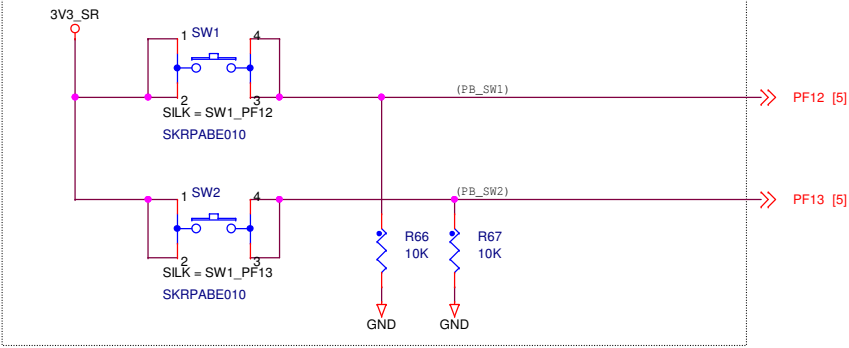
OpenSDA INTERFACE JTAG CONNECTOR

The CSLEW pin is provided to increase control of the output voltage ramp at turn-on. The upper limit on the value of C87 is 4nF. Herein, C87 is DNP - only a footprint for further use.

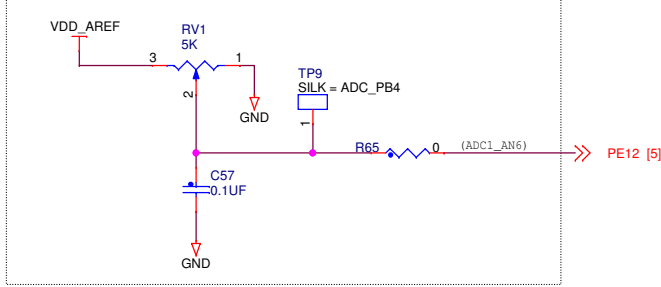


User Peripherals

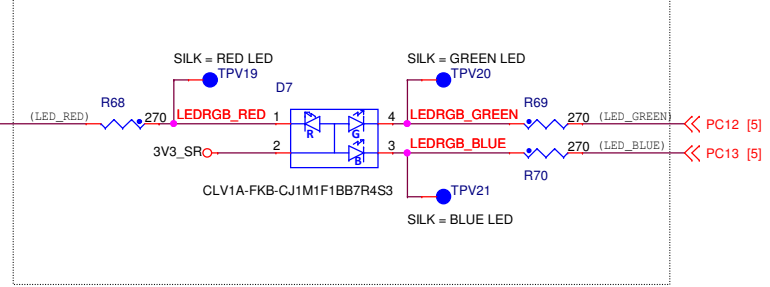
User Pushbutton Switches (Active High)



ADC Input Pot and Test Point



User RGB LED (Active Low)



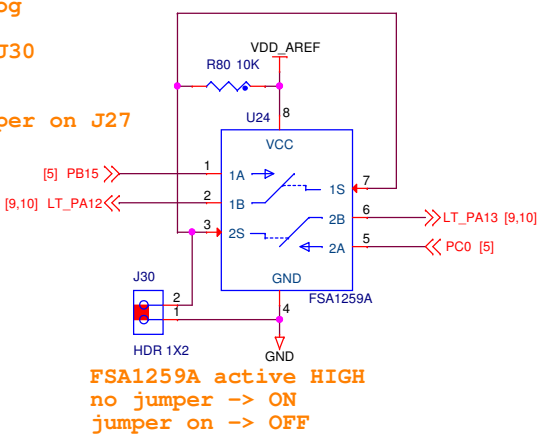
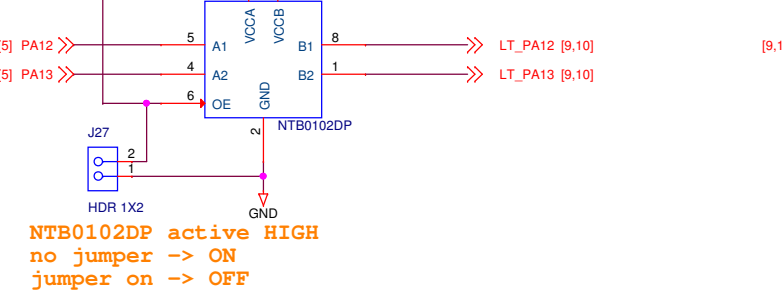
LEVEL TRANSLATOR FOR FRDM+

1-2 -> 3.3V
2-3 -> 5V

Arduino UNO compatible pins
alternative for PWM or Analog

default PWM with jumper on J30
with no jumper on J27

alternative Analog with jumper on J27
with no jumper on J30

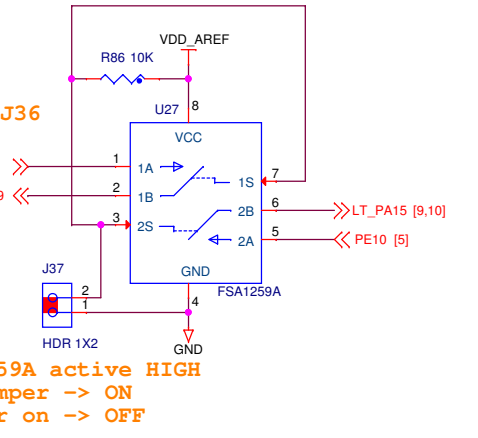
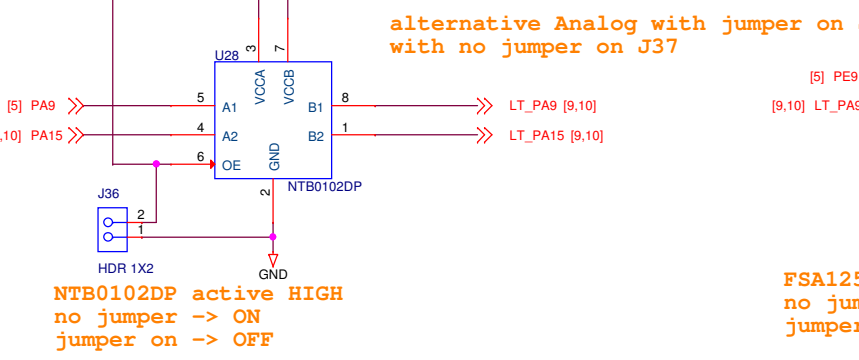


1-2 -> 3.3V
2-3 -> 5V

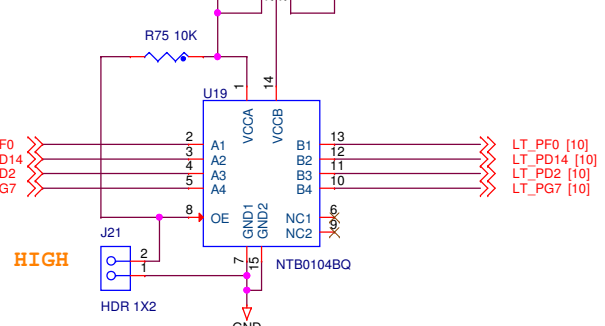
Arduino UNO compatible pins
alternative for PWM/IRQ or Analog

default PWM/IRQ with jumper on J37
with no jumper on J36

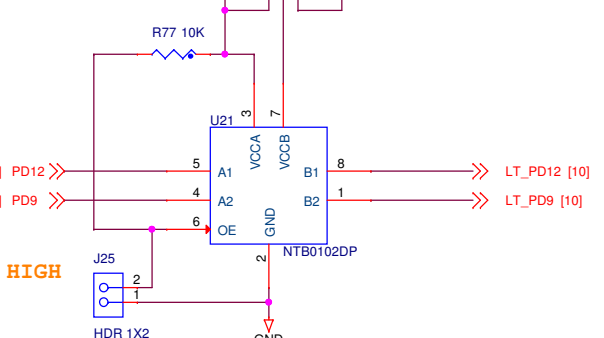
alternative Analog with jumper on J36
with no jumper on J37



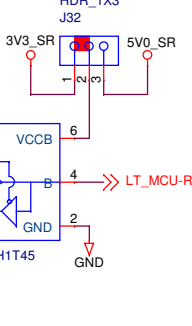
1-2 -> 3.3V
2-3 -> 5V



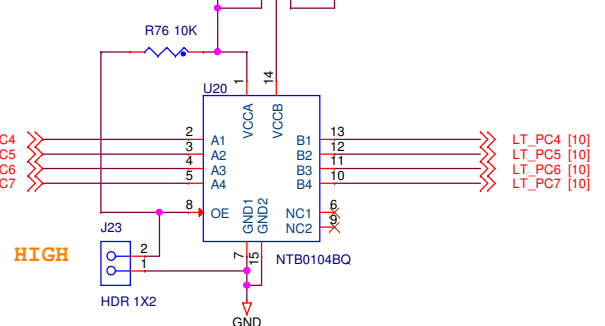
1-2 -> 3.3V
2-3 -> 5V



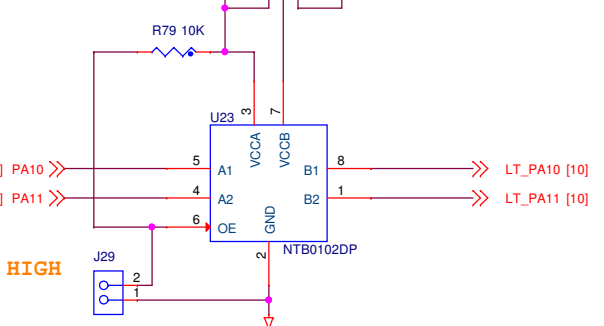
1-2 -> 3.3V
2-3 -> 5V



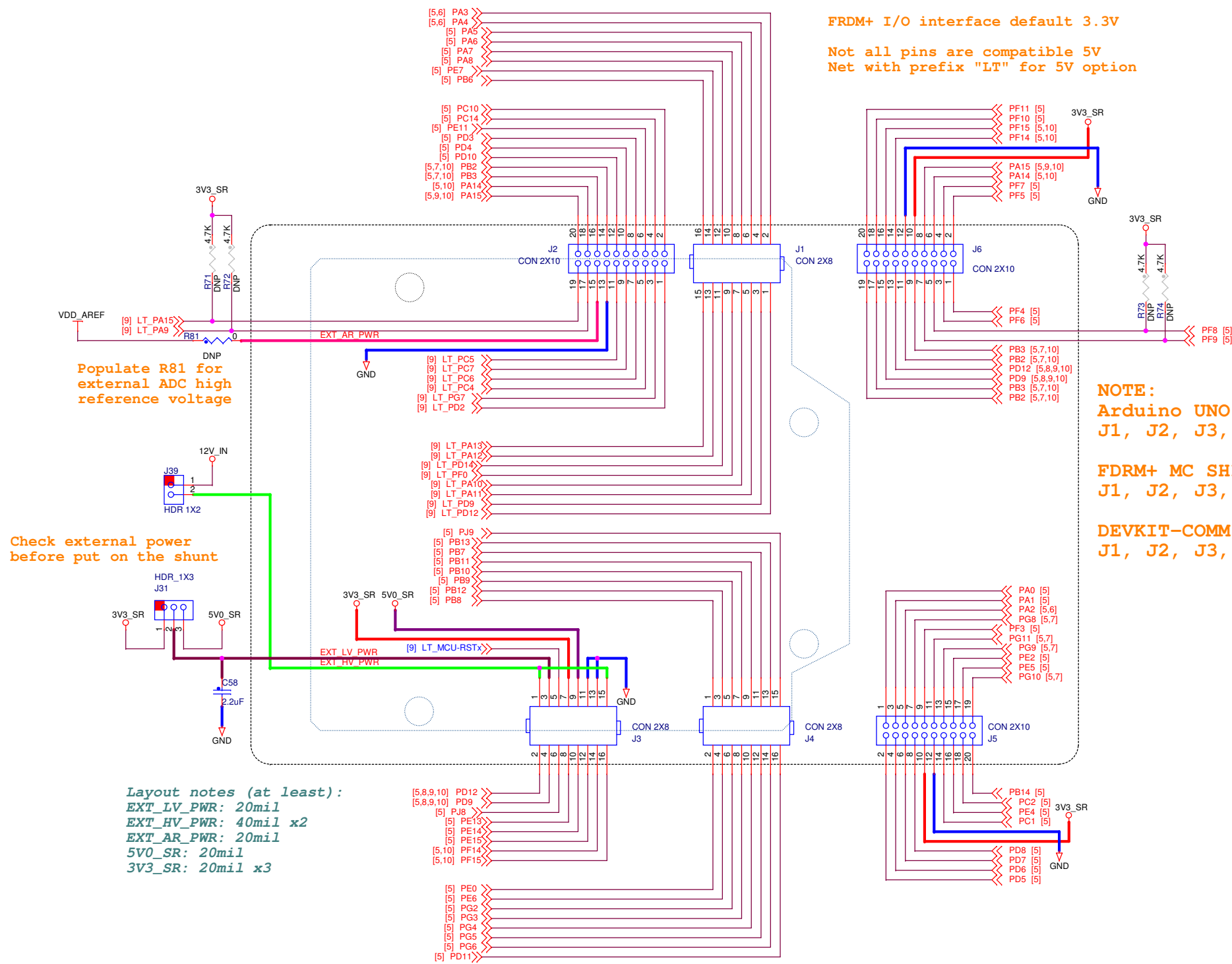
1-2 -> 3.3V
2-3 -> 5V



1-2 -> 3.3V
2-3 -> 5V



FRDM+ Connectors



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Size C	Document Number SCH-29333 PDF: SPF-29333	Rev B
Date: Wednesday, September 28, 2016	Sheet 10	of 10