



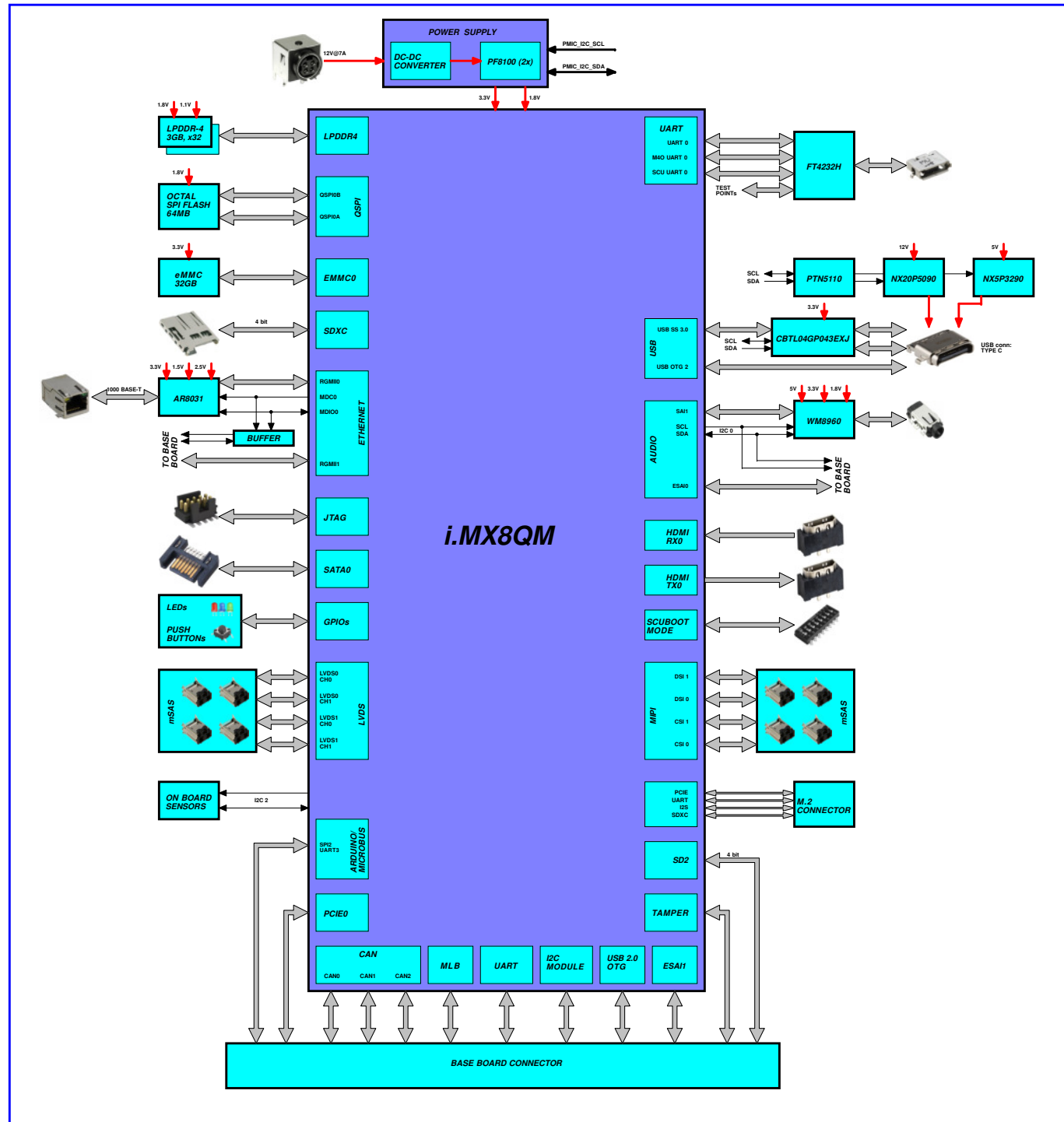
## MCIMX8QM-CPU MEK Platform

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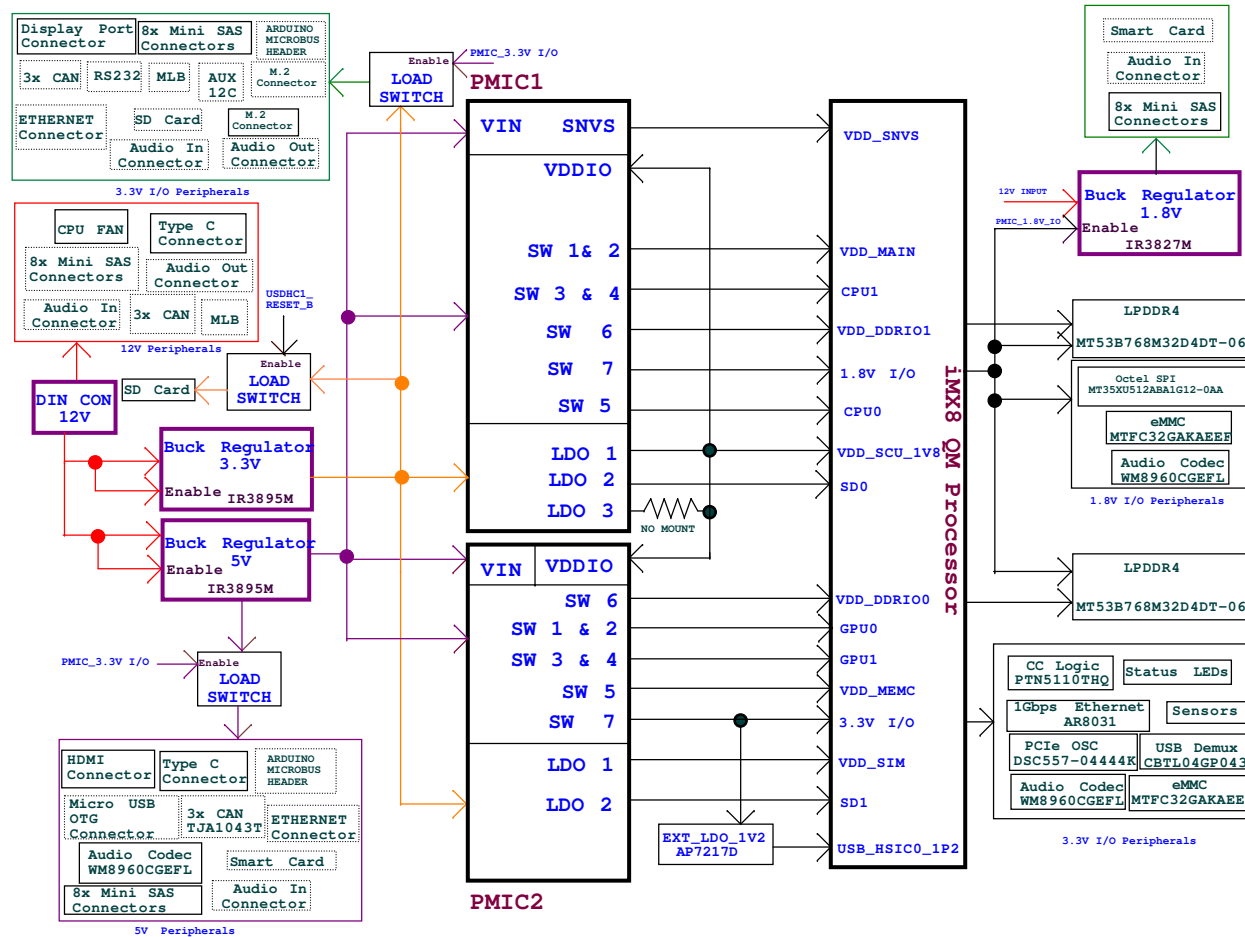
ICAP Classification: CP: _____ IUG: _____ PUB: X			
Drawing Title: <b>I.MX 8QM CPU CARD</b>			
Page Title: <b>FRONT PAGE</b>			
Size A2	Document Number	SOURCE: SCH-29420, PDF: SPF-29420	Rev C5
Date: Monday, June 08, 2020		Sheet 1 of 32	



# i.MX 8QM CPU BOARD BLOCK\_DIAGRAM



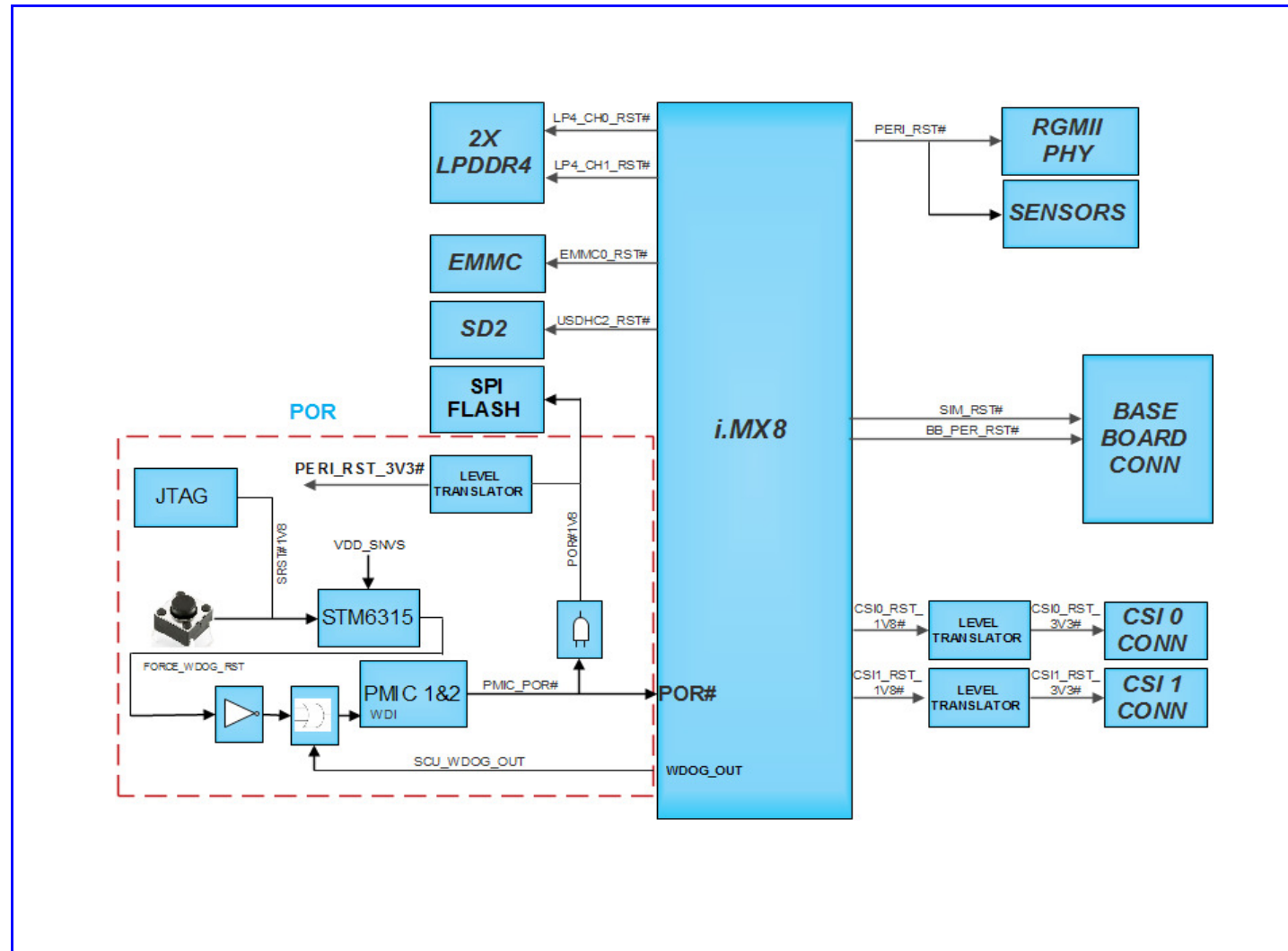
## Power Flow Diagram



Note: Dotted line represents components in Base Board.



# BLOCK DIAGRAM - RESET

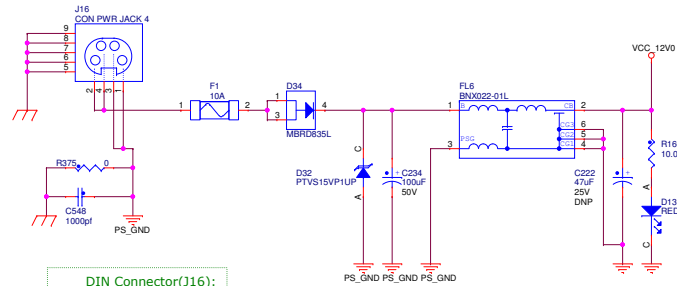


## i.MX 8QM CPU CARD I2C TABLE

DEVICE	Location	Speed (kbps)	8-bit write addresses	DEVICE ADDRESS	I2C	IO LEVEL
PMIC1	CPU	3400		0x08	PMIC I2C	1.8V
PMIC2	CPU	3400		0x09	PMIC I2C	1.8V
FXOS8700CQ	CPU	400	0x1E	0x1E	I2C0	3.3V
MPL3115A2	CPU	400	0xC0	0x60	I2C0	3.3V
FXAS21002CQR1	CPU	400	0x40	0x20	I2C0	3.3V
PTN5110	CPU	400	0xA2	0x51	I2C0	3.3V
ARDUINO/MIKROBUS	BASE				I2C0	3.3V
ENET CONN	BASE				I2C0	3.3V
MLB	BASE			0x40	I2C0	3.3V
AUDIO IN/OUT	BASE			0x90	M41.I2C	1.8V
WM8960	CPU			0x34	I2C1	1.8V
AUX I2C	BASE			0x20	I2C4	3.3V

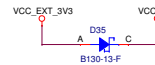
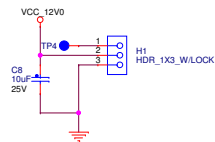
# POWER SUPPLY

## 12V DC INPUT DIN CONNECTOR

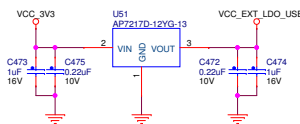


DIN Connector(J16):  
Part number: KP1X-4S-S  
Vendor : Kycon

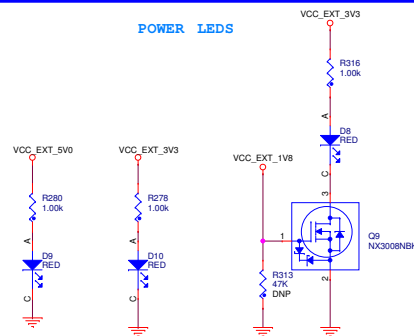
## FAN CONNECTOR



## LDO FOR 1V2:VDD\_USB\_HSIC0\_1P2

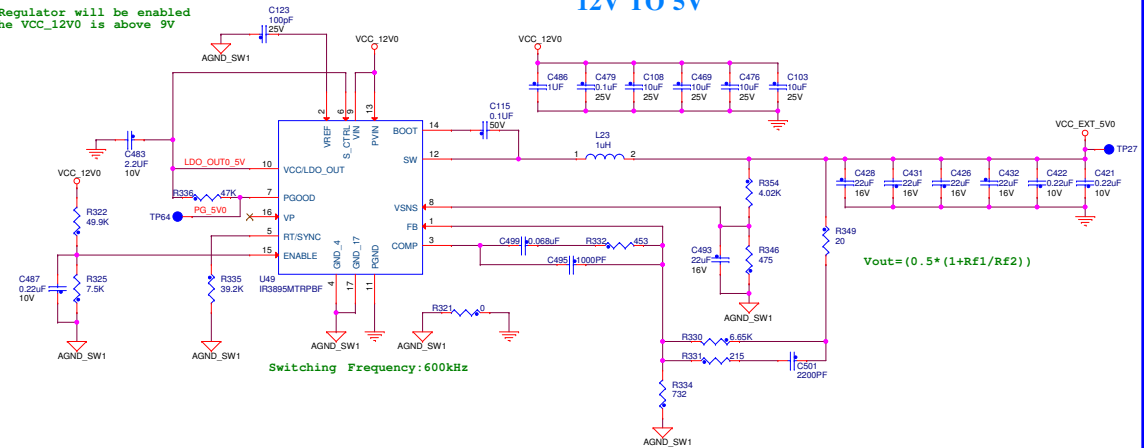


## POWER LEDS



Note: Regulator will be enabled  
once the VCC\_12V0 is above 9V

## 12V TO 5V

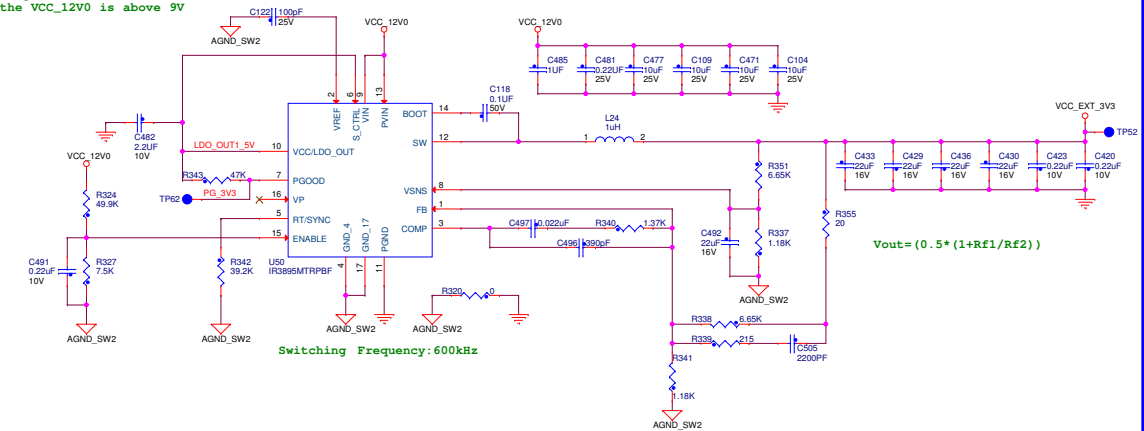


Switching Frequency:600kHz

$$V_{out} = (0.5 * (1 + R_{f1} / R_{f2}))$$

Note: Regulator will be enabled  
once the VCC\_12V0 is above 9V

## 12V TO 3.3V

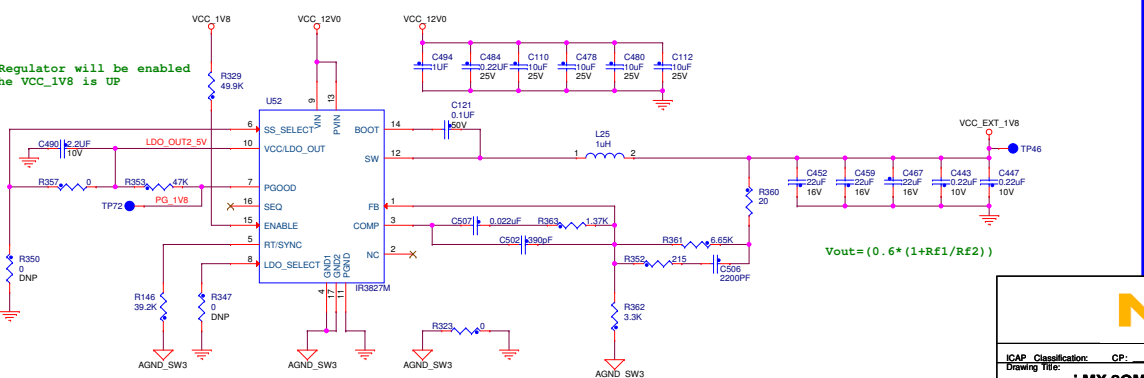


Switching Frequency:600kHz

$$V_{out} = (0.5 * (1 + R_{f1} / R_{f2}))$$

## 12V TO 1.8V

Note: Regulator will be enabled  
once the VCC\_1V8 is UP

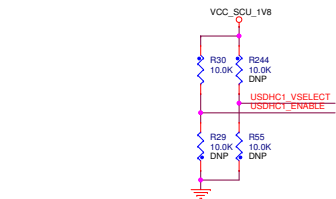
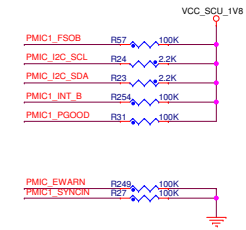
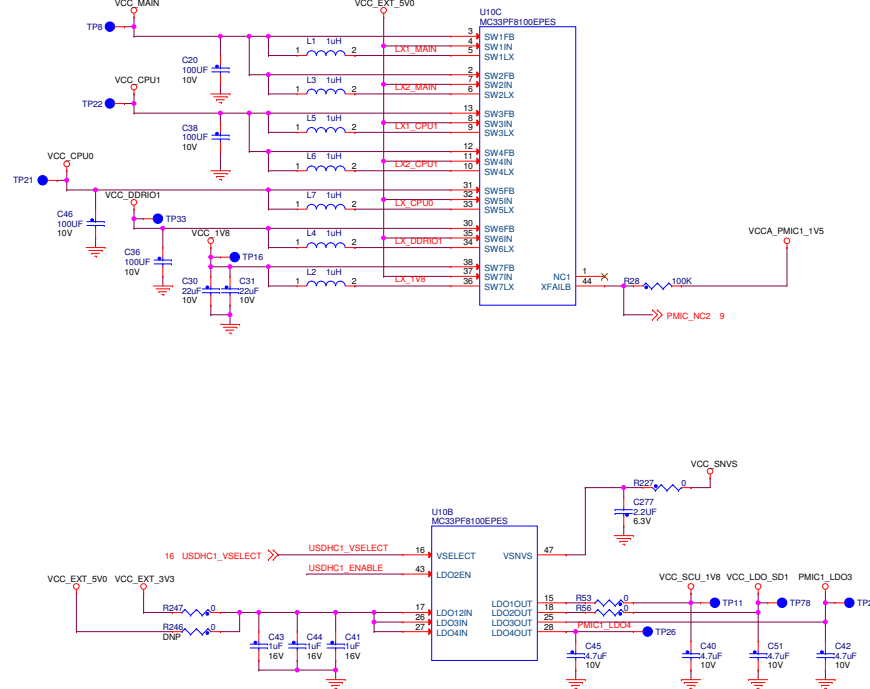
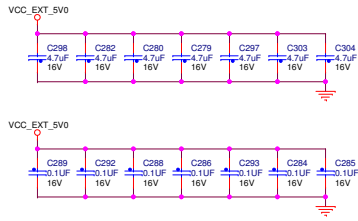
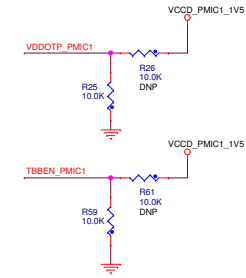
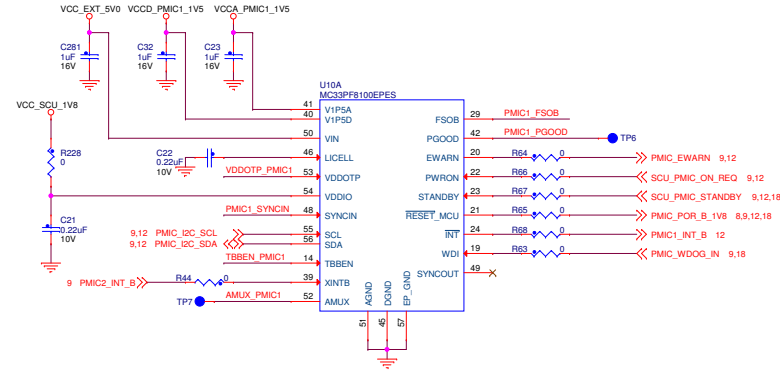


Switching Frequency:600kHz

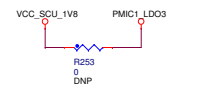
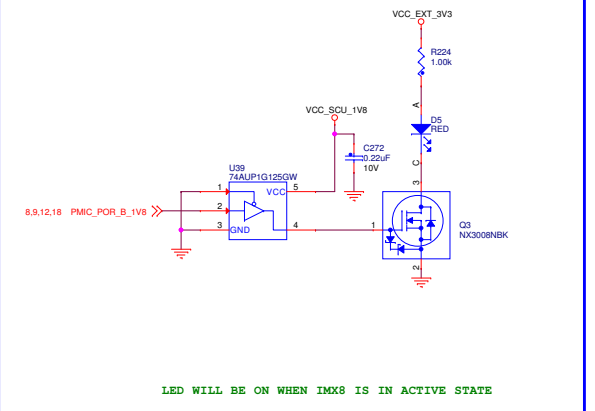
$$V_{out} = (0.6 * (1 + R_{f1} / R_{f2}))$$



# POWER SUPPLY - PMIC 1

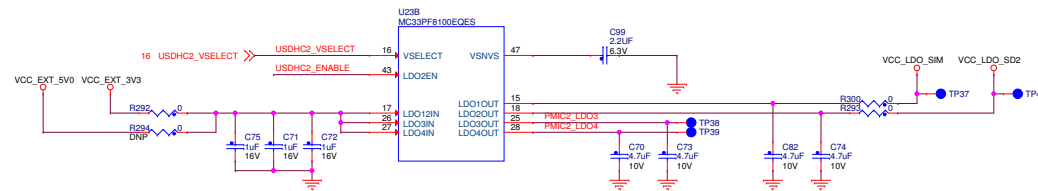
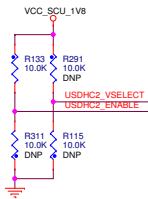
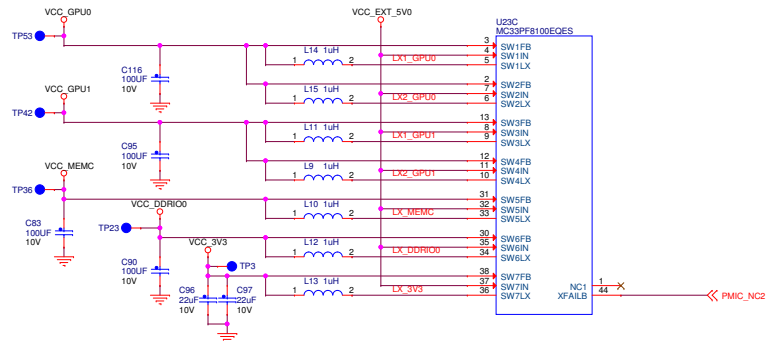
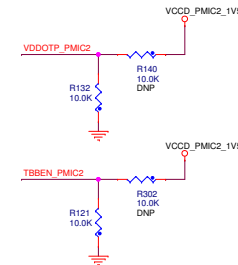
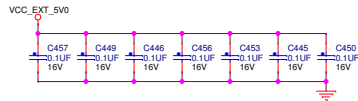
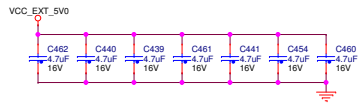
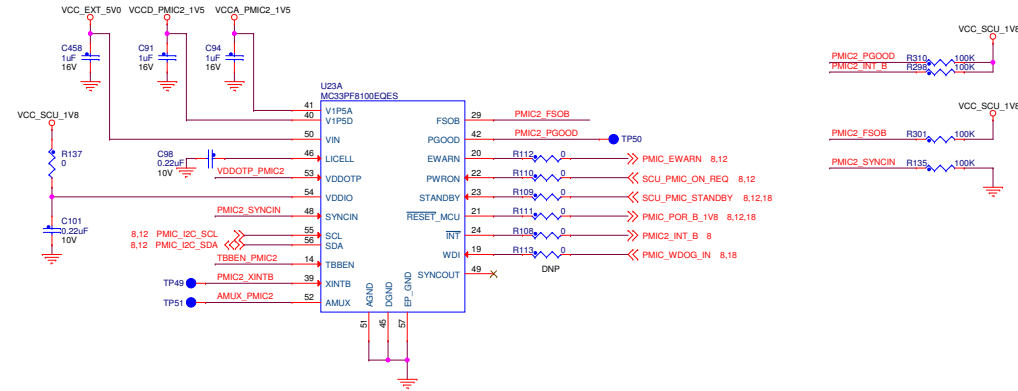


## IMX8 RESET INDICATION

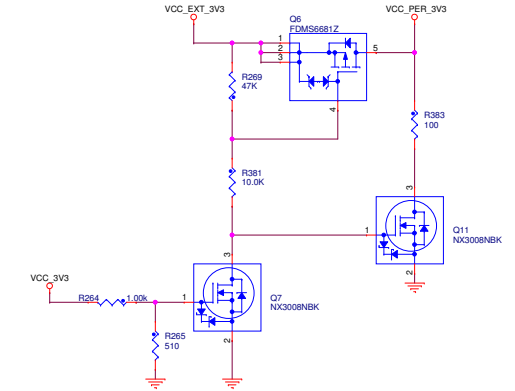




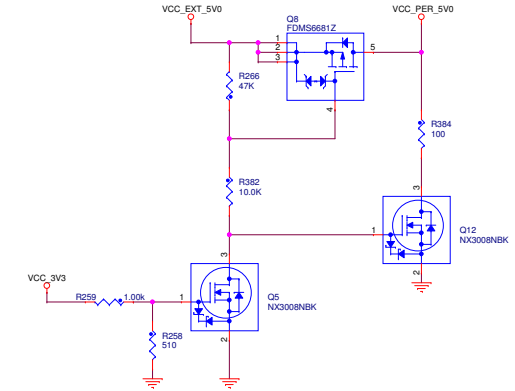
## POWER SUPPLY - PMIC 2



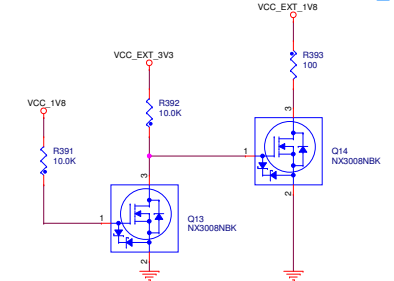
## LOAD SWITCH FOR 3V3 PERIPHERALS



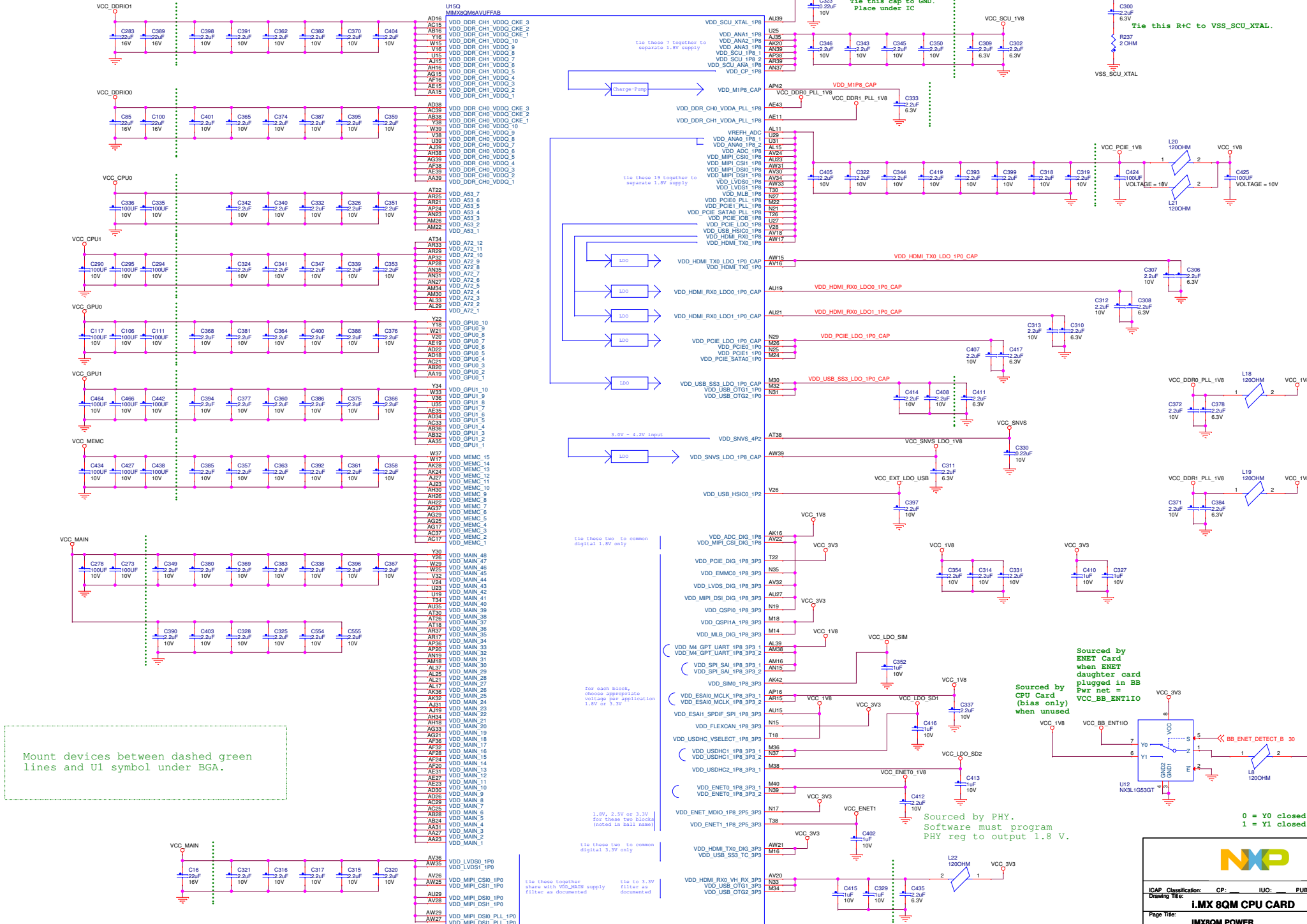
## LOAD SWITCH FOR 5V0 PERIPHERALS



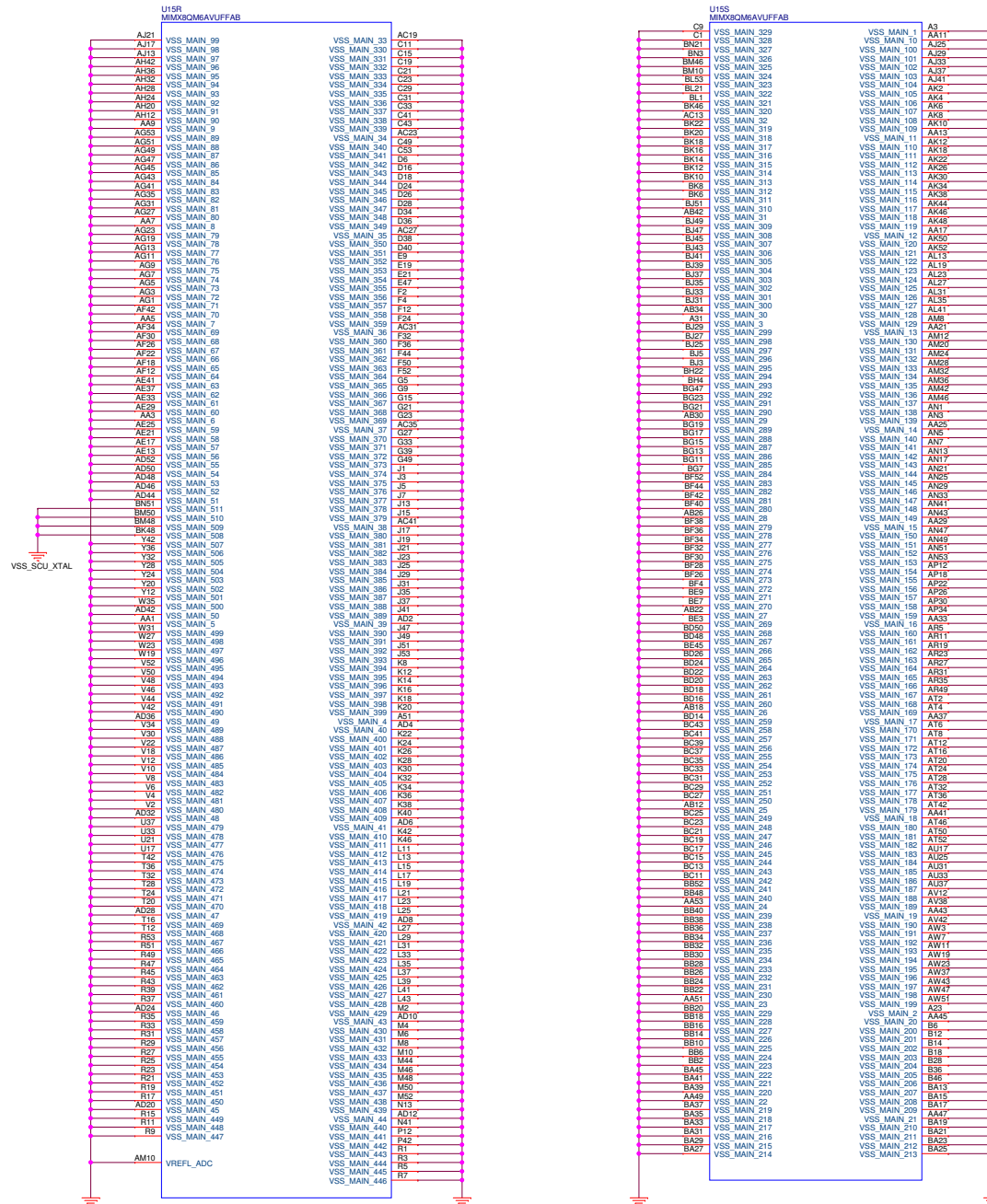
### DISCHARGE CIRCUIT FOR EXT\_1V8



# IMX8QM POWER



## IMX8QM GND SECTIONS



ICAP Classification: CP: \_\_\_\_ IUO: \_\_\_\_ PUBI: X

Drawing Title: **1. MAX CONGRU CARD**

I.MX 8QM CPU CARD

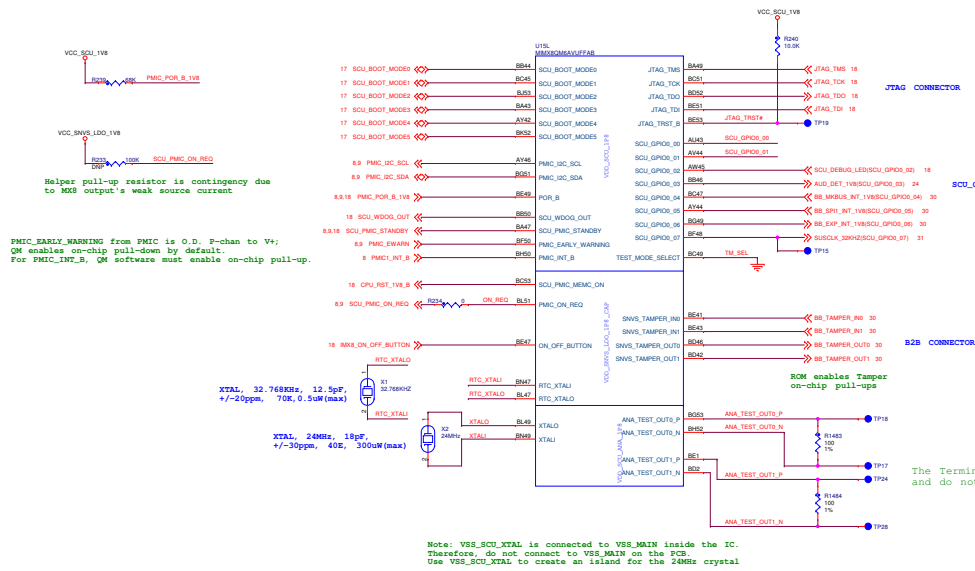
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IMX8QM GND	
Size	Document Number

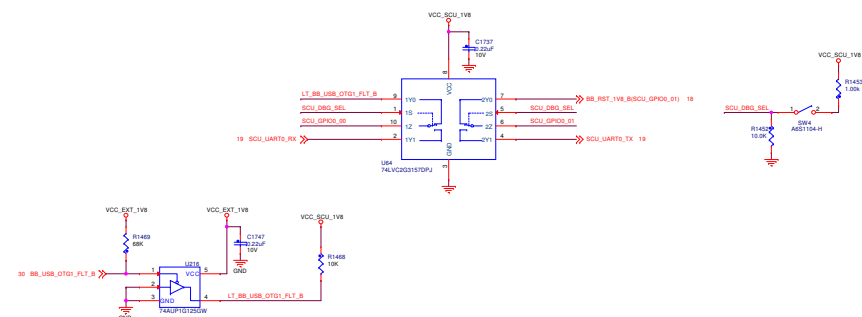
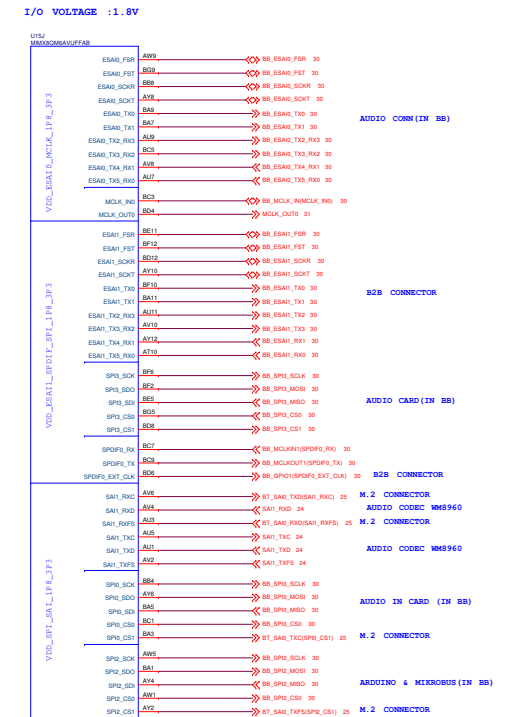
Size: A2 Document Number: SOURCE: SCH-29420, PDF: SPF-2

Date:	Monday, June 08, 2020	Sheet	11	of
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## IMX8 SECTIONS\_1

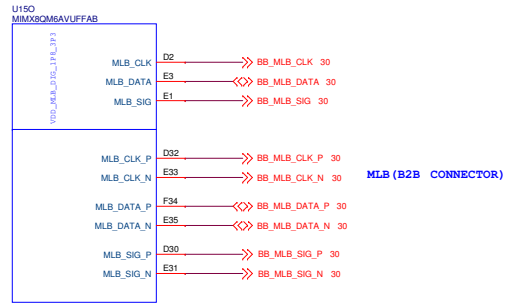


The Termination resistors (R1483 and R1484) are added for Factory use only and do not connect for customer use cases.

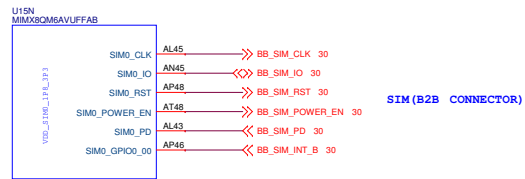
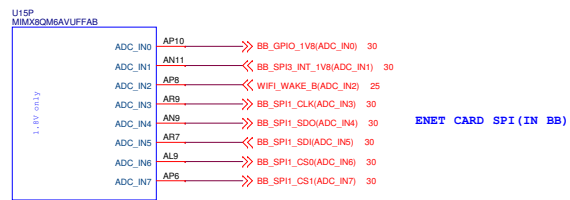


IMX8 SECTIONS\_2

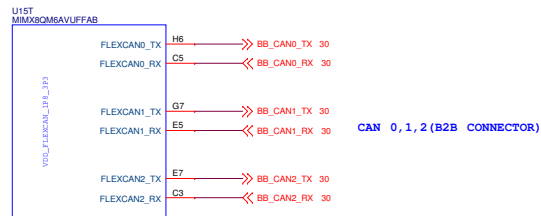
I/O VOLTAGE :3.3V



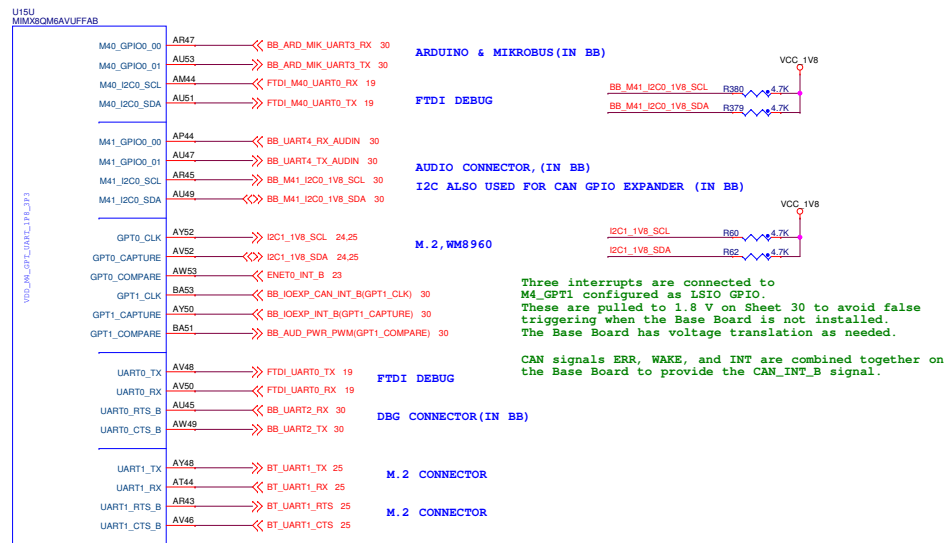
I/O VOLTAGE :1.8V



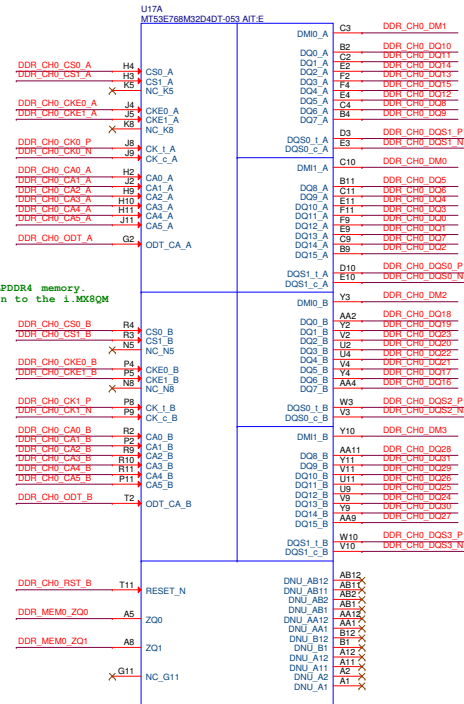
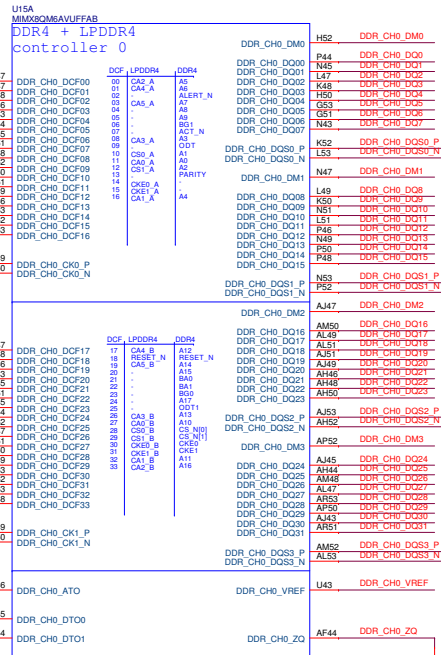
I/O VOLTAGE :3.3V



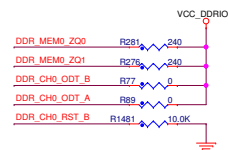
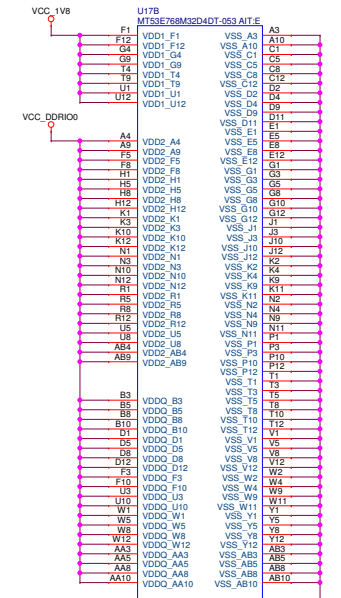
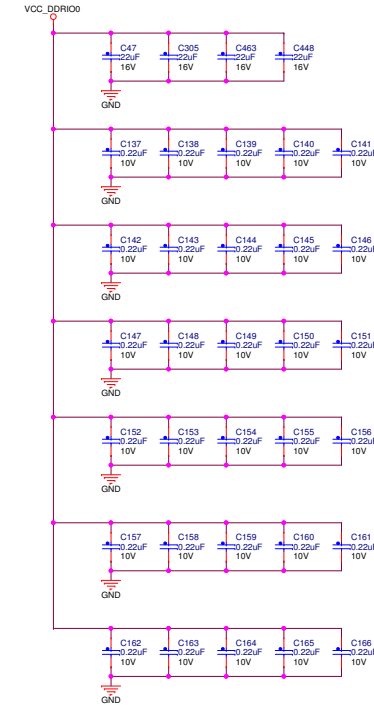
I/O VOLTAGE :1.8V



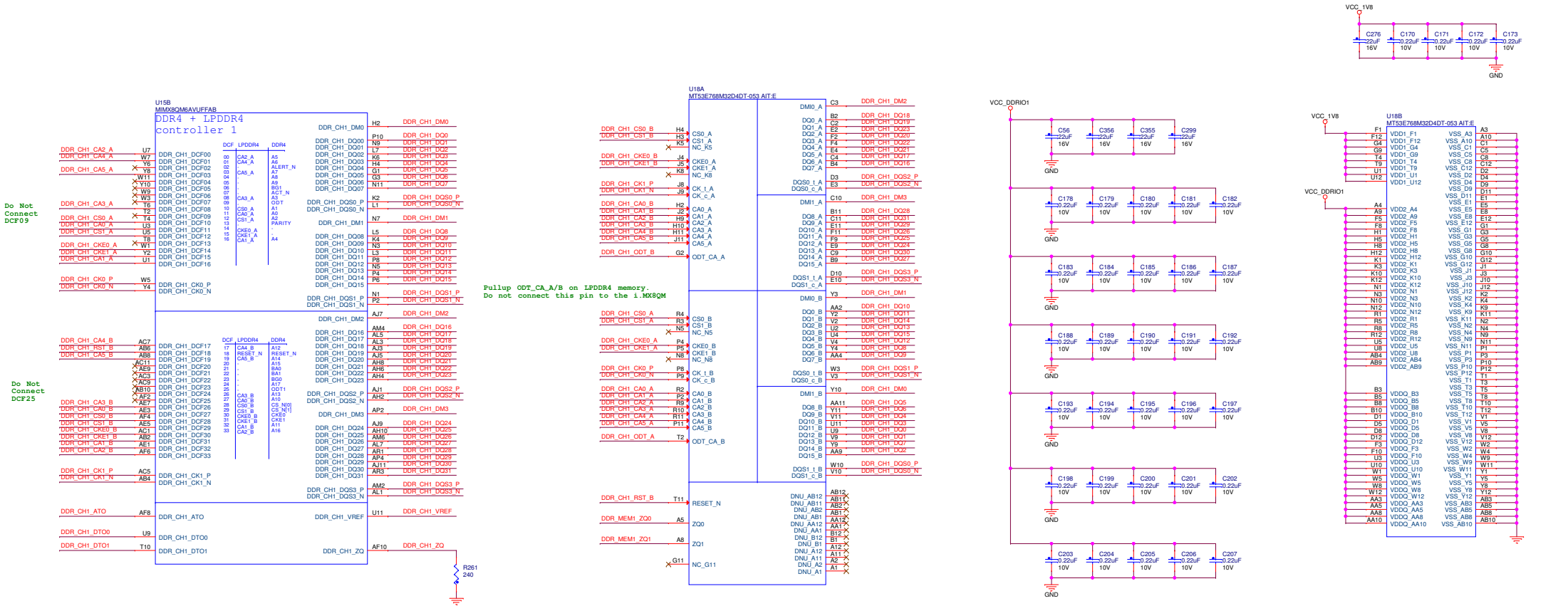
Total System DRAM = 6 Gbyte



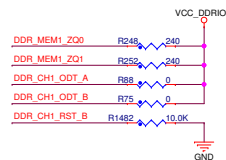
The processor requires x16 for each chip inside the DRAM package.  
The x8 configuration is not compatible.



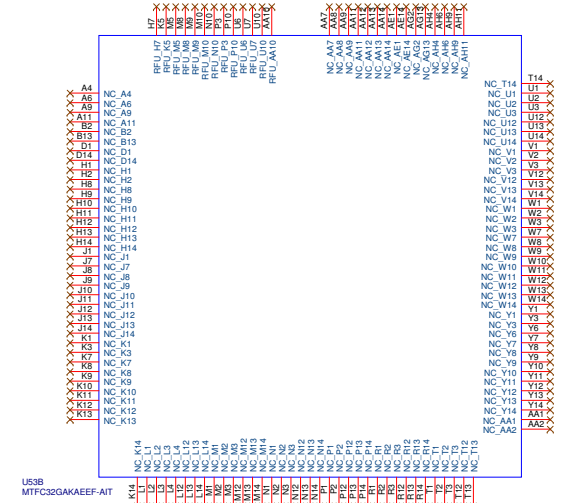
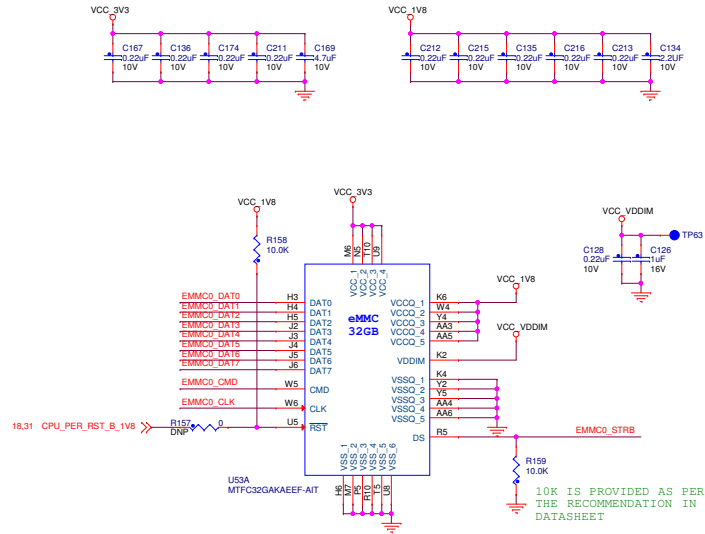
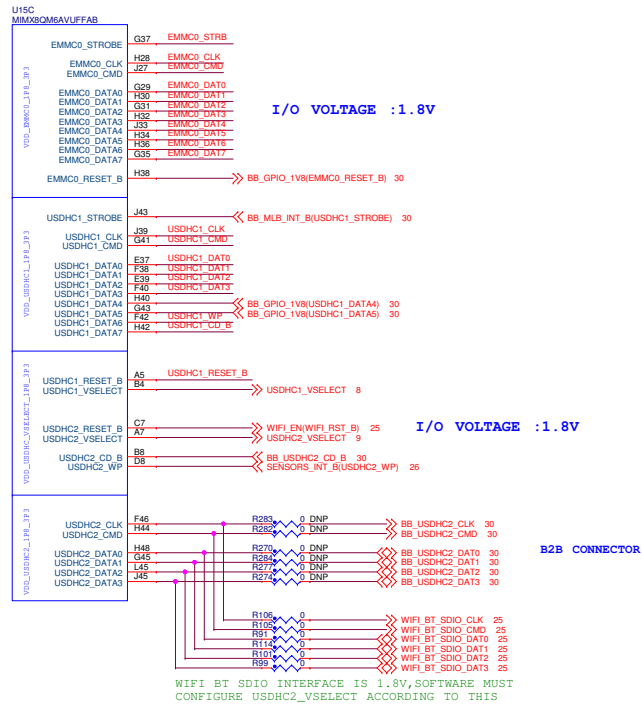
LPDDR4 DRAM 2 OF 2  
Total System DRAM = 6 Gbyte



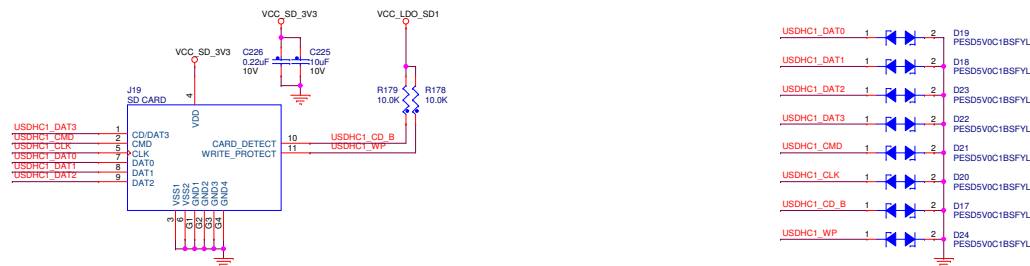
The processor requires x16 for each chip inside the DRAM package.  
The x8 configuration is not compatible.



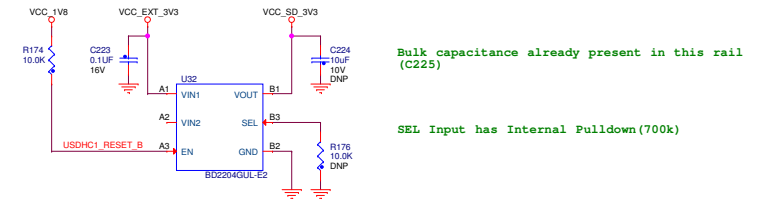




## SD CARD INTERFACE

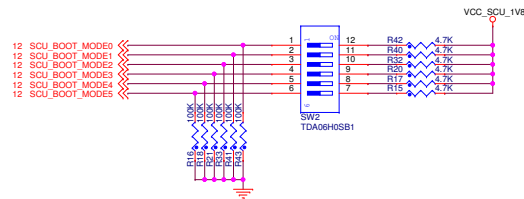


## SDXC Power Control



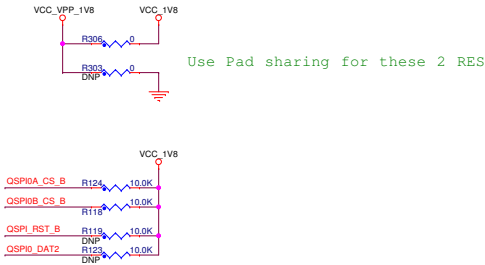
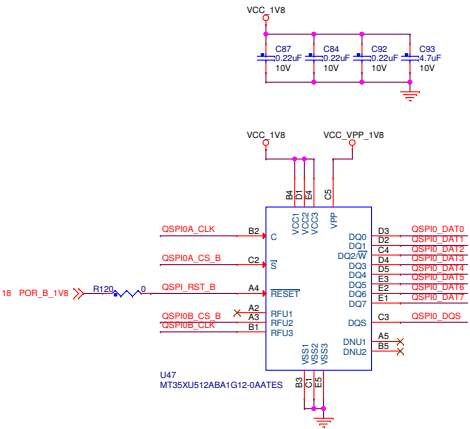
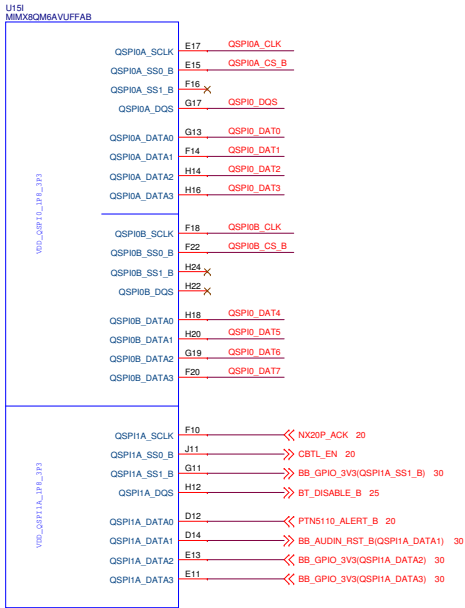


BOOT CONFIGURATIONS



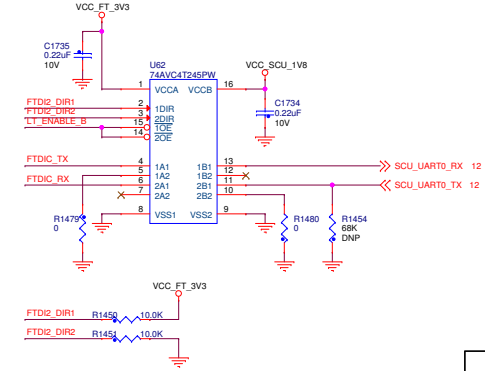
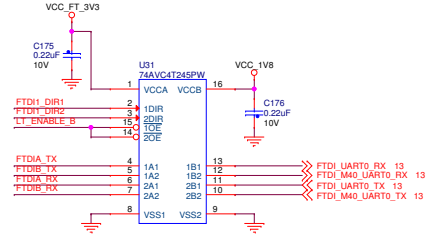
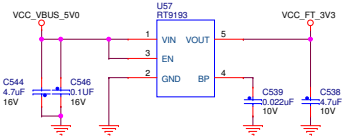
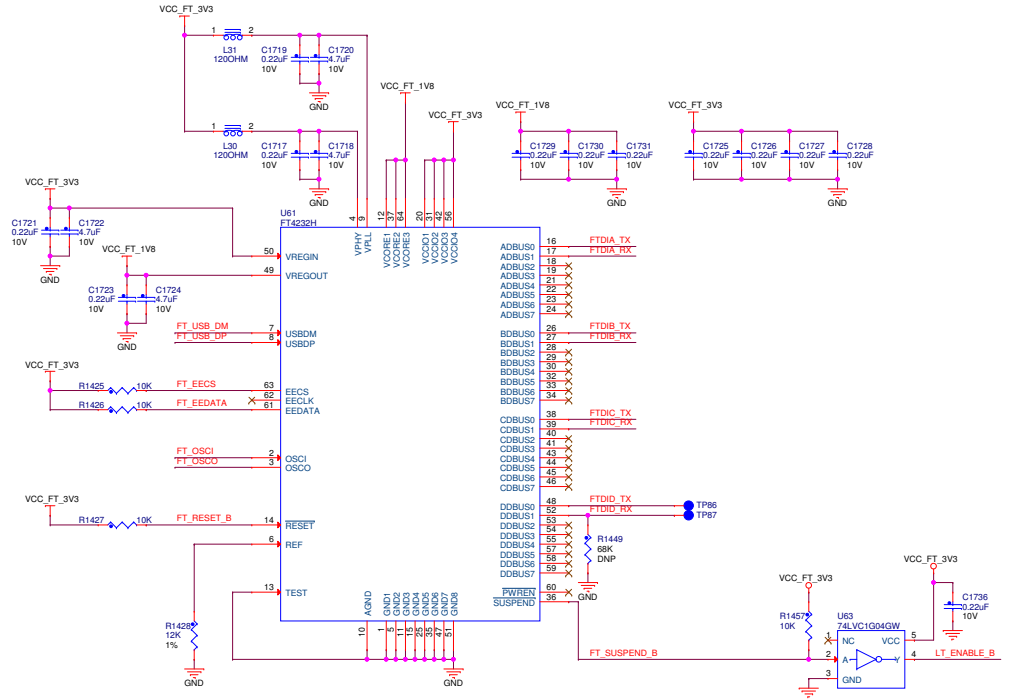
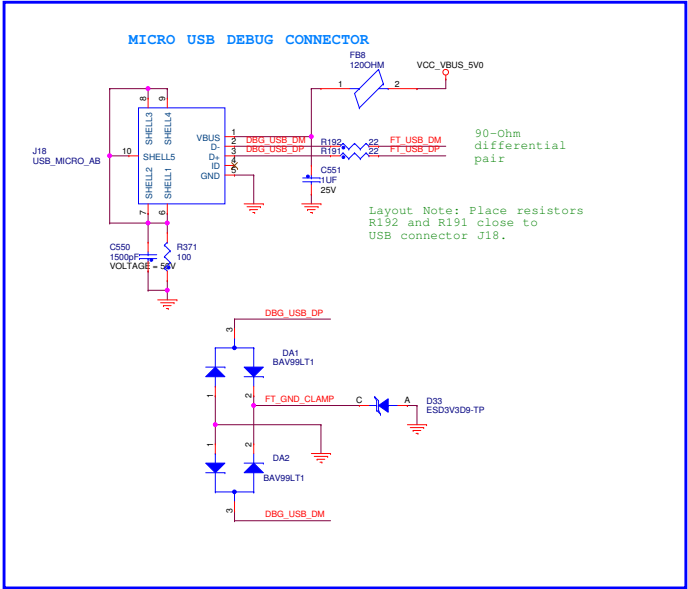
BOOT MODE						
MODE	5	4	3	2	1	0
=====						
FUSE	0	0	0	0	0	0
SERIAL BOOT	0	0	0	1	0	0
eMMC0	0	0	1	0	0	0
SD1	0	0	1	1	0	0
Octal SPI	0	1	1	0	0	0

OCTAL/XSPI/QSPI FLASH



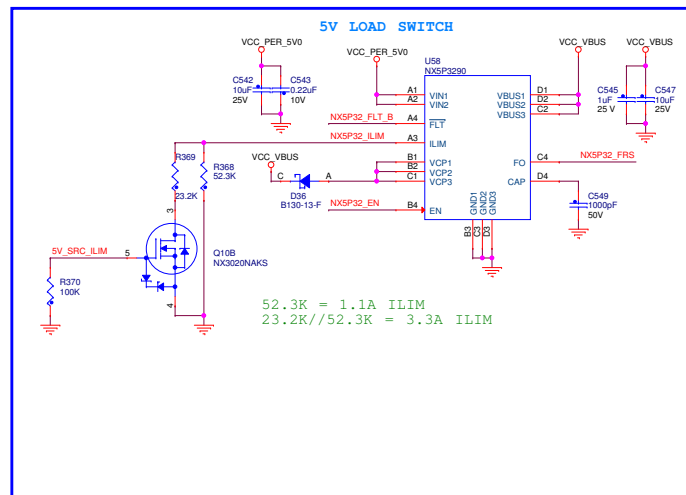


DEBUG UART-USB



VCC\_3V3

Resistor	Value	Signal
R299	10.0K	USB_OTG2_ID
R190	47K	NX5P32_FLT_B
R365	100K	NX20P_ACK
R189	10.0K	PTN5110_ALERT_B

[illegible]

The schematic shows the I2C interface for the LIS37 sensor. The sensor's I2C pins are connected to the microcontroller's I2C pins. Power is supplied by VCC\_3V3 and VCC\_VBUS. Signal lines include NXSP2\_FRS, NXSP2\_FLT\_B, and PTNST\_DBG\_ACC. A pull-up resistor is connected to the I2C line.

**I2C Address: "1010001s"**

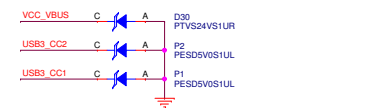
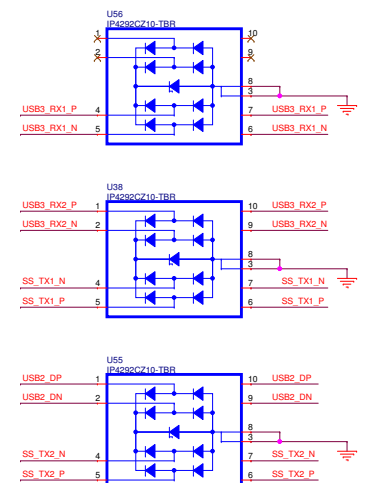
Pin connections for the sensor:

- 1: NXSP2\_FRS
- 2: NXSP2\_FLT\_B
- 3: PTNST\_DBG\_ACC
- 4: VCC\_3V3
- 5: VCC\_VBUS
- 6: I2C\_SDA
- 7: I2C\_SCL
- 8: GND
- 9: I2C\_ADDR
- 10: I2C\_ADDR
- 11: I2C\_ADDR
- 12: I2C\_ADDR
- 13: I2C\_ADDR
- 14: I2C\_ADDR
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- 284: I2C\_ADDR
- 285: I2C\_ADDR

I2C ADDRESS SELECTION	
ADDR PIN	ADDRESS
=====	=====
	1010000x
K PULL UP TO BYPASS	1010011x
CONNECTED	1010010x
PULL UP TO BYPASS	1010001x

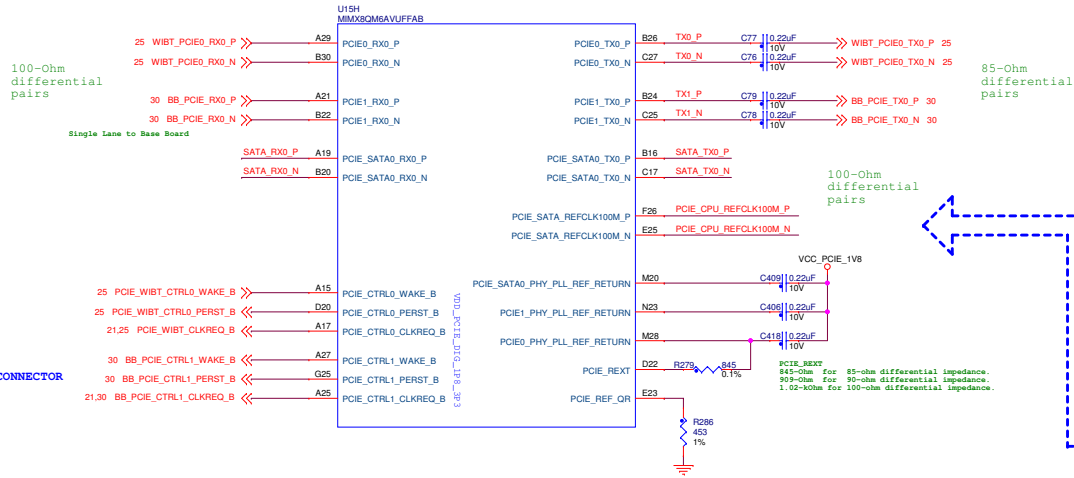
[illegible]

OTG1 Can be connected to M.2 Connector  
or Baseboard USB2.0 port using these resistor options.

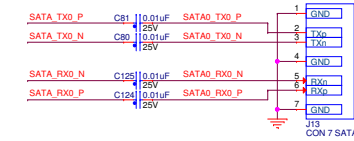


## PCIe & SATA

I/O VOLTAGE : 3.3V



## SATA CONNECTOR

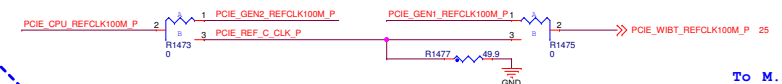


M.2 Connector on CPU Card has two PCIe Clock options:  
(Set resistor strapping as per table)

1. Processor (NXP experimental use only; not recommended for customer use)
2. External Clock generator (By default)

M.2 Connector on Base Card has PCIe Clock Option only from External clock generator. (Set resistor strapping as per table)

From Ext Osc U26

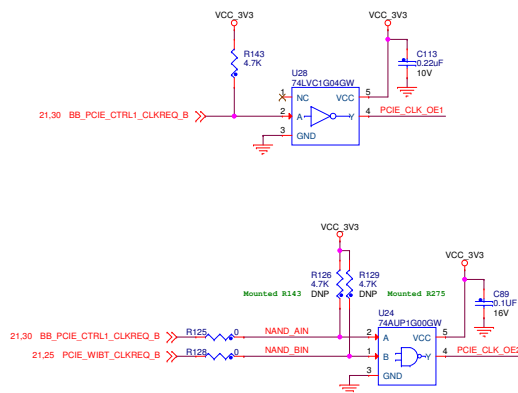


To M.2 Connector

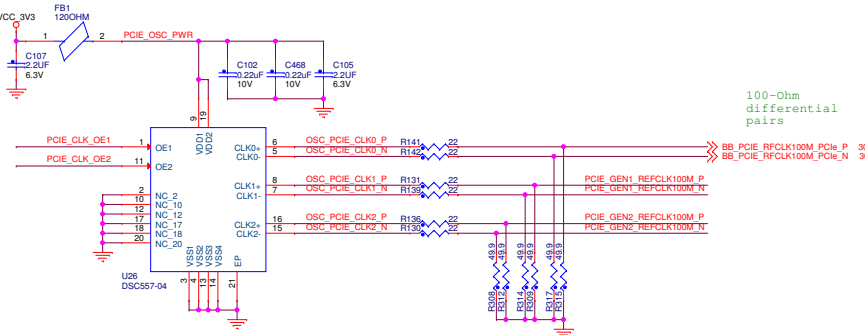
From Ext Osc U26



## PCIe CLOCK ENABLE LOGIC



## PCIe 100MHz OSCILLATOR



DSC557 has internal 40kOhm pullup on OE1 and OE2.  
Default always ON for DSC557 Osc.

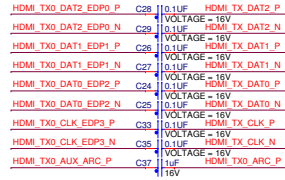
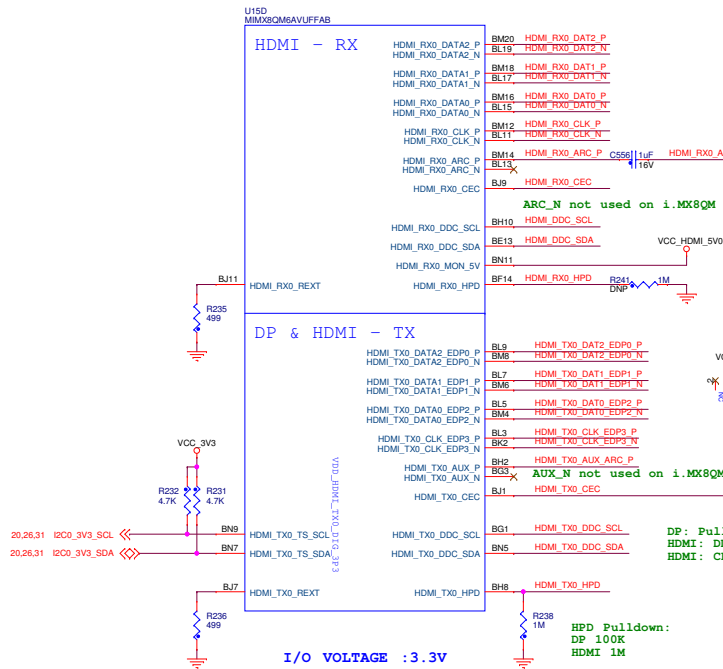
## CLOCK CONFIG

OE1	OE2	CLK0	CLK1	CLK2
0	0	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	EN	EN
1	0	EN	Hi-Z	Hi-Z
1	1	EN	EN	EN

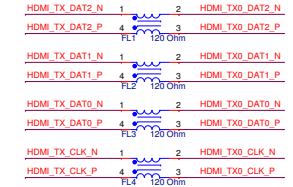
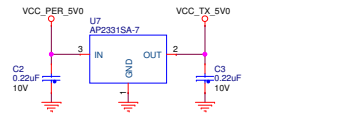
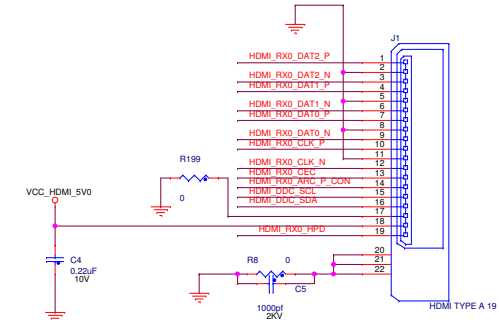
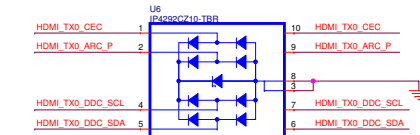
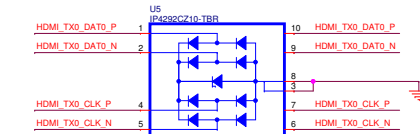
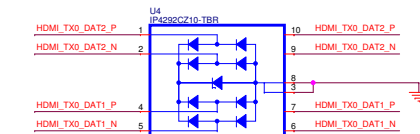
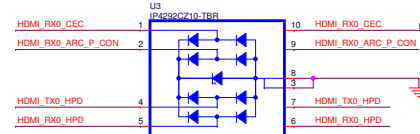
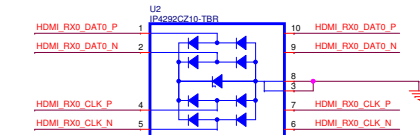
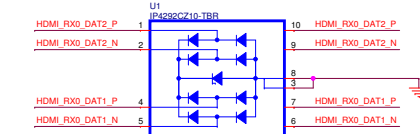
	Option Resistors	Clock Source	
		Processor	Clock Generator
M.2 Connector on CPU Card	R1473	POS B	POS A
	R1474	POS B	POS A
	R1475	POS B	POS A
	R1476	POS B	POS A
	R128	DNP	MOUNT
	R129	MOUNT	DNP
	R130	DNP	MOUNT
	R131	DNP	MOUNT
	R136	DNP	MOUNT
M.2 Connector on Base Card	R139	DNP	MOUNT
	R1473	NA	POS A
	R1474	NA	POS A
	R1475	NA	POS A
	R1476	NA	POS A
	R128	NA	MOUNT
	R129	NA	DNP
	R130	NA	MOUNT
	R131	NA	MOUNT
	R136	NA	MOUNT
	R139	NA	MOUNT



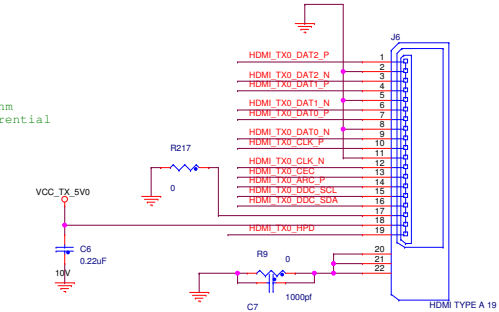
# HDMI TX & RX



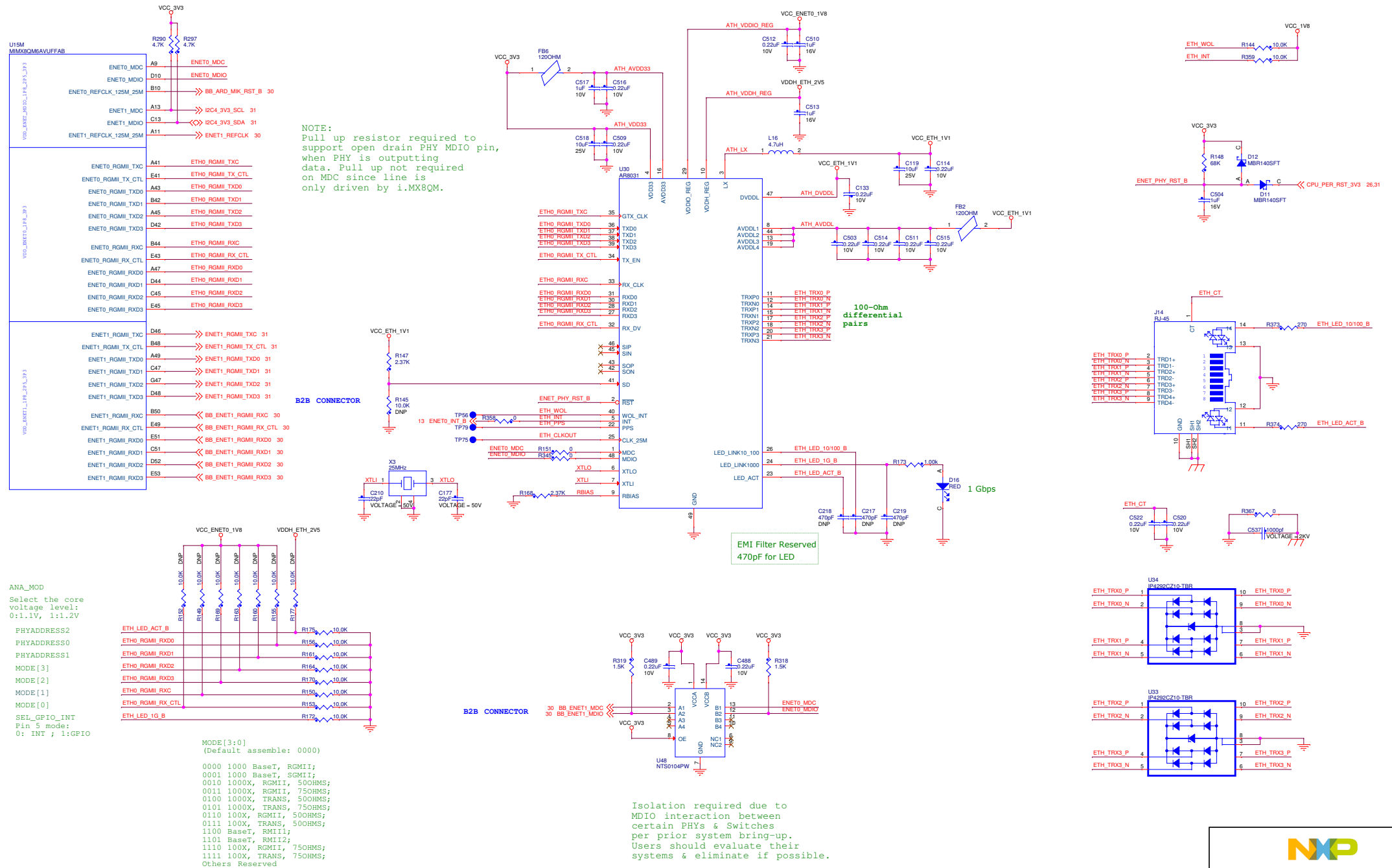
DP: Pulldown unused DDC and CEC pins  
HDMI: DDC requires 2K pullup to 5V  
HDMI: CEC requires 27K pullup to 3V3 with blocking diode



100-Ohm differential pairs

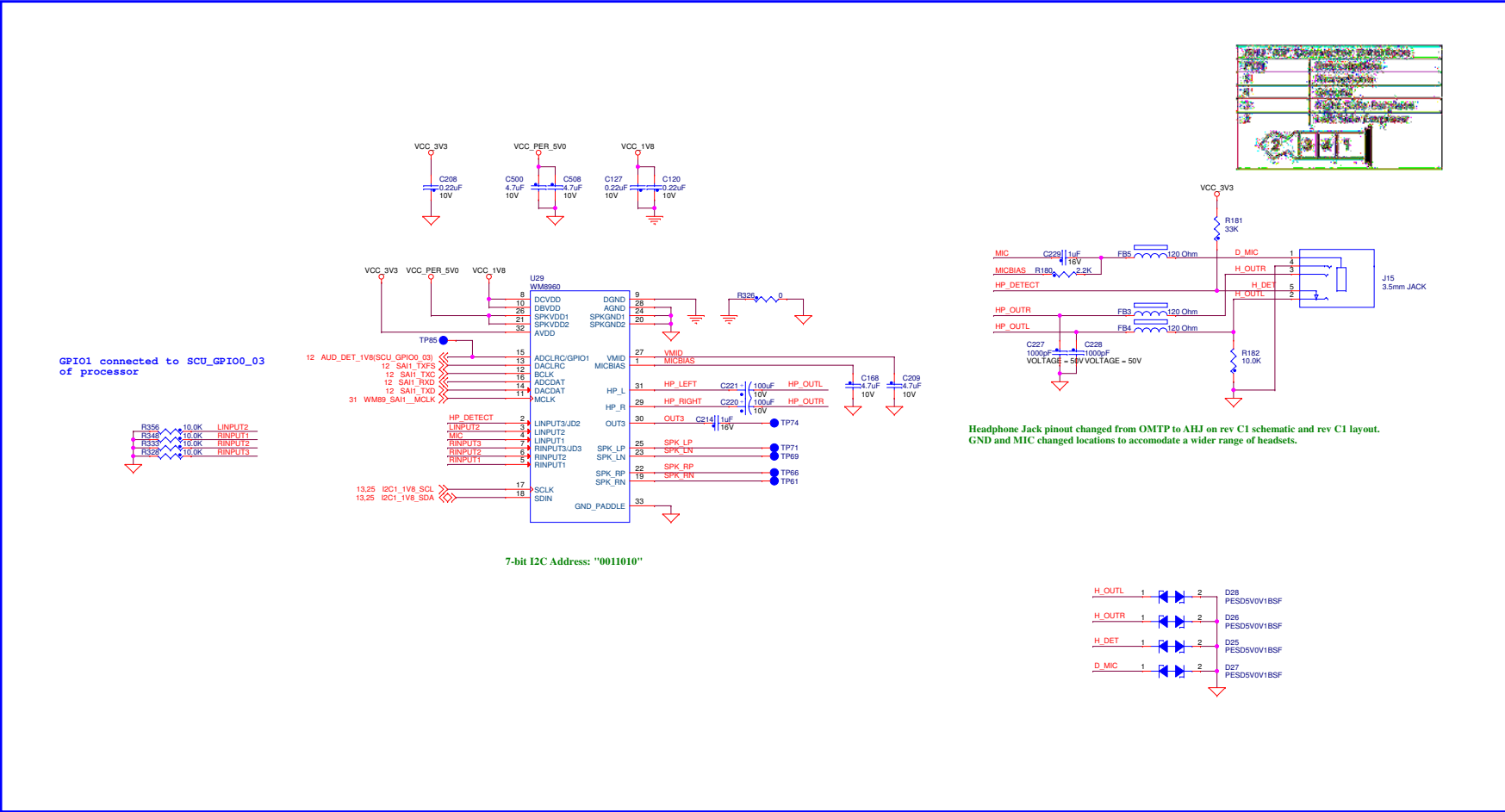


## 1 Gbps ETHERNET PHY



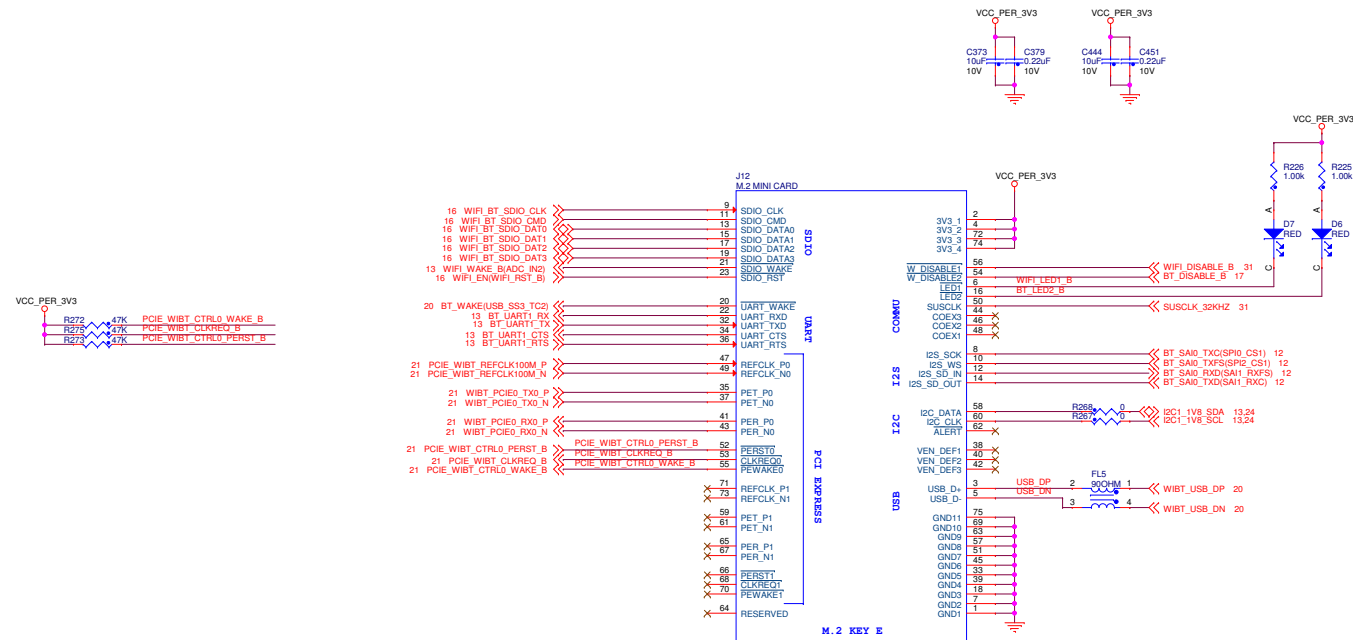
Isolation required due to MDIO interaction between certain PHYs & Switches per prior system bring-up. Users should evaluate their systems & eliminate if possible.

AUDIO CODEC WM8960





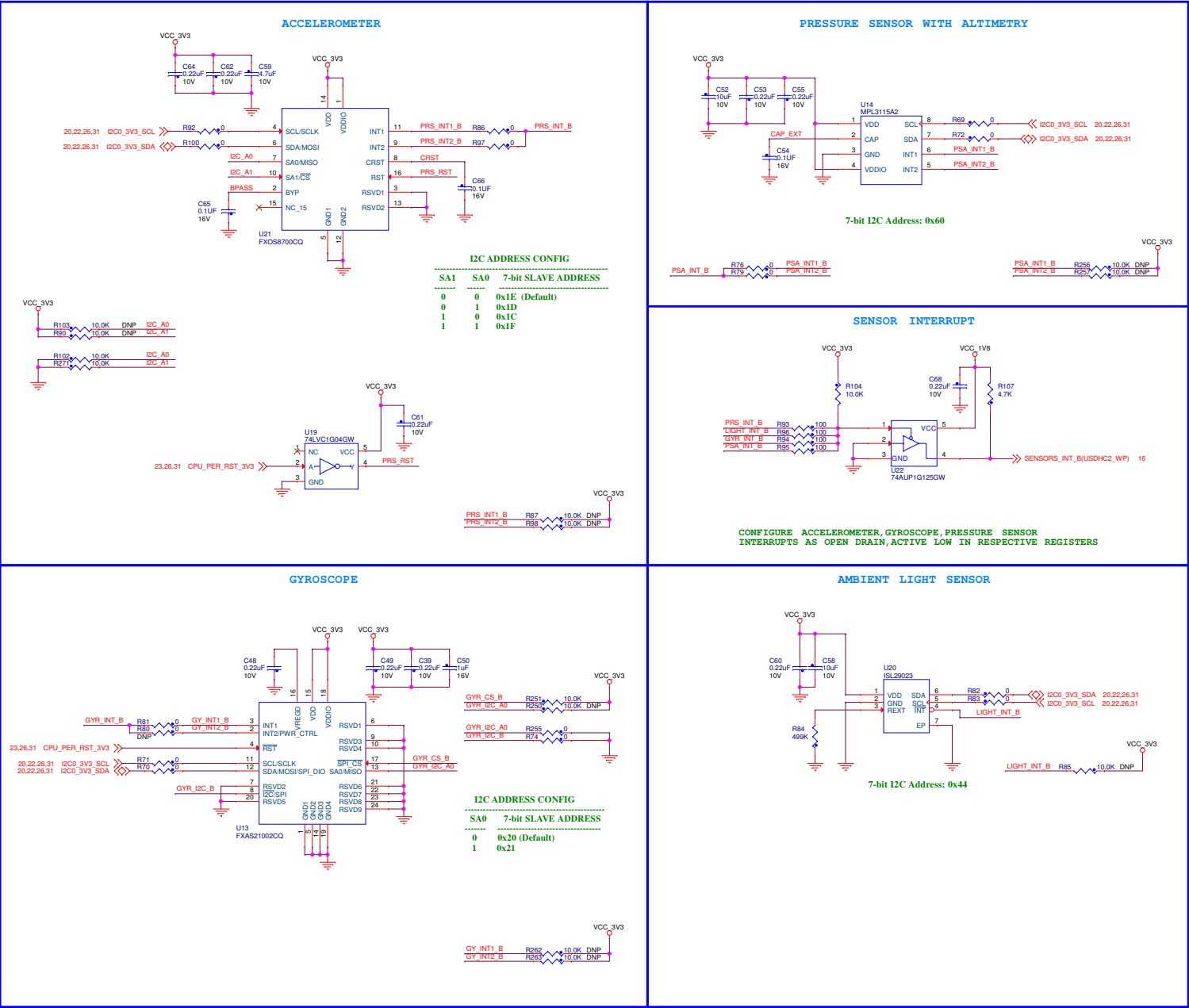
## WIFI\_BLUETOOTH -M.2 CONNECTOR E-KEY

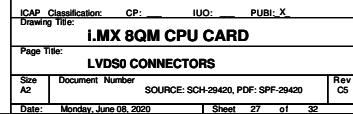


Add On Card used will be M.2 with E-Key Type 30x30 Dimension.

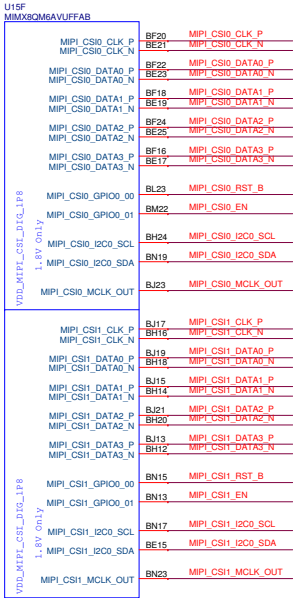
Information on compatible cards is provided on the [nxp.com](http://nxp.com) website.

SENSORS



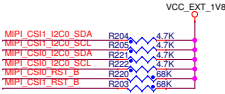
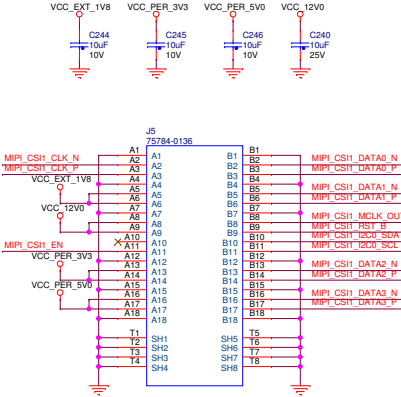
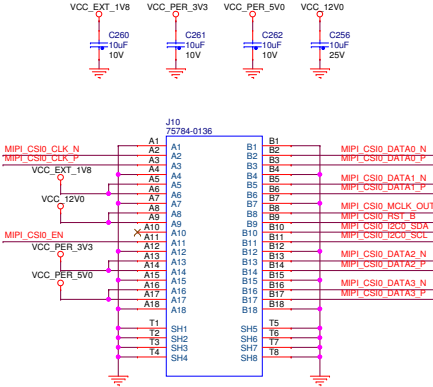
[illegible]

MIPI CSI CONNECTORS



100-ohm differential pairs

100-ohm differential pairs

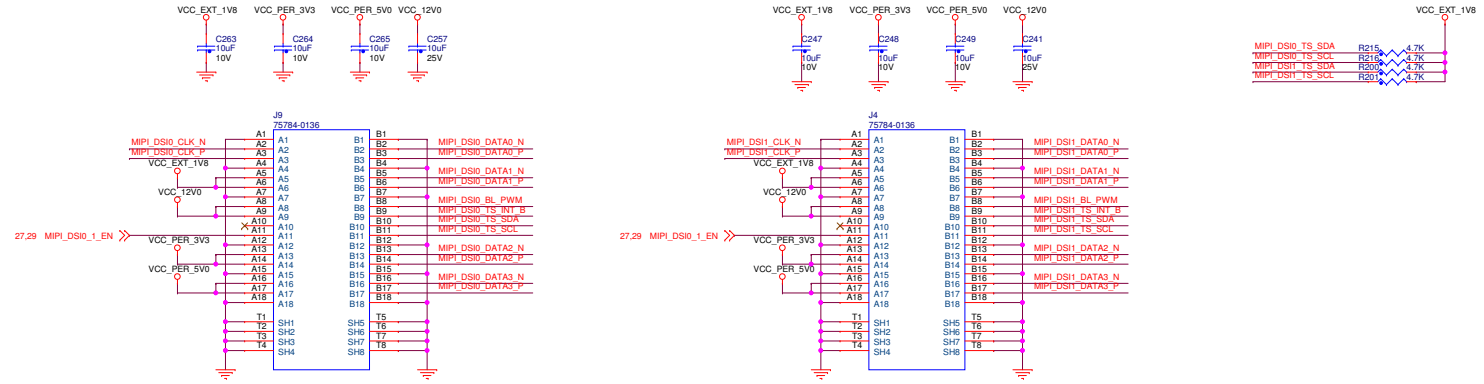


MIPI DSI CONNECTORS

VDD_MIP1_DSI1_D1G1_IP8_3P3	U15G	
	MMXG06AVUFFAB	
	MIPI_DSI0_CLK_P	BL27 MIPI_DSI0_CLK_P
	MIPI_DSI0_CLK_N	BN27 MIPI_DSI0_CLK_N
	MIPI_DSI0_DATA0_P	BK28 MIPI_DSI0_DATA0_P
	MIPI_DSI0_DATA0_N	BM28 MIPI_DSI0_DATA0_N
	MIPI_DSI0_DATA1_P	BK26 MIPI_DSI0_DATA1_P
	MIPI_DSI0_DATA1_N	BM26 MIPI_DSI0_DATA1_N
	MIPI_DSI0_DATA2_P	BL29 MIPI_DSI0_DATA2_P
	MIPI_DSI0_DATA2_N	BN29 MIPI_DSI0_DATA2_N
	MIPI_DSI0_DATA3_P	BL25 MIPI_DSI0_DATA3_P
	MIPI_DSI0_DATA3_N	BN25 MIPI_DSI0_DATA3_N
	MIPI_DSI0_GPIO0_00	BD30 MIPI_DSI0_BL_PWM
	MIPI_DSI0_GPIO0_01	BD28 MIPI_DSI0_TS_INT_B
VDD_MIP1_DSI1_D1G1_IP8_3P3	MIPI_DSI0_I2C0_SCL	BE29 MIPI_DSI0_TS_SCL
	MIPI_DSI0_I2C0_SDA	BE31 MIPI_DSI0_TS_SDA
	MIPI_DSI1_CLK_P	BG31 MIPI_DSI1_CLK_P
	MIPI_DSI1_CLK_N	BH30 MIPI_DSI1_CLK_N
	MIPI_DSI1_DATA0_P	BG33 MIPI_DSI1_DATA0_P
	MIPI_DSI1_DATA0_N	BH32 MIPI_DSI1_DATA0_N
	MIPI_DSI1_DATA1_P	BG29 MIPI_DSI1_DATA1_P
	MIPI_DSI1_DATA1_N	BH28 MIPI_DSI1_DATA1_N
	MIPI_DSI1_DATA2_P	BG35 MIPI_DSI1_DATA2_P
	MIPI_DSI1_DATA2_N	BH34 MIPI_DSI1_DATA2_N
	MIPI_DSI1_DATA3_P	BG27 MIPI_DSI1_DATA3_P
	MIPI_DSI1_DATA3_N	BH26 MIPI_DSI1_DATA3_N
	MIPI_DSI1_GPIO0_00	BM24 MIPI_DSI1_BL_PWM
	MIPI_DSI1_GPIO0_01	BK24 MIPI_DSI1_TS_INT_B
	MIPI_DSI1_I2C0_SCL	BE27 MIPI_DSI1_TS_SCL
	MIPI_DSI1_I2C0_SDA	BG25 MIPI_DSI1_TS_SDA

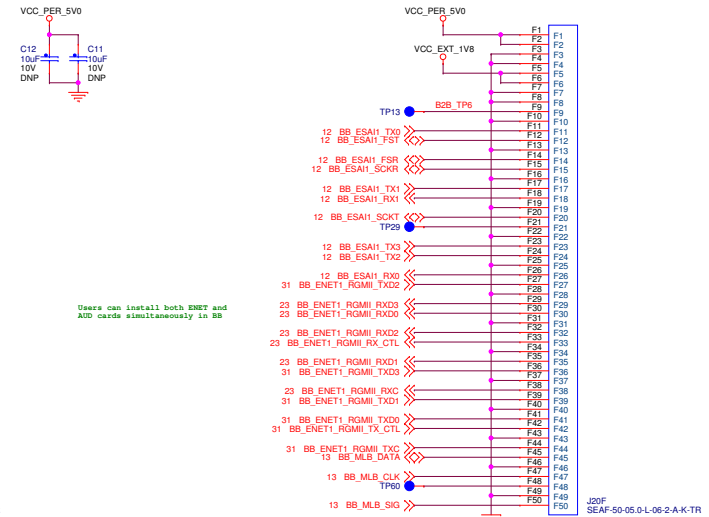
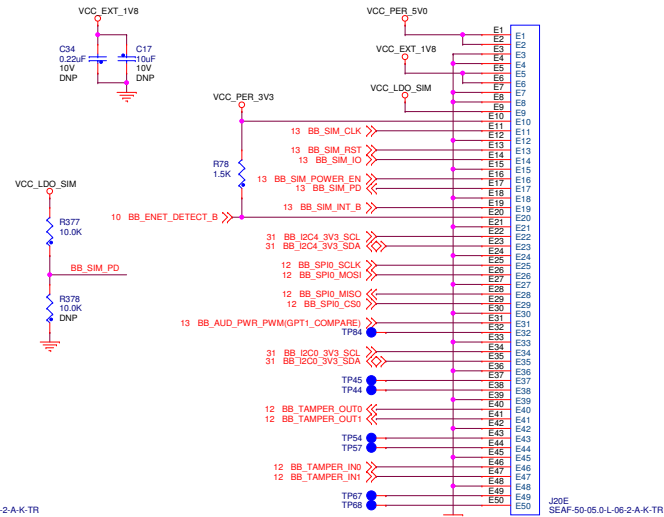
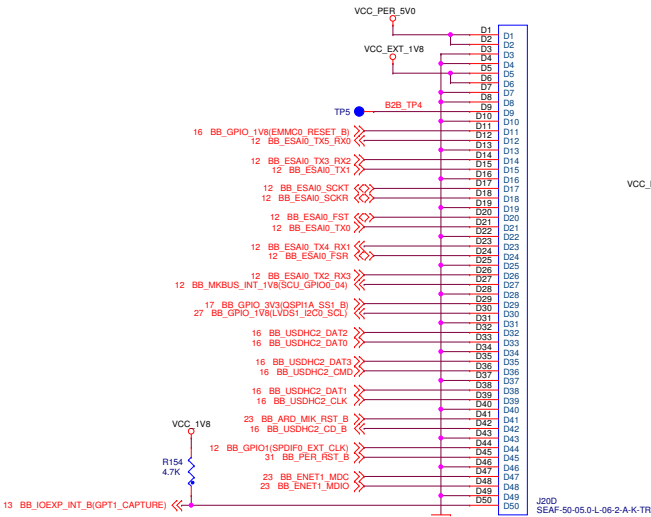
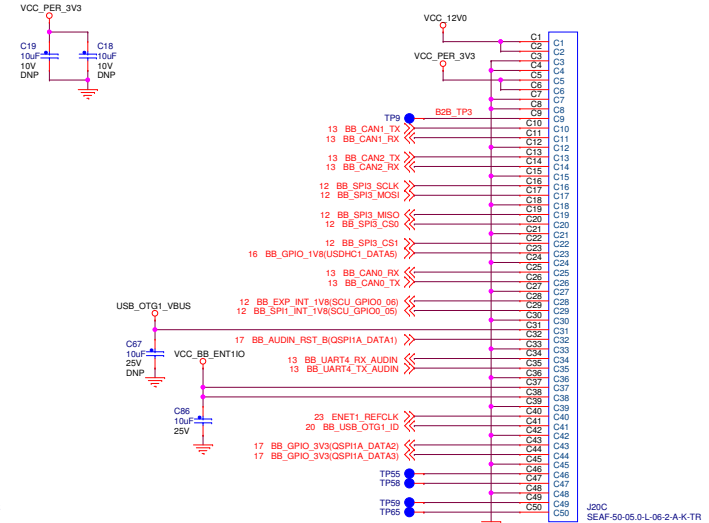
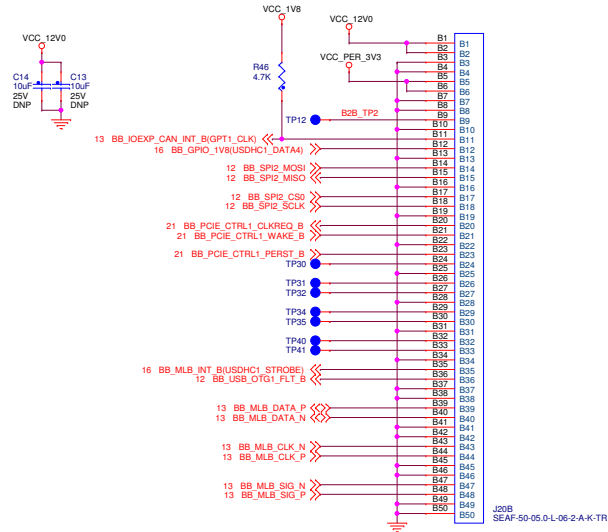
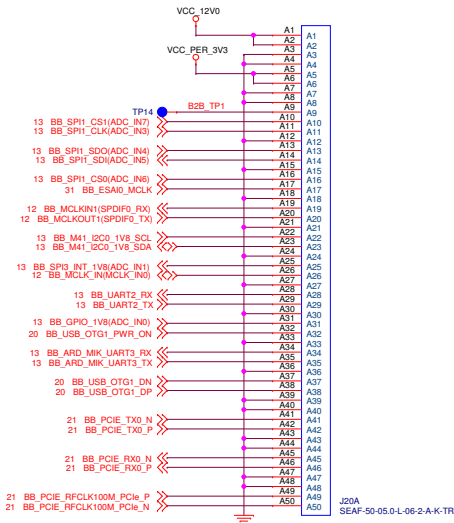
100-Ohm differential pairs

100-Ohm differential pairs



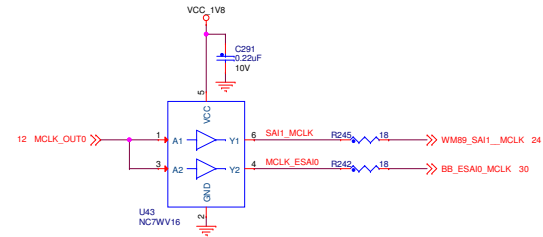
## B2B CONNECTOR

EACH PIN CAPABLE OF 1.2A

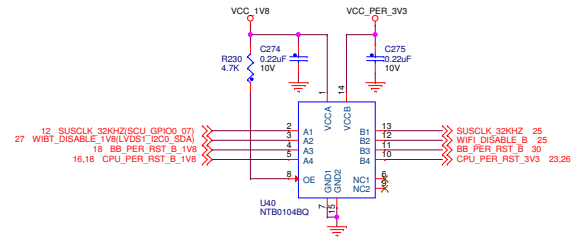


SOME PINS ARE RESERVED FOR MAKING COMMON BASE BOARD FOR QM AND QXP

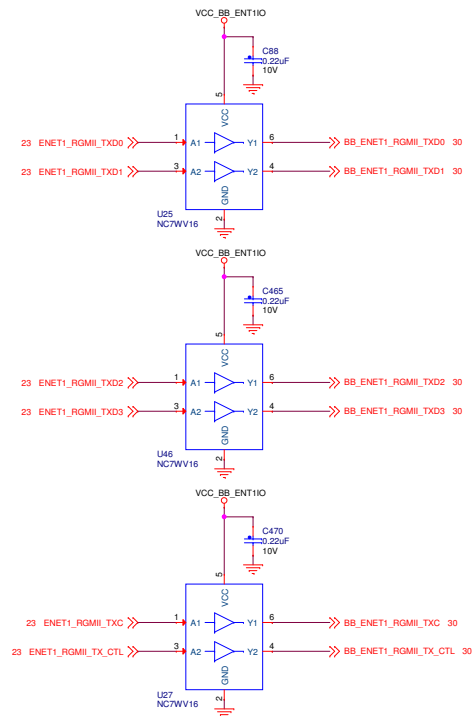
## MCLK CLOCK DRIVERS FOR BASE BOARD FAN OUT



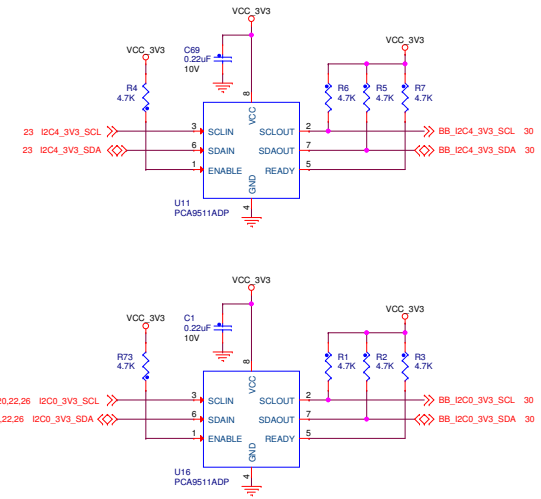
## LEVEL TRANSLATOR



## ETHERNET TX BUFFERS FOR BASEBOARD



## I2C BUFFERS FOR BASE BOARD



MISCELLANEOUS

