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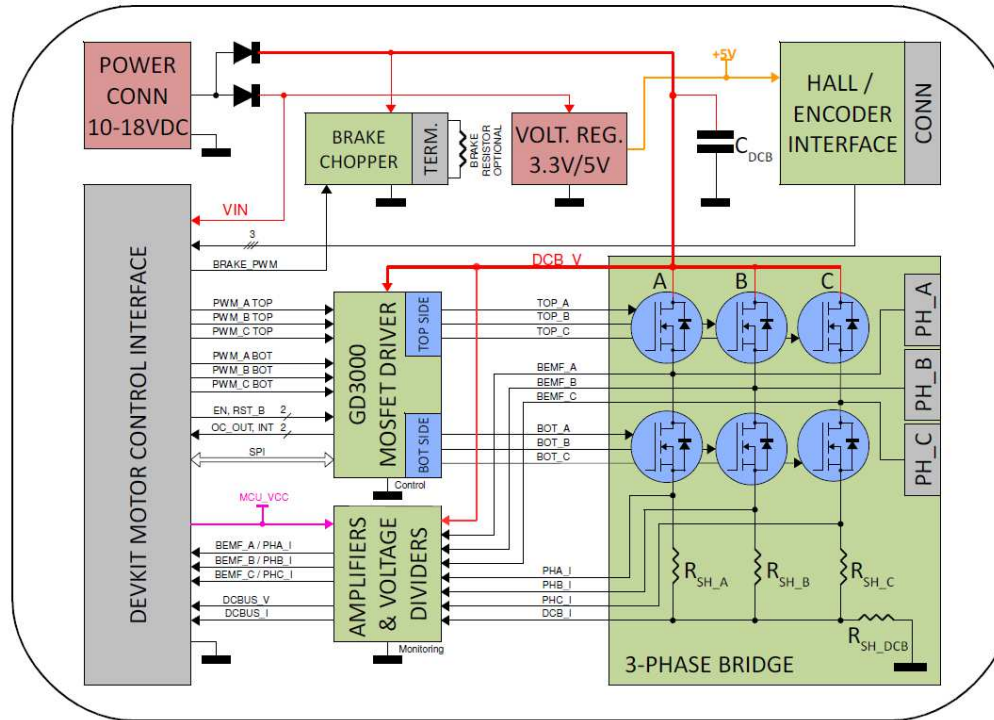
Revisions			
Rev	Description	Date	Approved
A	A085, Prototype Release	16 Sep 16	Jim/David
B	A085 (Final Schematic, BoM), Pilot Release	26 May 17	Phil/David
B1	IO Connector (J1 to J6) MFG. PN changed A085 (Final Schematic, BoM), Production Release	23 Jun 17	Alfredo A
B2	C16 (470pF) changed to DNP as per test feedback A085 (Final Schematic, BoM), Production Release	23 Aug 17	David C

# DEVKIT-MOTORGD BLDC/PMSM - MOTOR CONTROL REFERENCE DESIGN

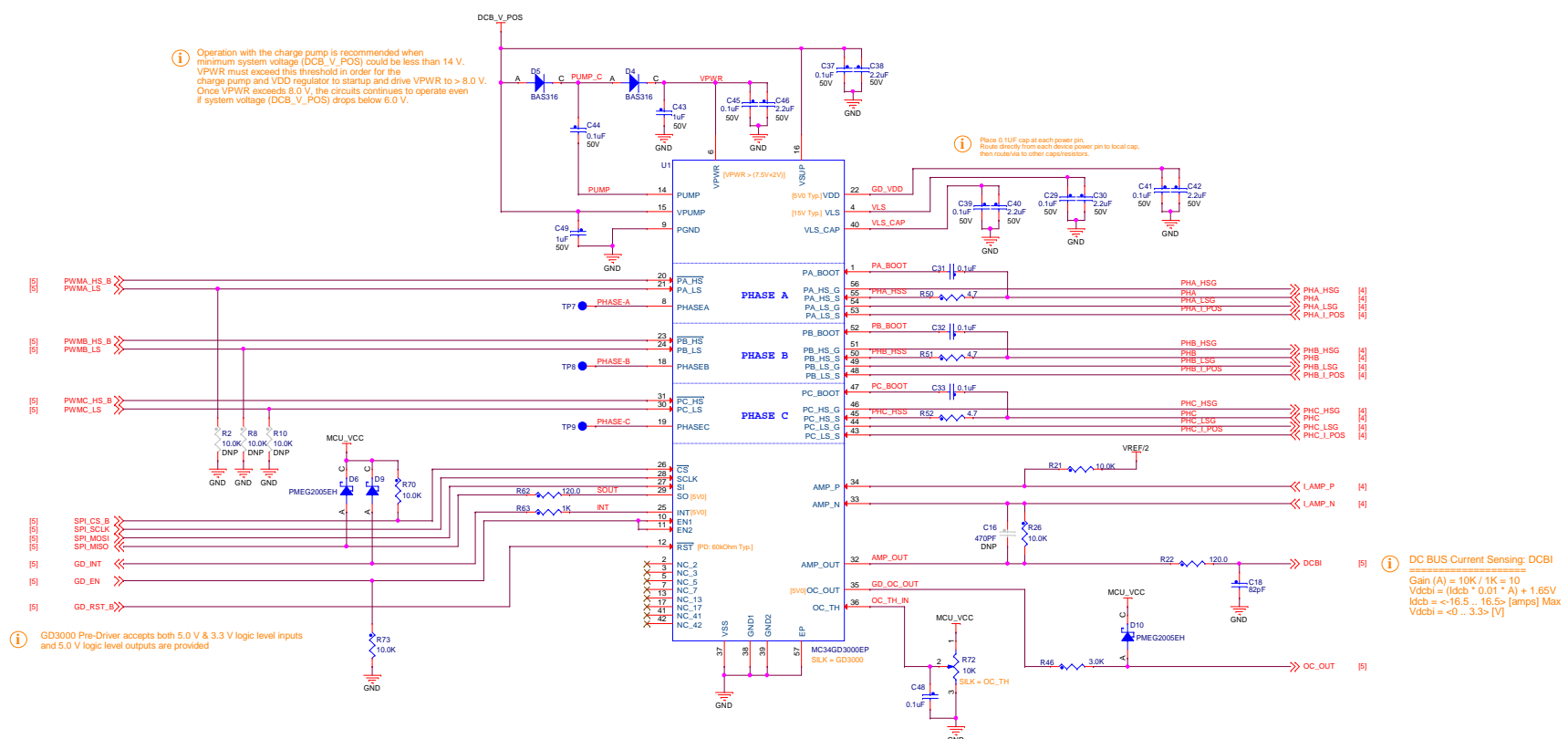
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ICAP Classification: CP: _____ IUC: X PUBE: _____			
Designer: Sahasubramanian	Drawing Title: <b>DEVKIT-MOTORGD</b>		
Drawn by: Sahasubramanian	Page Title: <b>TITLE PAGE</b>		
Approved: Phil / David Chung	Size C	Document Number SCH-29379 PDF: SPF-29379	Rev B2
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- Unless Otherwise Specified:
  - All resistors are in ohms, 5%, 1/10 Watt
  - All capacitors are in uF, 20%, 50V
  - All voltages are DC
  - All polarized capacitors are aluminum electrolytic
- Interrupted lines coded with the same letter or letter combinations are electrically connected.
- Device type number is for reference only. The number varies with the manufacturer.
- Special signal usage:
  - \_B Denotes - Active-Low Signal
  - <> or [] Denotes - Vectors Signals
- Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

## DEVKIT-MOTORGD for BLDC/PMSM



# GD3000 - THREE PHASE FET PRE-DRIVER



**i** Operation with the charge pump is recommended when minimum system voltage (DCB\_V\_POS) could be less than 14 V. VPWR must exceed this threshold in order for the charge pump and VDD regulator to startup and drive VPWR to > 8.0 V. Once VPWR exceeds 8.0 V, the circuits continues to operate even if system voltage (DCB\_V\_POS) drops below 6.0 V.

**i** Place 0.1uF cap at each power pin. Route directly from each device power pin to local cap, then route via to other capacitors.

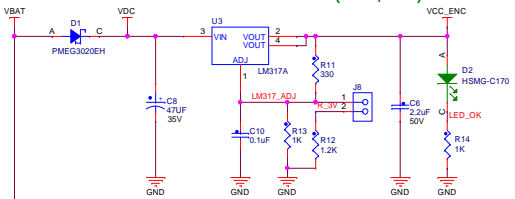
**i** GD3000 Pre-Driver accepts both 5.0 V & 3.3 V logic level inputs and 5.0 V logic level outputs

**i** DC BUS Current Sensing: DCBI  
Gain (A) = 10K / 1K = 10  
Vdcbi = (Idcb \* 0.01 \* A) + 1.65V  
Idcb = <-16.5 ... 16.5 [amps] Max  
Vdcbi = <0 ... 3.3> [V]

ICAP Classification:	CP: _____	NO: X PURL: _____
Drawing Title:	<b>DEVKIT-MOTORG8</b>	
Page Title:	<b>MOSFET PRE DRIVER GD3000</b>	
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# MOTOR CONTROL - POWER STAGE

## POWER SUPPLY - POSITION SENSOR (3.3V / 5V0)

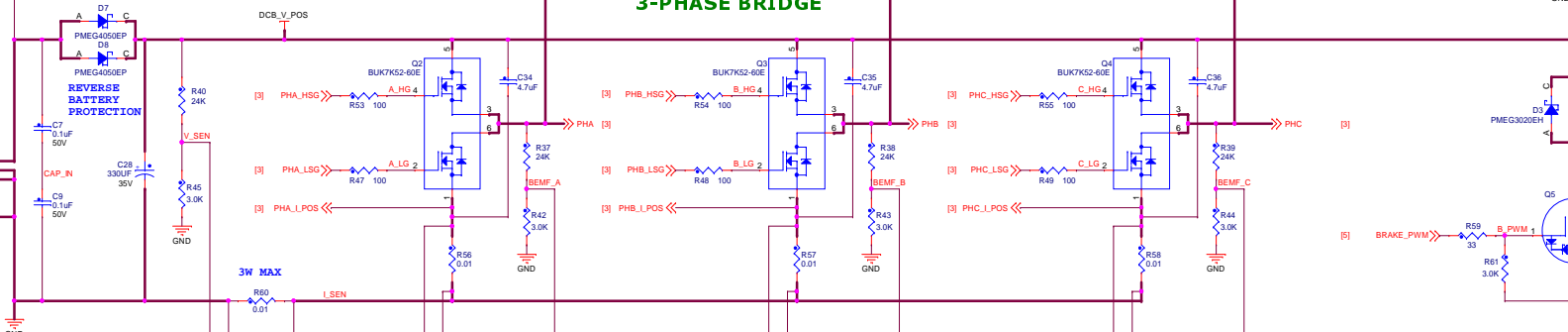


J8 VOLTAGE SELECTOR

VOLTAGE	J8
3.3V	3.3V
5.0V	5.0V

\*Default

## 3-PHASE BRIDGE

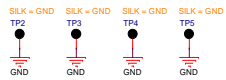


[10VDC - 18VDC]

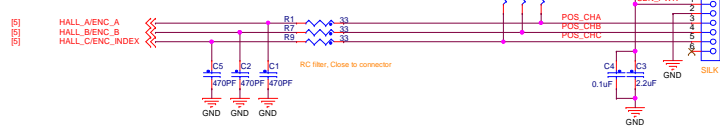
REVERSE BATTERY PROTECTION

Layout Note:  
Single GND in the Design. High Current GND path to be separated in the Layout by making void.

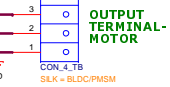
### GND - TEST POINTS



## HALL / ENCODER INTERFACE



## OUTPUT TERMINAL MOTOR



## BRAKE RESISTOR TERMINAL



### PMSM/BLDC, Jumper Selection

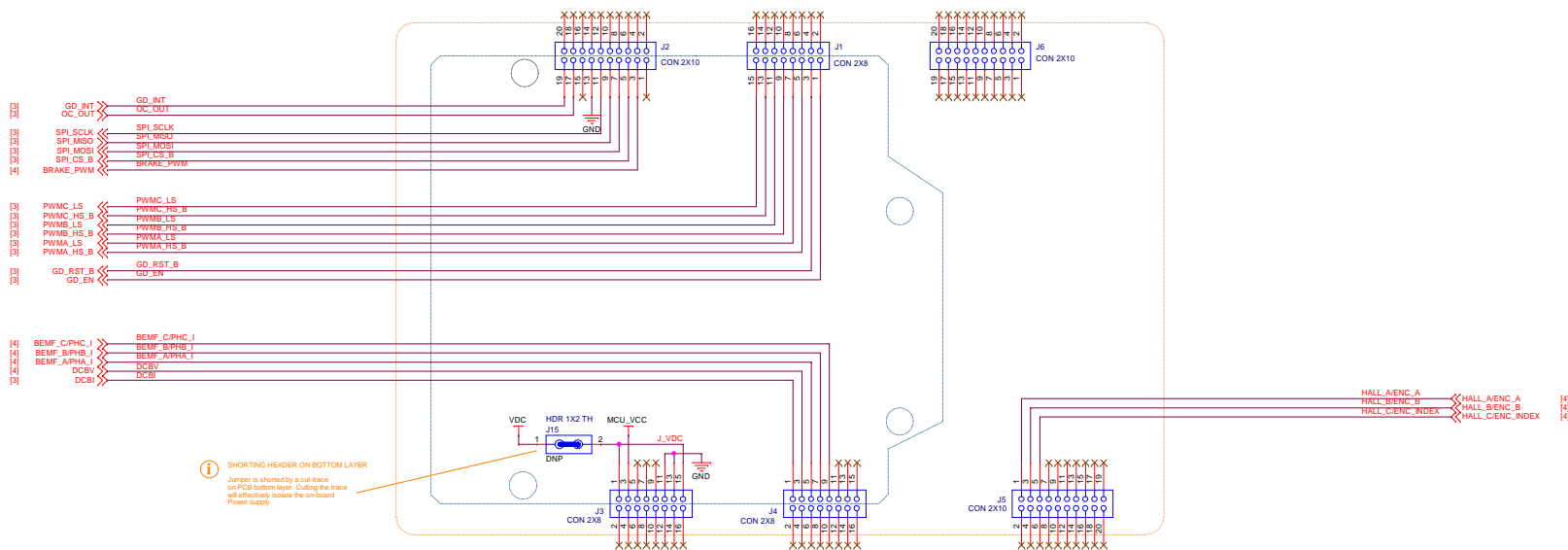
MODE	TP2	TP3	TP4	TP5
J10	1-2	2-3	1-3	1-4
J11	1-2	2-3	1-3	1-4
J12	1-2	2-3	1-3	1-4

\*Default

DC BUS Voltage sensing: DCBV  
3.3V @ 29.75V \*(3K/(24K+3K))  
5.0V @ 45.0V \*(3K/(24K+3K))

ICAP Classification: CP: ___ I/O: X PUR: ___	
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## DEVKIT / FRDM+ - IO CONNECTORS



① SHORTING HEADER ON BOTTOM LAYER  
 Jumper is shorted by a cut-trace on PCB bottom layer. Cutting the trace will effectively isolate the on-board Power supply.

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