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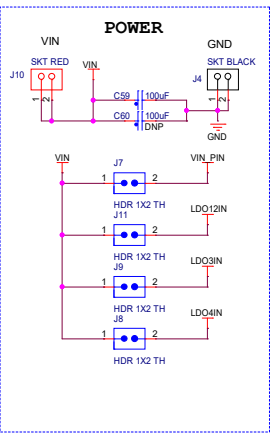
1	TITLE, TOC & REV
2	PMIC
3	KL25, Connector, AMUX

**Revisions**

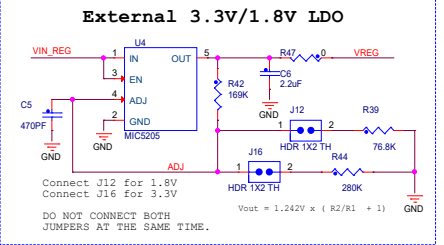
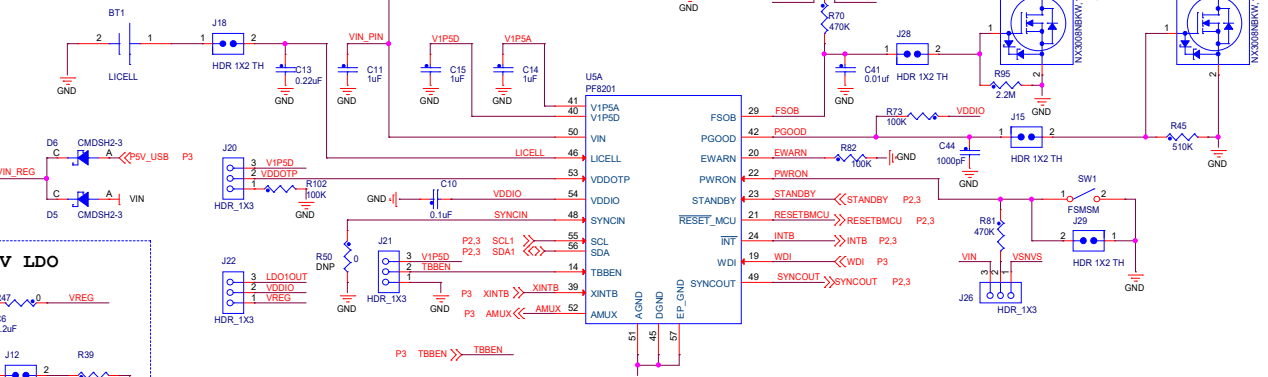
Rev	Description	Date	Approved
A	Initial schematic (Derivative from SCH-29723)	11-JUN-18	J. Romo
B	Replace R95 with a 2.2Mohm Resistor Mark R49, R55, R63, R62 as DNP Replace 4.7uF capacitor C45, C49, C55, C58, C57, C51, C46 (from 150-79693 to 150-79698) Replace red LED D2 from 370-76647 to 370-76617	1-JUL-19	Joaquin Romo

**KITPF8201FRDMEVM**

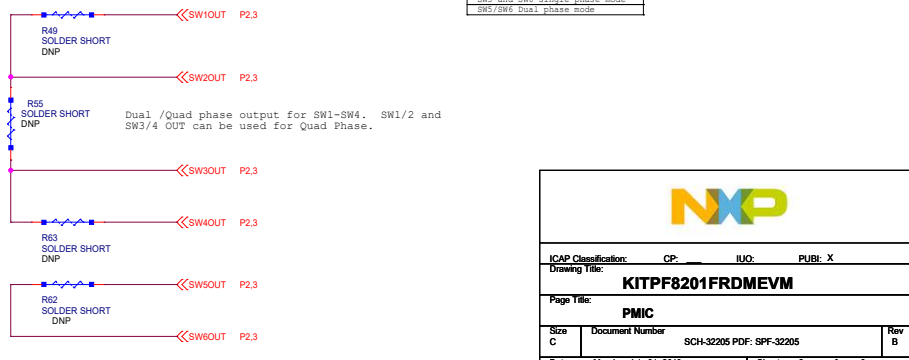
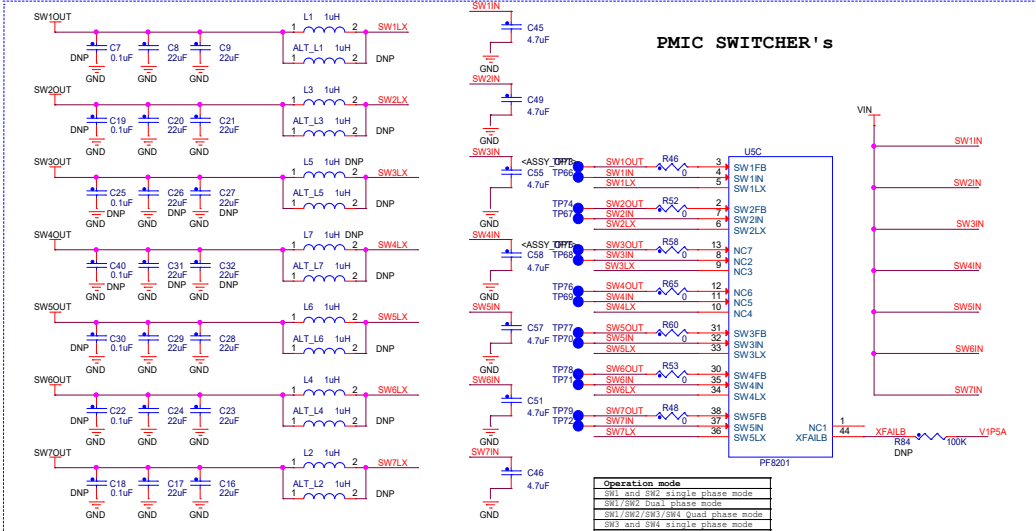
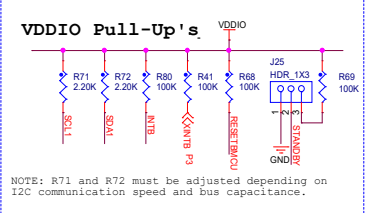
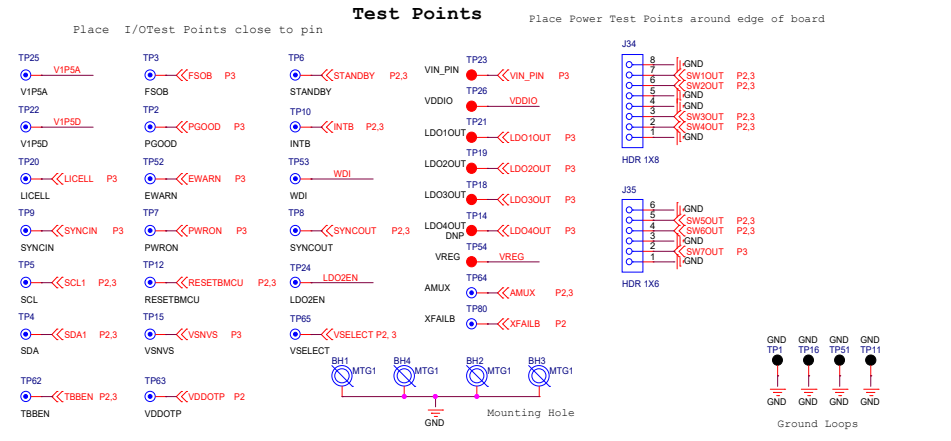
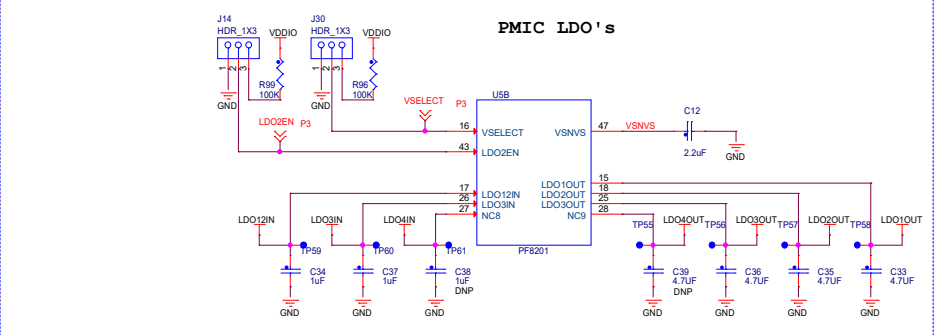
		<b>Analog Sensor Product Group</b> 6501 William Cannon Drive West Austin, TX 78735-8568	
		<small>This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.</small>	
Designer: Romo J.		ICAP Classification: CP: IJO: PUB: X	
Drawn by: Romo J.		Drawing Title: <b>KITPF8201FRDMEVM</b>	
Approved: Sakiu Y.		Page Title: <b>TITLE</b>	
Size C	Document Number SCH-32205 PDF: SFF-32205	Date: Monday, July 01, 2019	Rev B
Date: Monday, July 01, 2019		Sheet 1 of 3	



NOTE:  
 VDDOTP = GND, the device loads the configuration from the OTP Fuses  
 VDDOTP = VIP5D, the device loads the configuration from the default hardware configuration.



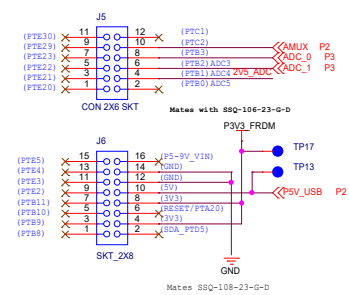
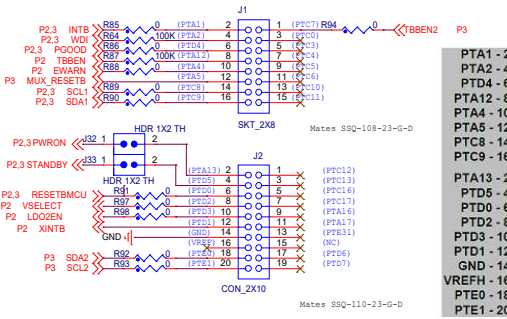
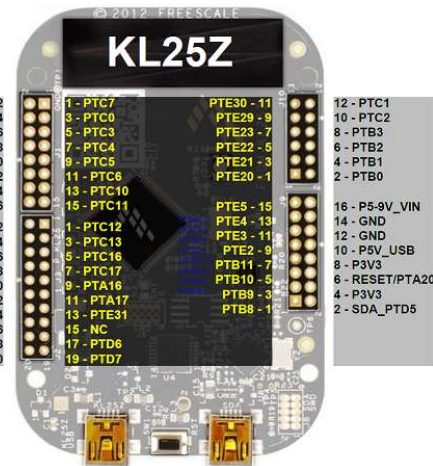
NOTE:  
 TBBSN = GND, the device operates in normal mode (full functionality)  
 TBBSN = VIP5D, the device enters TBS configuration and limited functionality. TBS registers can be set and then will be loaded after PWRON event.



**NXP**

ICAP Classification: CP- IUC: PUB: X  
 Drawing Title: **KITPF8201FRDMEV**  
 Page Title: **PMIC**  
 Size: Document Number: SCH-32205 PDF: SPF-32205 Rev B  
 Date: Monday, July 01, 2019 Sheet 2 of 3

## KL25Z INTERFACE



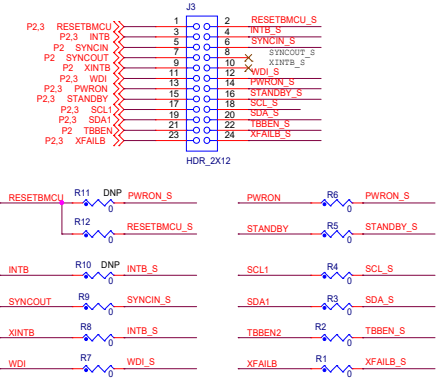
Populate the following connectors on the Freedom board (female with long pins, low insertion):  
 SSQ-106-23-G-D / 210-80515  
 SSQ-110-23-G-D / 210-80513  
 SSQ-108-23-G-D (x2) / 210-80247

## VOLTAGE SENSE

RAIL	VOLTAGE RANGE	AMUX/CHANNEL
SW1	0.4V to 1.8V, 2500mA	AMUX 1/CH 1
SW2	0.4V to 1.8V, 2500mA	AMUX 1/CH 2
SW3	0.4V to 1.8V, 2500mA	AMUX 1/CH 3
SW4	0.4V to 1.8V, 2500mA	AMUX 1/CH 4
SW5	0.4V to 1.8V, 2500mA	AMUX 1/CH 5
SW6	0.4V to 1.8V, 2500mA	AMUX 1/CH 6
RESERVED		AMUX 1/CH 7
RESERVED		AMUX 1/CH 8
VIN	2.7V to 5.5V	AMUX 2/CH 1
VSNVS	1.8V, 3.0V, 3.3V, 10mA	AMUX 2/CH 2
LICELL	1.8V, 3.0V, 3.3V, 10mA	AMUX 2/CH 3
SW7	1.2V to 4.5V, 2500mA	AMUX 2/CH 4
LDO1	1.5V to 5V, 400mA	AMUX 2/CH 5
LDO2	1.5V to 5V, 400mA	AMUX 2/CH 6
LDO3	1.5V to 5V, 400mA	AMUX 2/CH 7
LDO4	1.5V to 5V, 400mA	AMUX 2/CH 8

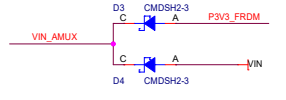
### Master/Slave Connector

NOTE: Use single 12 Row connector to connect Slave side from primary EVB to Master side of 2nd EVB. Resistors can be configured on primary board for specific configurations.

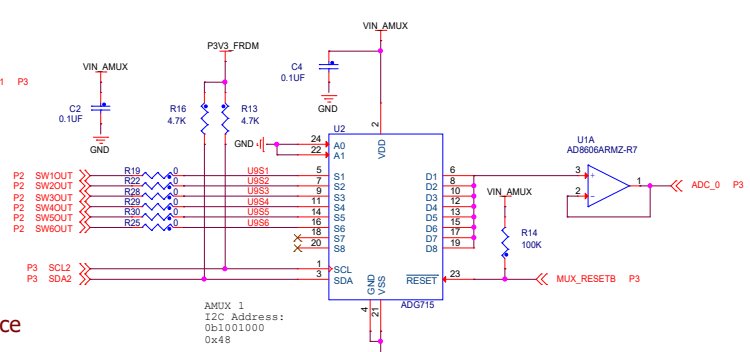


### SECONDARY AMUX

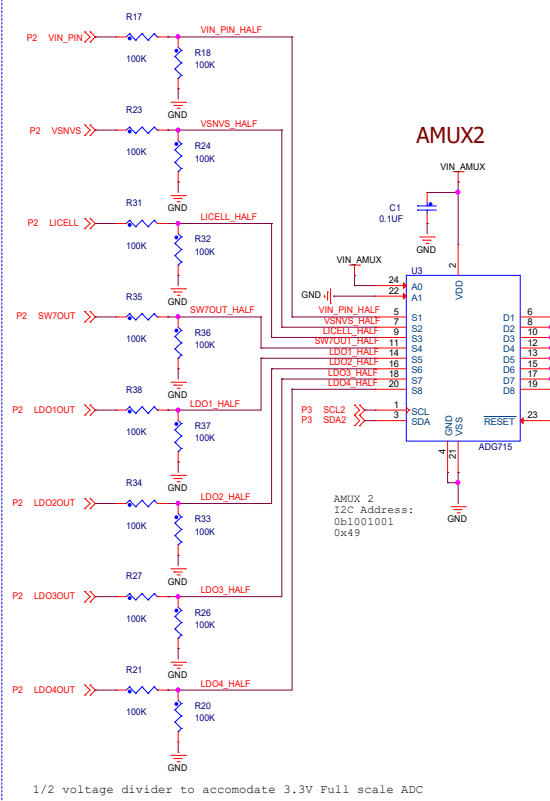
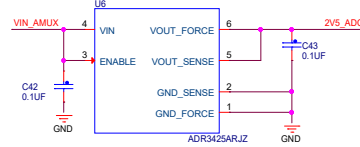
NOTE: Secondary AMUX is intended for Software purposes. GUI can use this to enable live monitoring instead of using AMUX on PFB100/8200. AMUX uses the best of supply from P3V3 Freedom supply and VIN.



### AMUX1



### 2.5V Voltage reference



1/2 voltage divider to accommodate 3.3V Full scale ADC

