TWR-P1025

Change List

Revision History

<table>
<thead>
<tr>
<th>Rev</th>
<th>Description</th>
<th>Approved Date</th>
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<tbody>
<tr>
<td>X1</td>
<td>Initial Draft</td>
<td>Jun 17, 11</td>
</tr>
<tr>
<td>X1.1</td>
<td>BOM changes for cost optimisation</td>
<td>Jul 27, 11</td>
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<td>X1.2</td>
<td>BOM Reduction for cost and space.</td>
<td>Sep 07, 11</td>
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<td>X1.3</td>
<td>Minor updates</td>
<td>Dec 07, 11</td>
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<td>X1.4</td>
<td>CPLD Pin Swapping to aid routing</td>
<td>Dec 07, 11</td>
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<tr>
<td>A</td>
<td>Released REV A - BRA085 - ECO33160</td>
<td>Aug 01, 11</td>
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<tr>
<td>B</td>
<td>Released REV B - MP210/Ethernet Routing cleanup and errata fixes</td>
<td>Aug 10, 11</td>
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<tr>
<td>B1</td>
<td>Changed P1025 part number and some DBPs so BOM changes only no LAY change</td>
<td>Dec 22, 11</td>
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</tbody>
</table>
1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _N Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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P1025 SPI CS allocation
-------------------------
CS0 - Elevator SPI0_CS0
CS1 - Elevator SPI0_CS1
CS2 - 1588 DAC
CS3 - Unused

P1025 I2C1 Bus
---------------
Address Device
0x50 Boot EEPROM
TBD Elevator I2C Bus 0

P1025 I2C2 Bus
---------------
Address Device
0x1C Accelerometer
0x23 GPIO Expander
0x52 BRD EEPROM
TBD Mini PCIe
TBD Elevator I2C bus 1

P1025 UART0
------------
FDTI - Default

P1025 UART1
------------
Elevator UART
FDTI

P1025 FLASH CS
---------------
CS0 - NOR FLASH
CS1 - Elevator CS0
CS2 - Elevator CS1