


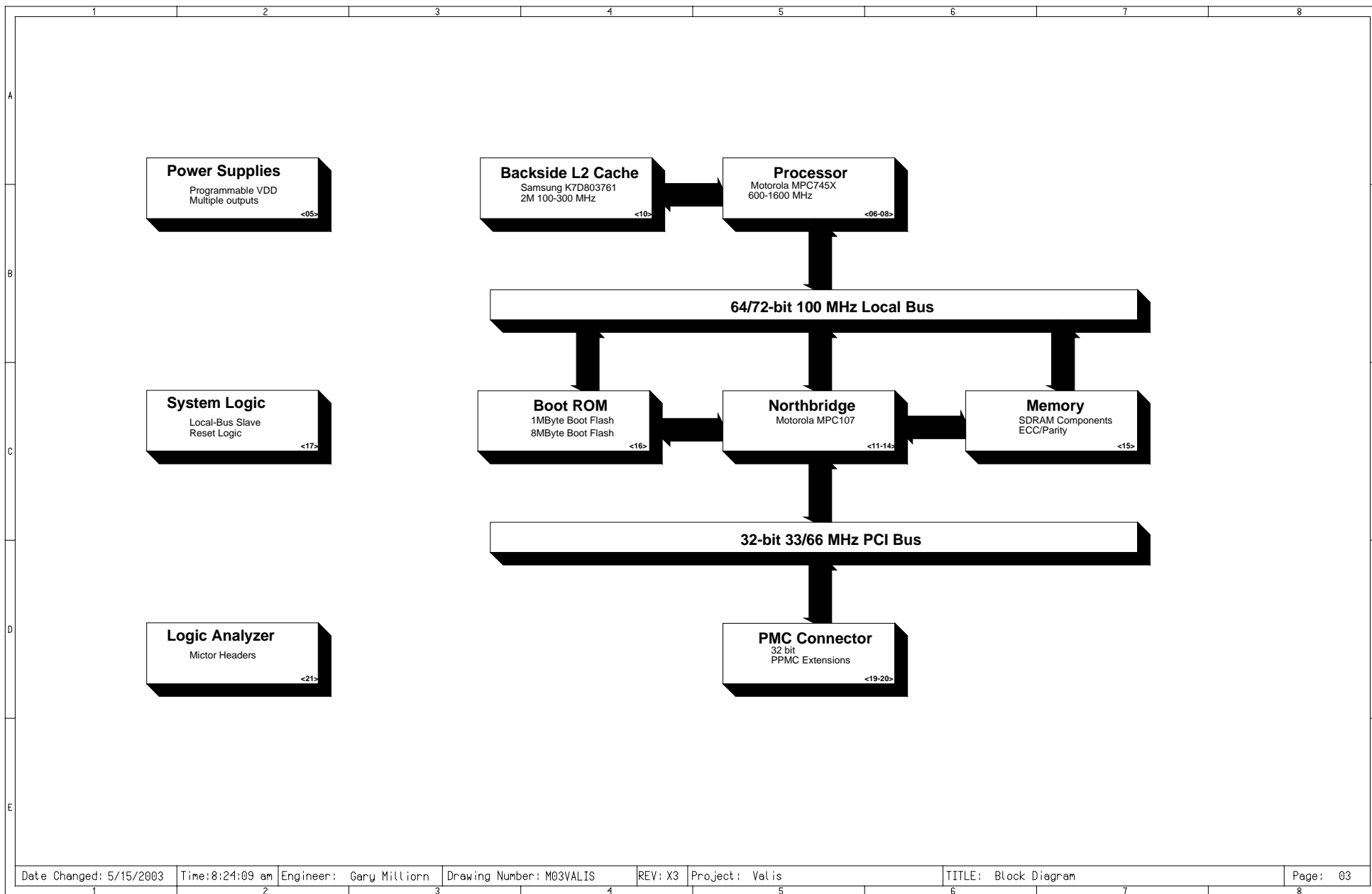
Valis*

***MPC7450
MPC7451
MPC7455
MPC7457***

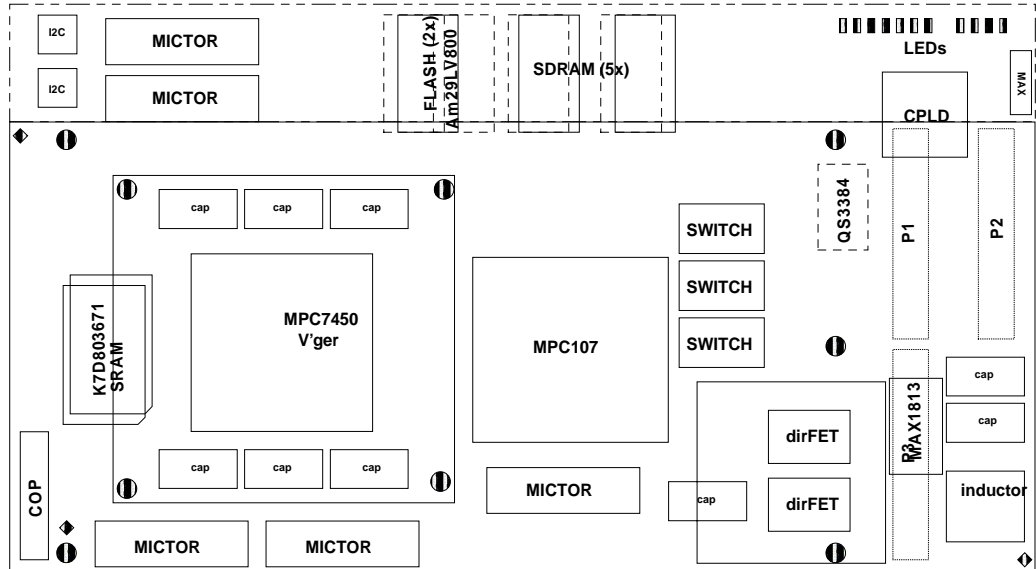
intelligence  ***everywhere***

digital dna*

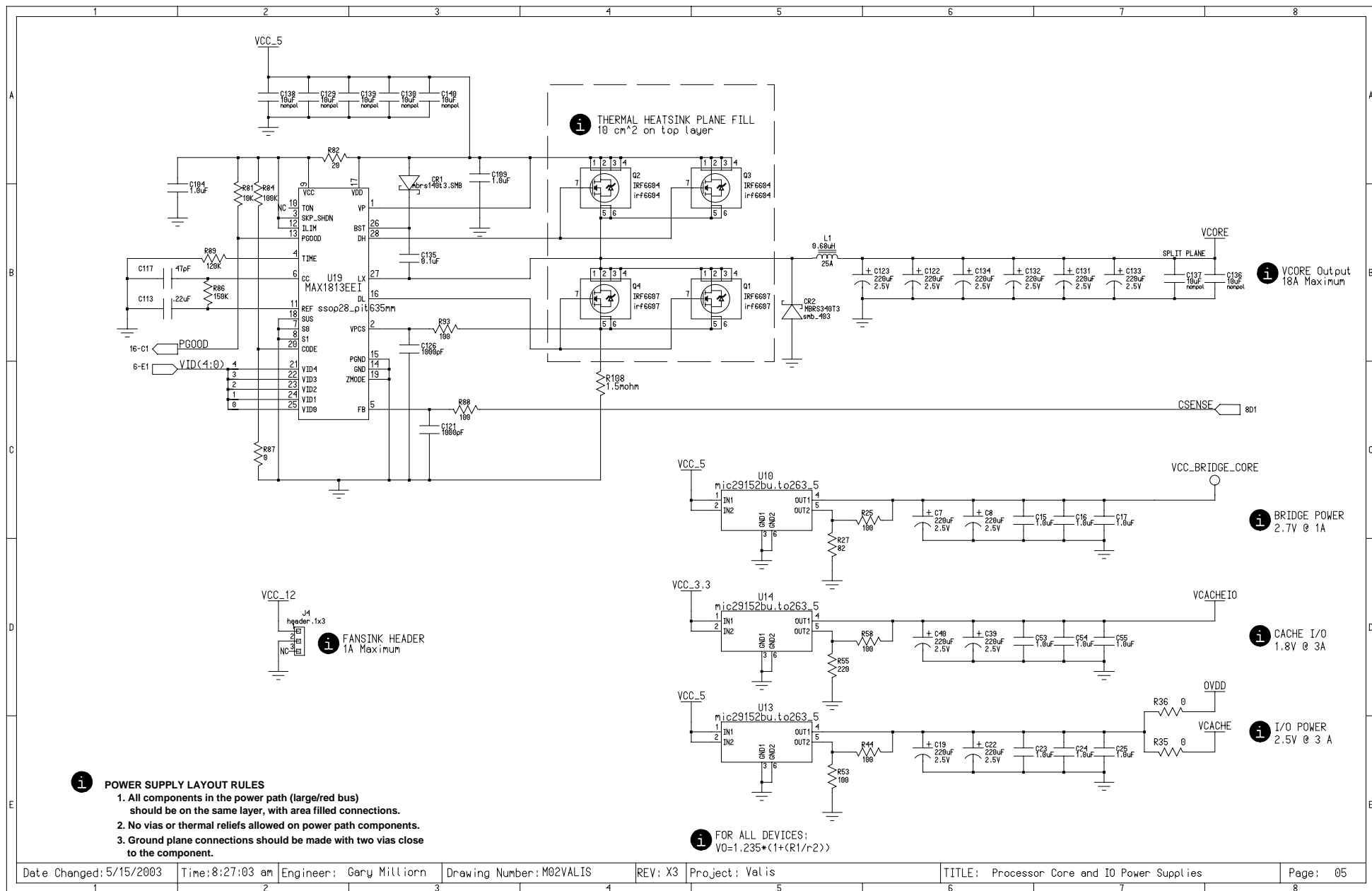
1												2												3												4												5												6												7												8											
A												Schematic Notes												Page												Contents																																																											
												1. Unless otherwise specified: All resistors are SMD0603, in ohms, 0.08W, +/-5% All capacitors are SMD0603, in microfarads (uF), +/-20%. All inductances are in microhenries (uH). All ferrites are Z=50 ohms at 100 MHz. All fuses are self-resetting polyswitch (PTC) devices. Board impedance is 55 +/- 5 ohms.												01												Cover Page																																																											
												2. Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are: GND VCACHE VCACHE_IO VCC_3.3 VCC_2.5 OVDD VCC_5 VCORE VCC_12												02												General Information																																																											
												3. Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.												03												Block Diagram																																																											
												4. Motorola and the Motorola logo are registered trademarks of Motorola. PowerPC is a trademark of IBM. Other trademarks are the respective property of their respective copyright holders. There is no spoon. All rights reserved. No warranty is made, express or implied.												04												Routing and Layout Information																																																											
												5. The sheet-to-sheet cross reference format is: Sheet "-" VertZoneLetter HorizZoneNumber												05												Power Supply																																																											
B												6. Components with the visible property "NO STUFF" are not to be installed by default; they are for test or manufacturing purposes only. 												06												MPC745X System Logic																																																											
												7. All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.												07												MPC745X Cache Interface																																																											
												8. Team Valis is: Cindy Callis.....CAD/Layout Ivan Erickson.....Program Manager Gary Milliom.....Hardware Design Tony Saucedo.....Purchasing Margarito Trevino.....Tech/Debug Gary Wojcik.....Grand Poobah												08												MPC745X Power																																																											
C												<div>Valis*</div>												09												Board Options/COP																																																											
																								10												L2 Cache SRAM																																																											
																								11												MPC107: System Logic																																																											
																								12												MPC107: Processor Interface																																																											
																								13												MPC107: PCI Interface																																																											
																								14												MPC107: Memory Interface																																																											
																								15												SDRAM SODIMM Socket																																																											
																								16												Local Boot ROM																																																											
																								17												System FPGA																																																											
																								18												Configuration Logic / LEDs																																																											
																								19												PMC Connectors.																																																											
																								20												Extra PMC Connector																																																											
																								21												Analyzer Headers																																																											

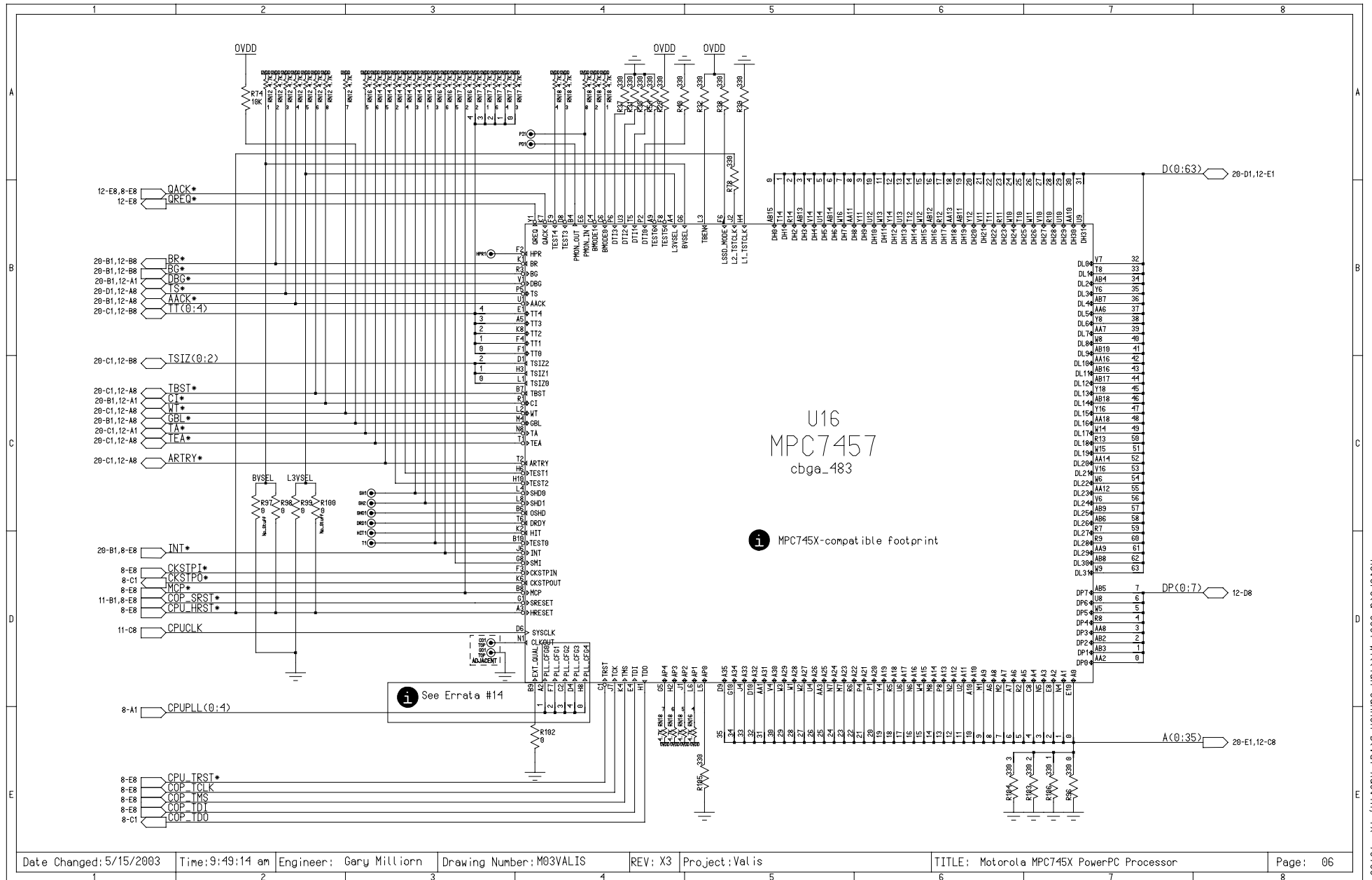


Layout/Routing Instructions	
05	Place components approximately as shown on this page. Keep relative distances short and use heavy traces for everything. All power connections are to be made to a plane except sense lines.
06	Avoid routing traces, especially noisy ones, across CPUPLL bus.
07	Keep AVDD filter near CPU. Route all groups to equal lengths. L3RU (routed daisy-chain) L3RL (routed daisy-chain) L3CTL (routed as a T)
08	Place bypass caps as shown. Use two ground-attach vias.
09	Place COP connector in I/O area. Proximity to CPU is not a high priority. Insure that COP pin numbering matches view as shown on schematic (i.e. pin 1 and pin 16 are on opposite corners).
10	Place BGAs paired on top and bottom of board. Place within 2.5cm of MPC7450. Surround each component with bypass capacitors. Use thick trace (>=12mil) for VREF, 24mil for VCACHE.
11	Avoid routing traces, especially noisy ones, across MPC107 PLL bus. Do not swap order of MPC107 PLL switch connections. PCI clock input must be 2.5" (per specification).
12	
13	Keep AVDD/LAVDD filters near MPC107. Use heavy, short traces from filter to pins. Surround MPC107 with bypass caps to provide additional ground-return paths. Use two ground-attach vias. Connect VCC_PCI_C (PCI Clamp) using heavy trace, not a plane.
14	Place series termination resistors very near source (MPC107), < 2cm. Route SDRAM clocks to equal lengths, including SDRAM_SYNCOUT to SDRAM_SYNCIN path.
15	
16	Keep data bus length for ROM short.
17	
18	
19	Maximum trace length for PCI signals to MPC107 is 1.5" per the PCI specification.
20	
21	



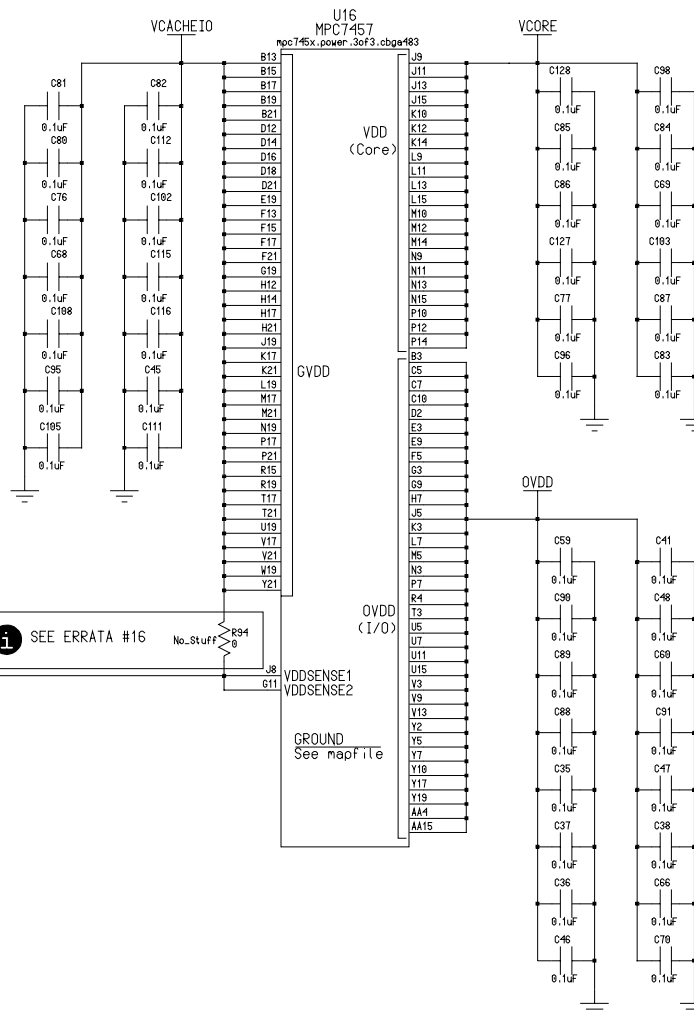
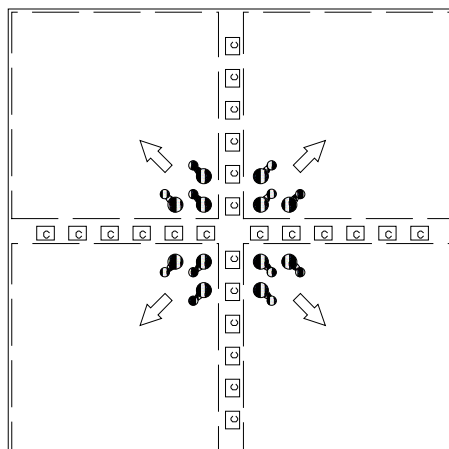
.095			
LAYER 1	COMP	1.0oz	SIGNAL: 1
LAYER 2	PLANE	0.5oz	PLANE: GND
LAYER 3	SIGNAL	0.5oz	SIGNAL: 3
LAYER 4	SIGNAL	0.5oz	SIGNAL: 4
LAYER 5	PLANE	0.5oz	PLANE: VCC, 2.5 + VCACHE
LAYER 6	SIGNAL	0.5oz	SIGNAL: 5
LAYER 7	SIGNAL	0.5oz	SIGNAL: 6
LAYER 8	PLANE	0.5oz	PLANE: VCORE + VCC_BRIDGE_CORE
LAYER 9	PLANE	0.5oz	PLANE: GND
LAYER 10	SIGNAL	0.5oz	SIGNAL: 7
LAYER 11	SIGNAL	0.5oz	SIGNAL: 8
LAYER 12	PLANE	0.5oz	PLANE: VCC, 3.3 + OVDD + VCACHEIO
LAYER 13	SIGNAL	0.5oz	SIGNAL: 9
LAYER 14	SIGNAL	0.5oz	SIGNAL: 10
LAYER 15	PLANE	0.5oz	PLANE: GND
LAYER 16	SOLDER	1.0oz	SIGNAL: 2



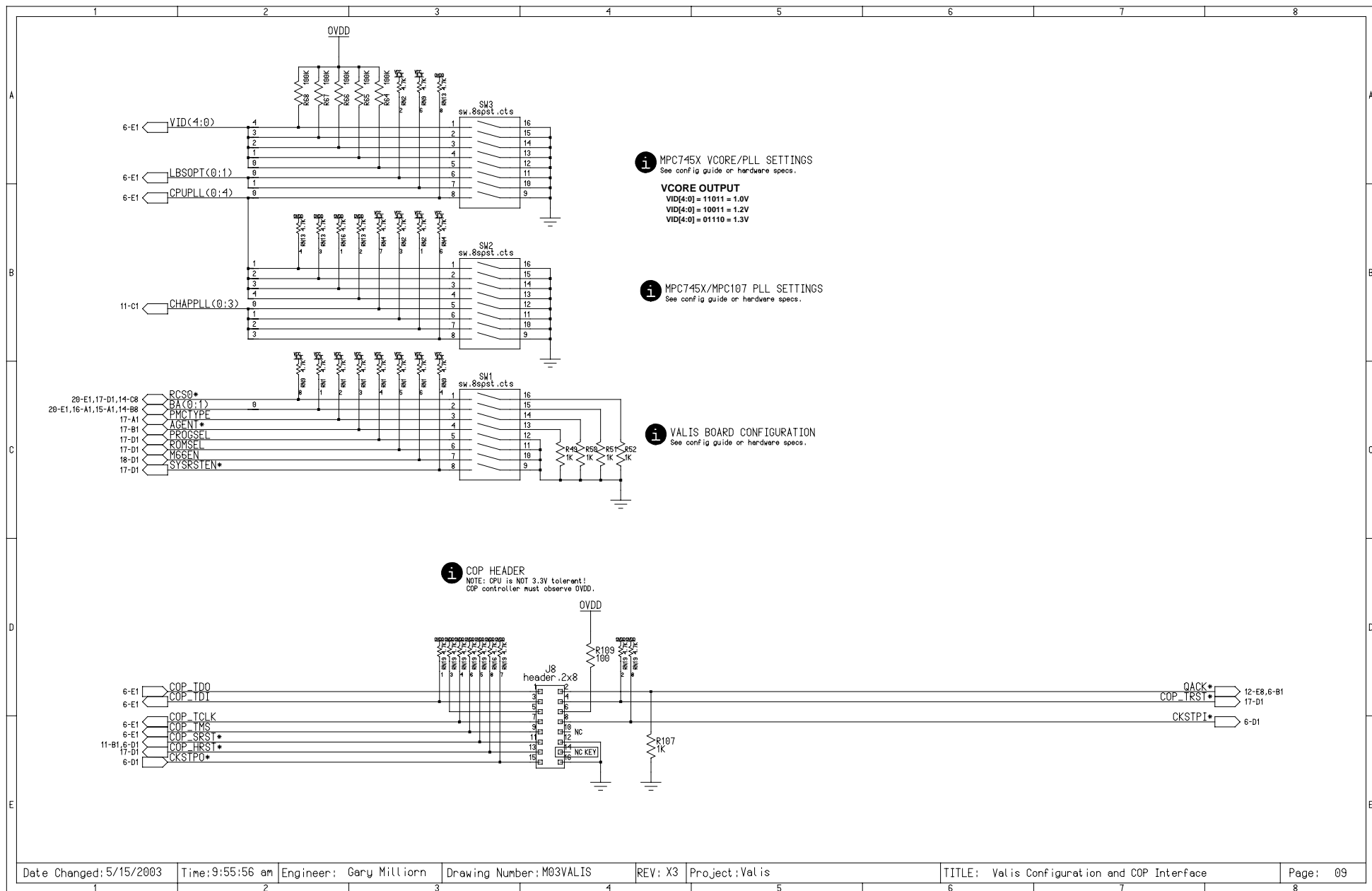


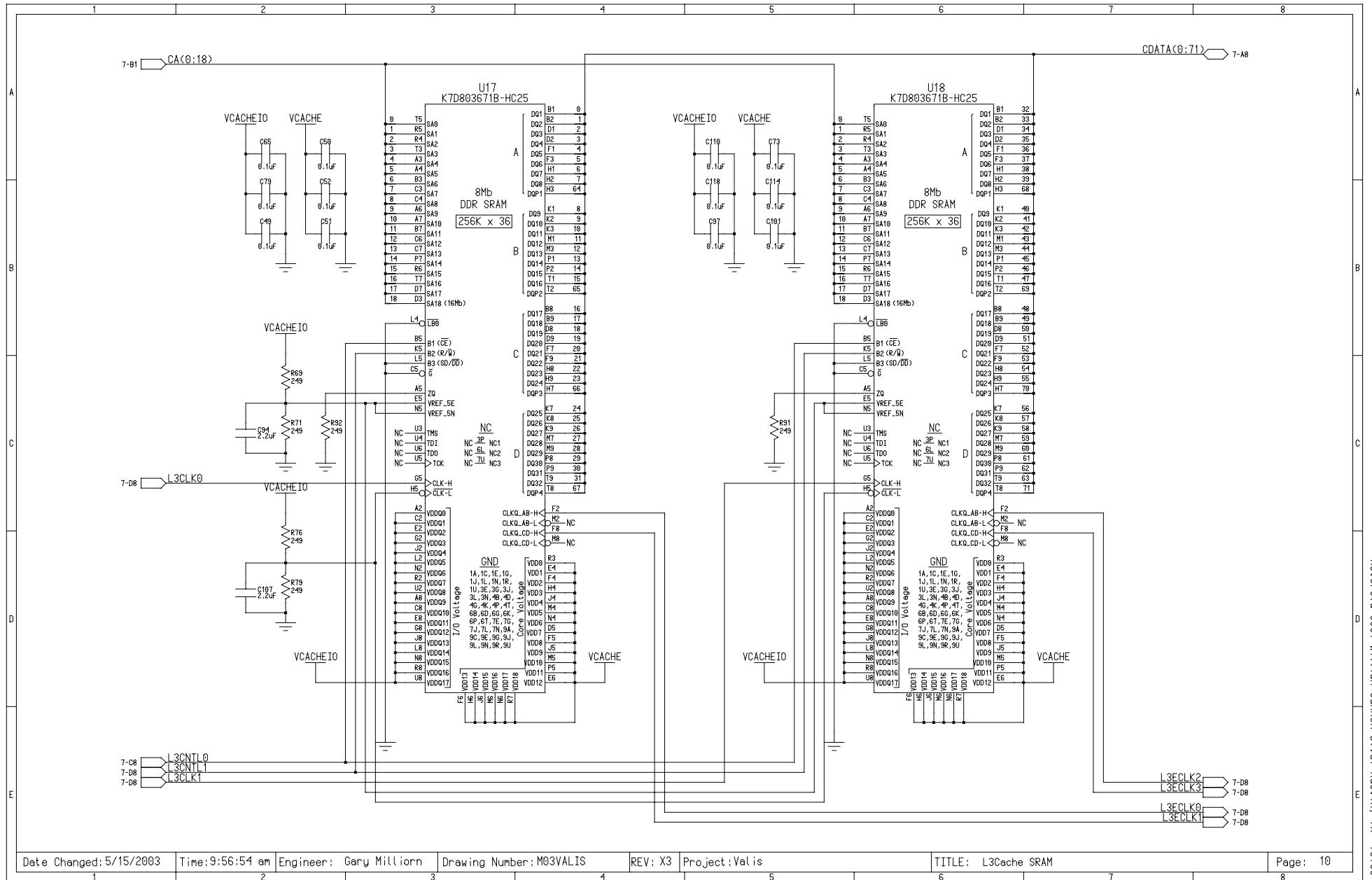
i CPU POWER BYPASS CAPS
Keep near CPU.

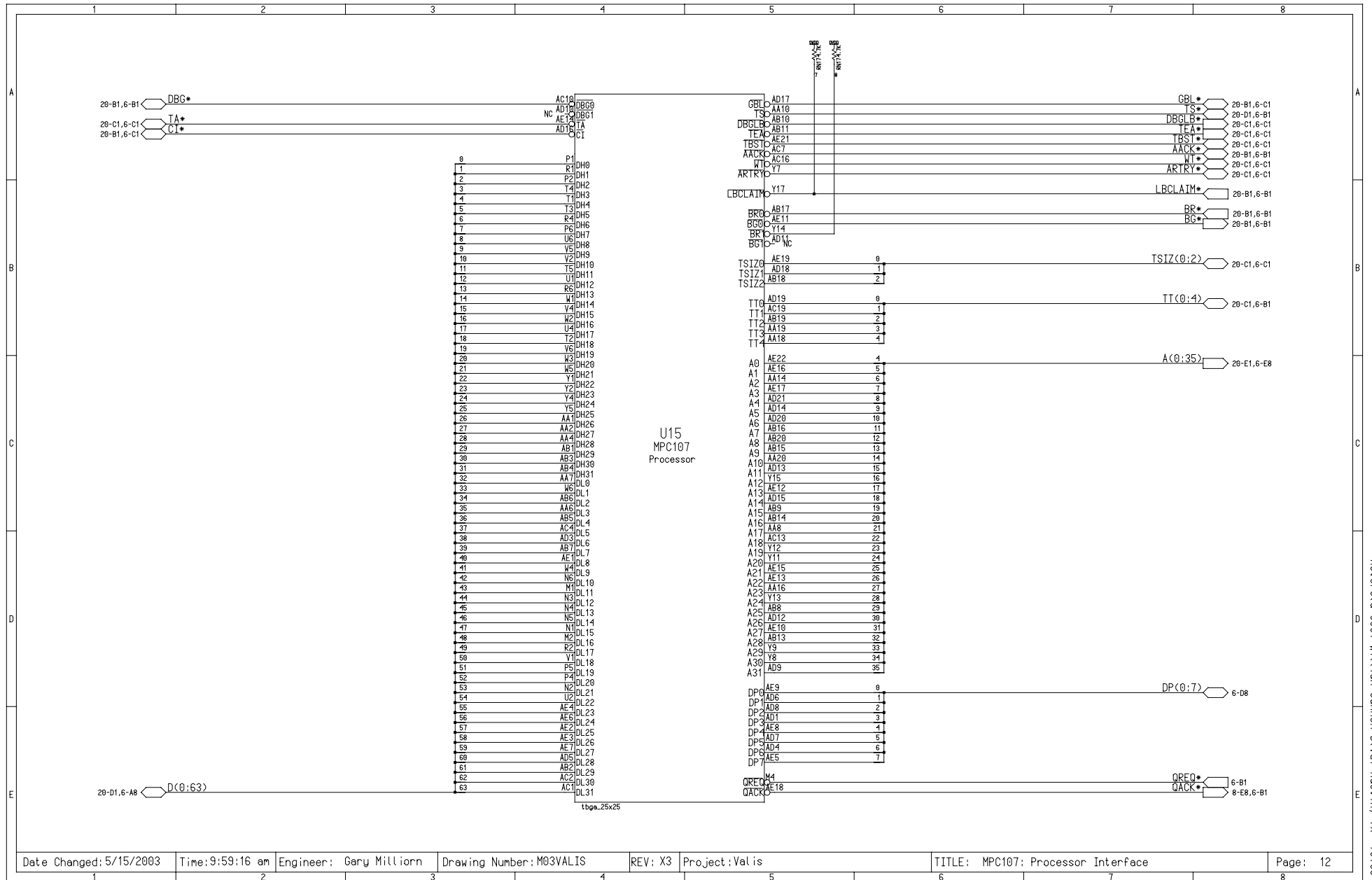
i CBGA483 ESCAPE PATTERN
and CAPACITOR PLACEMENT

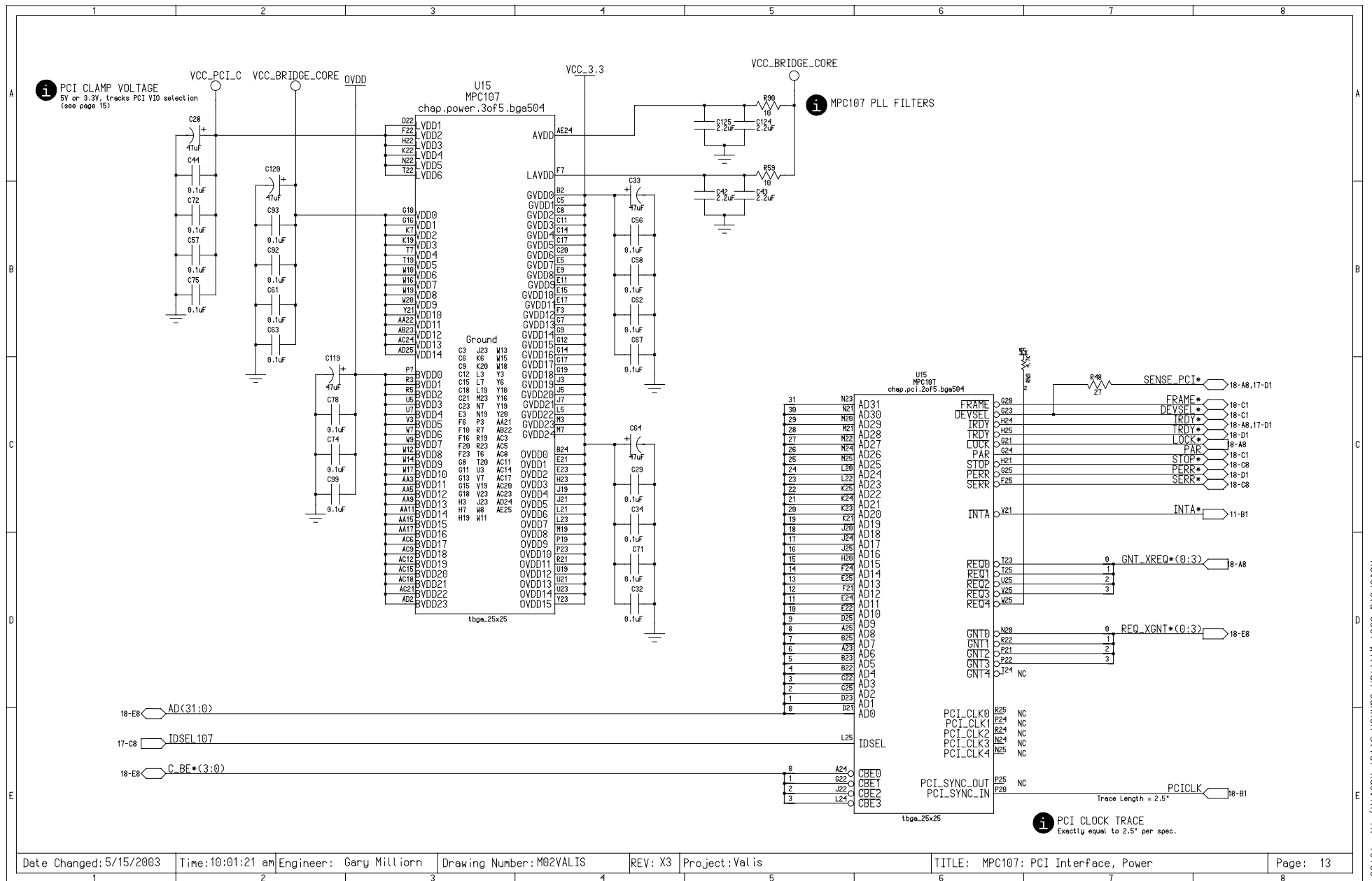


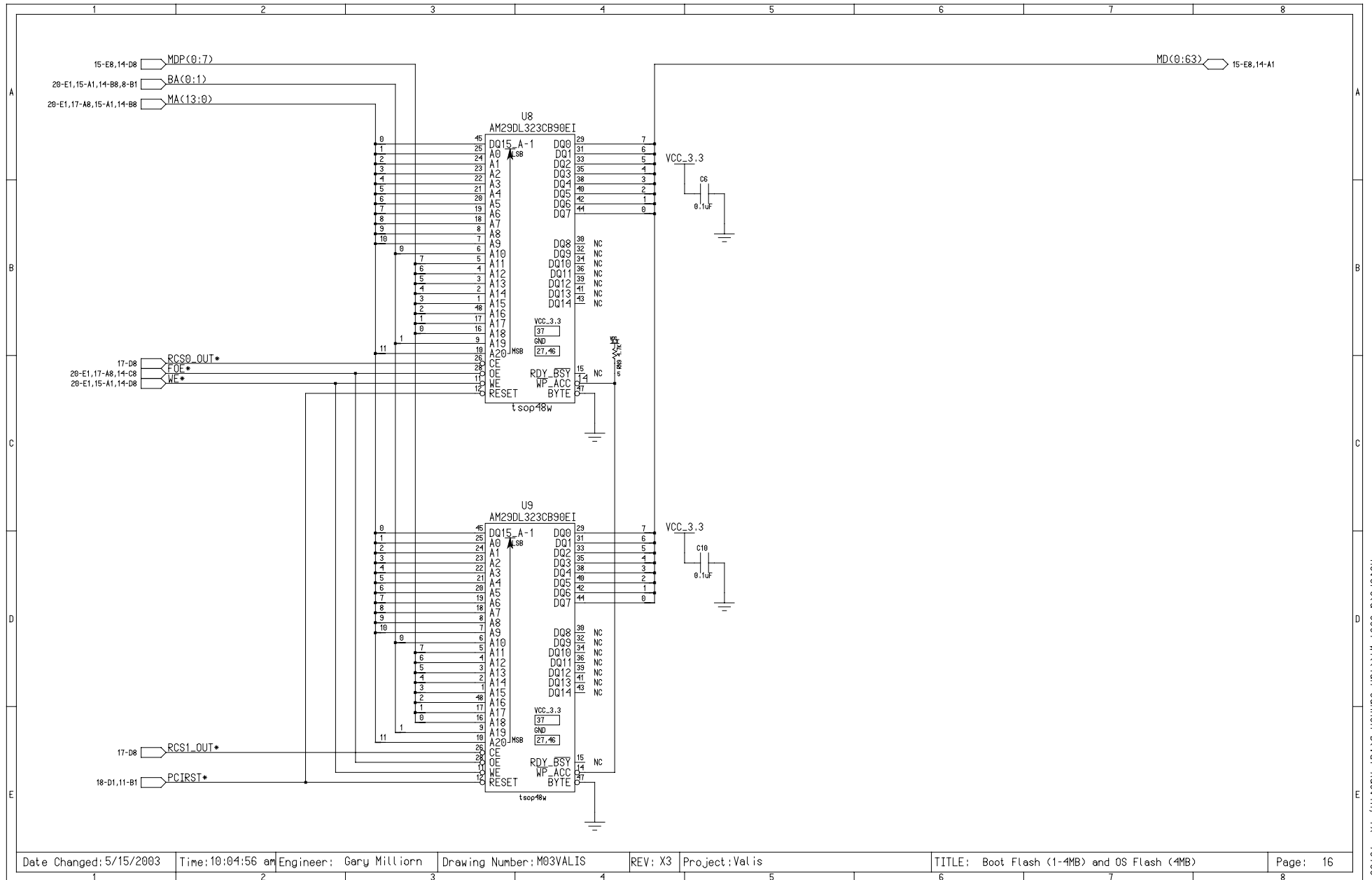
5C8 CSENSE

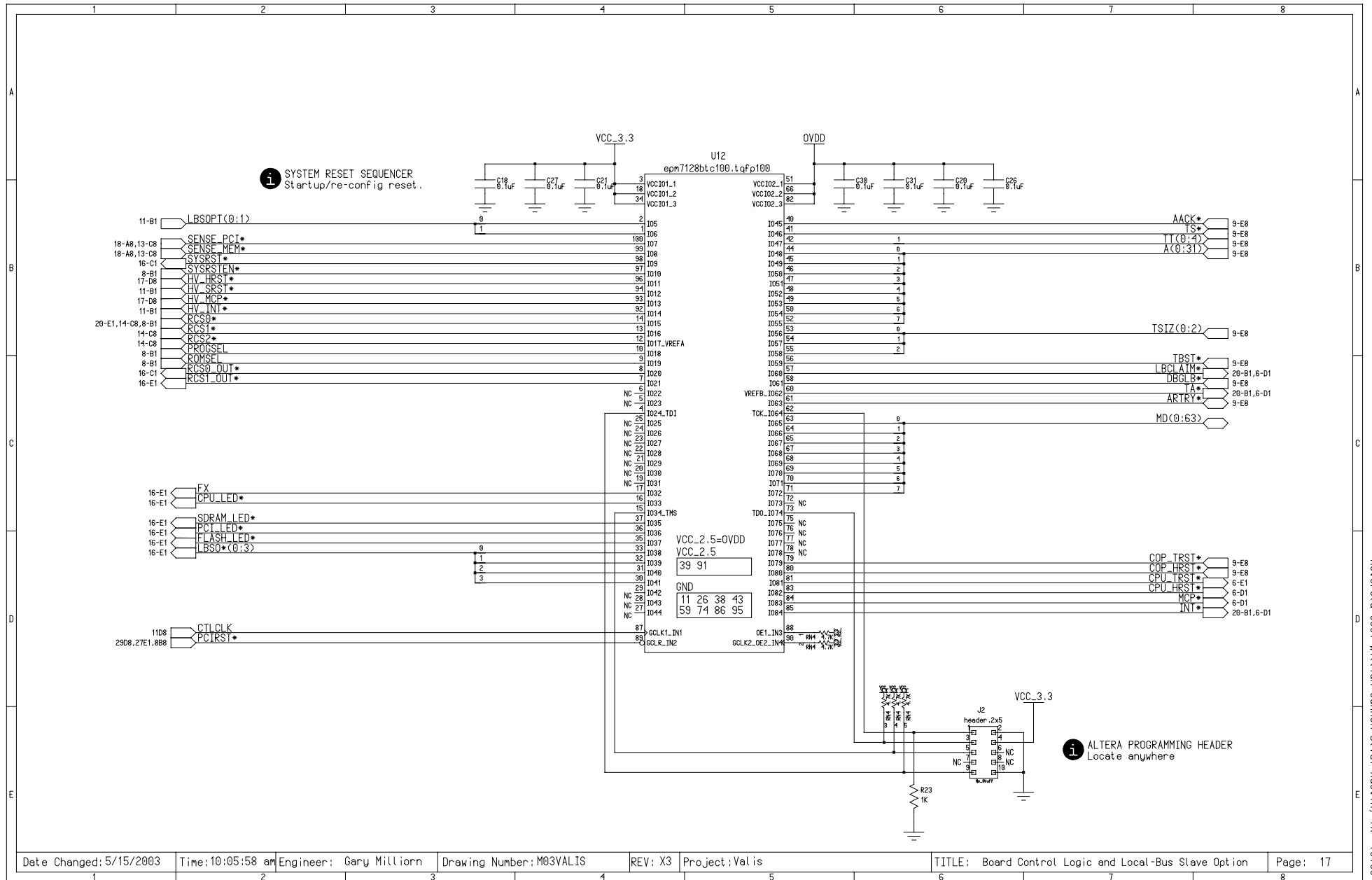


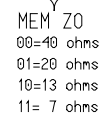




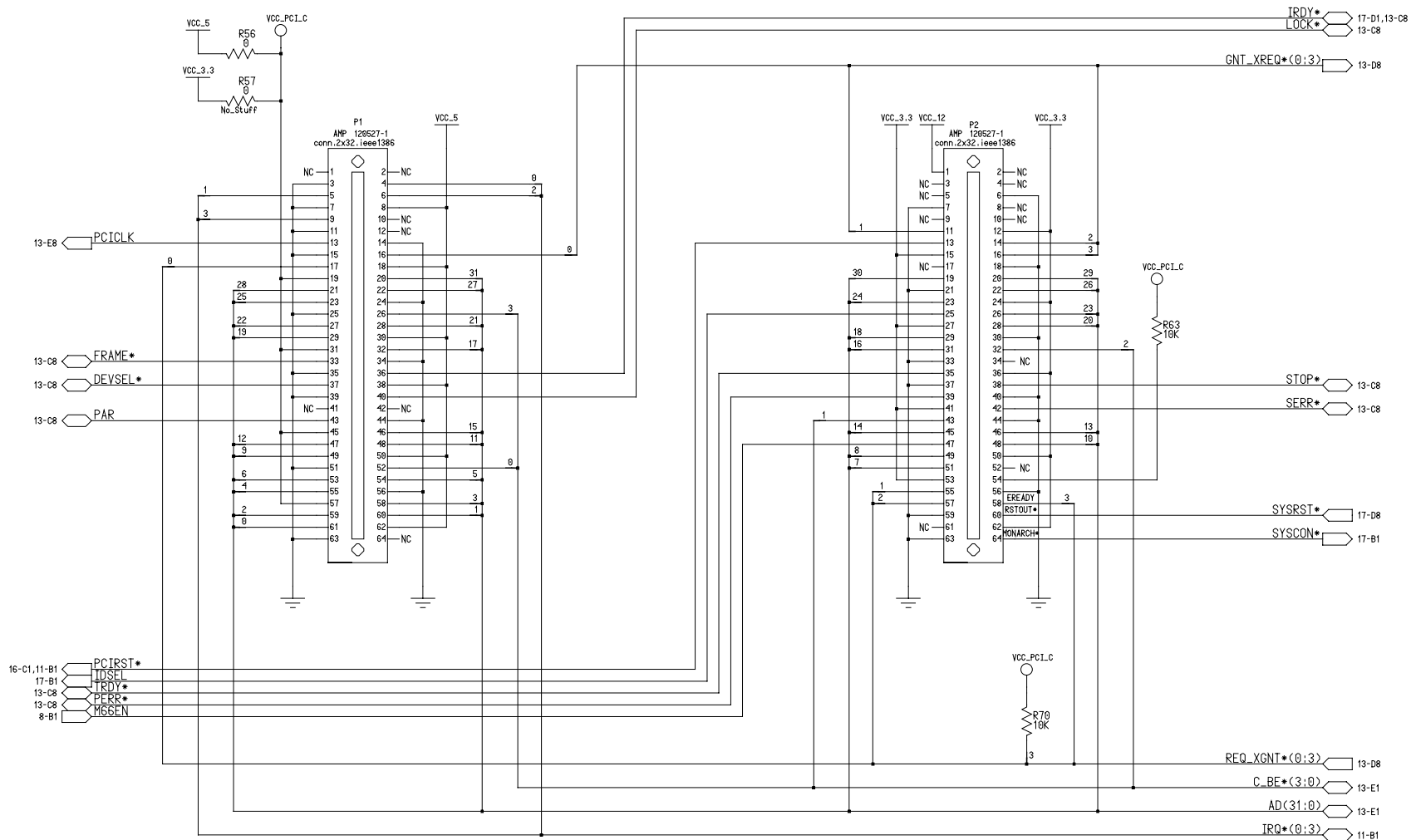


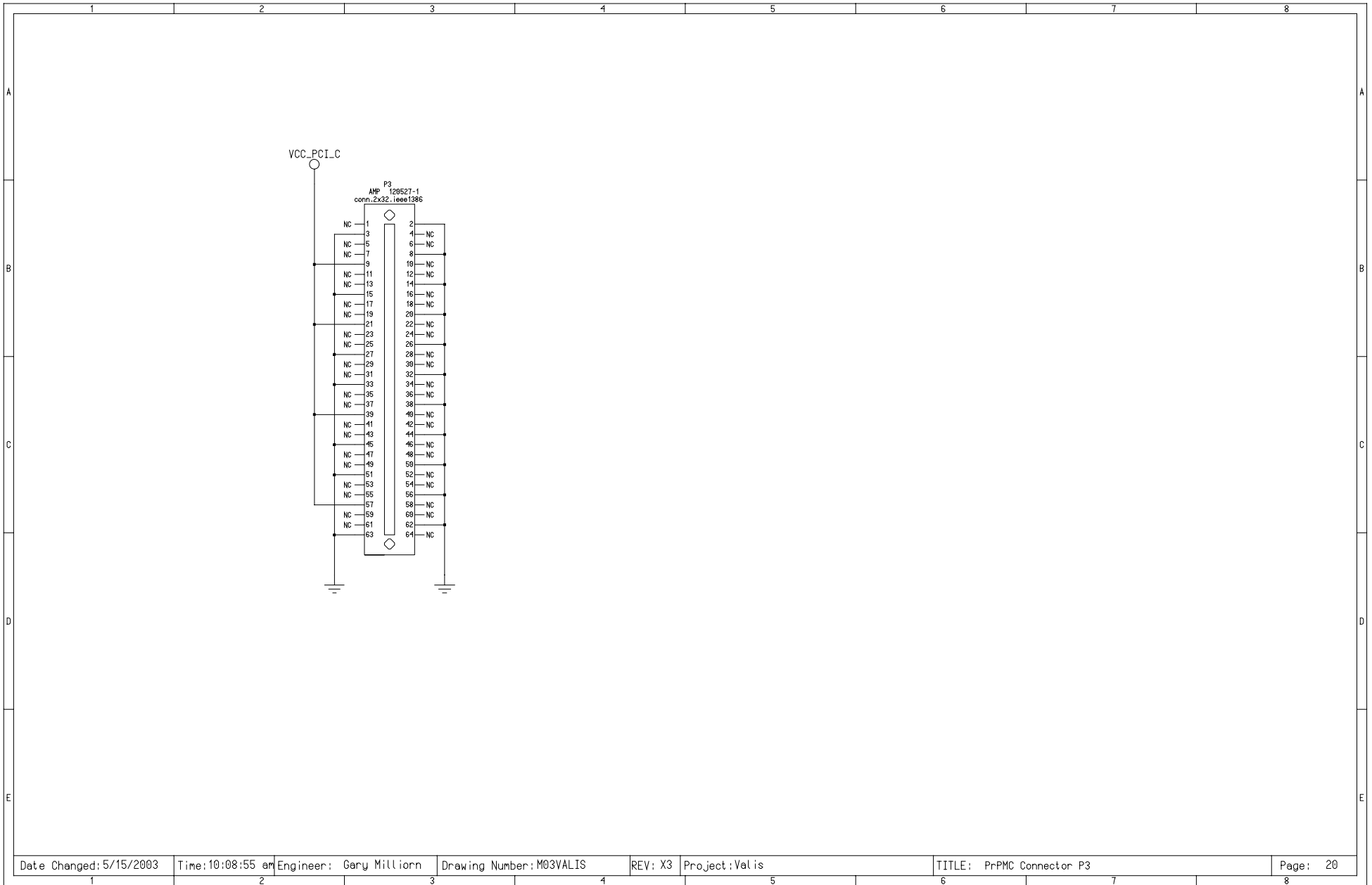


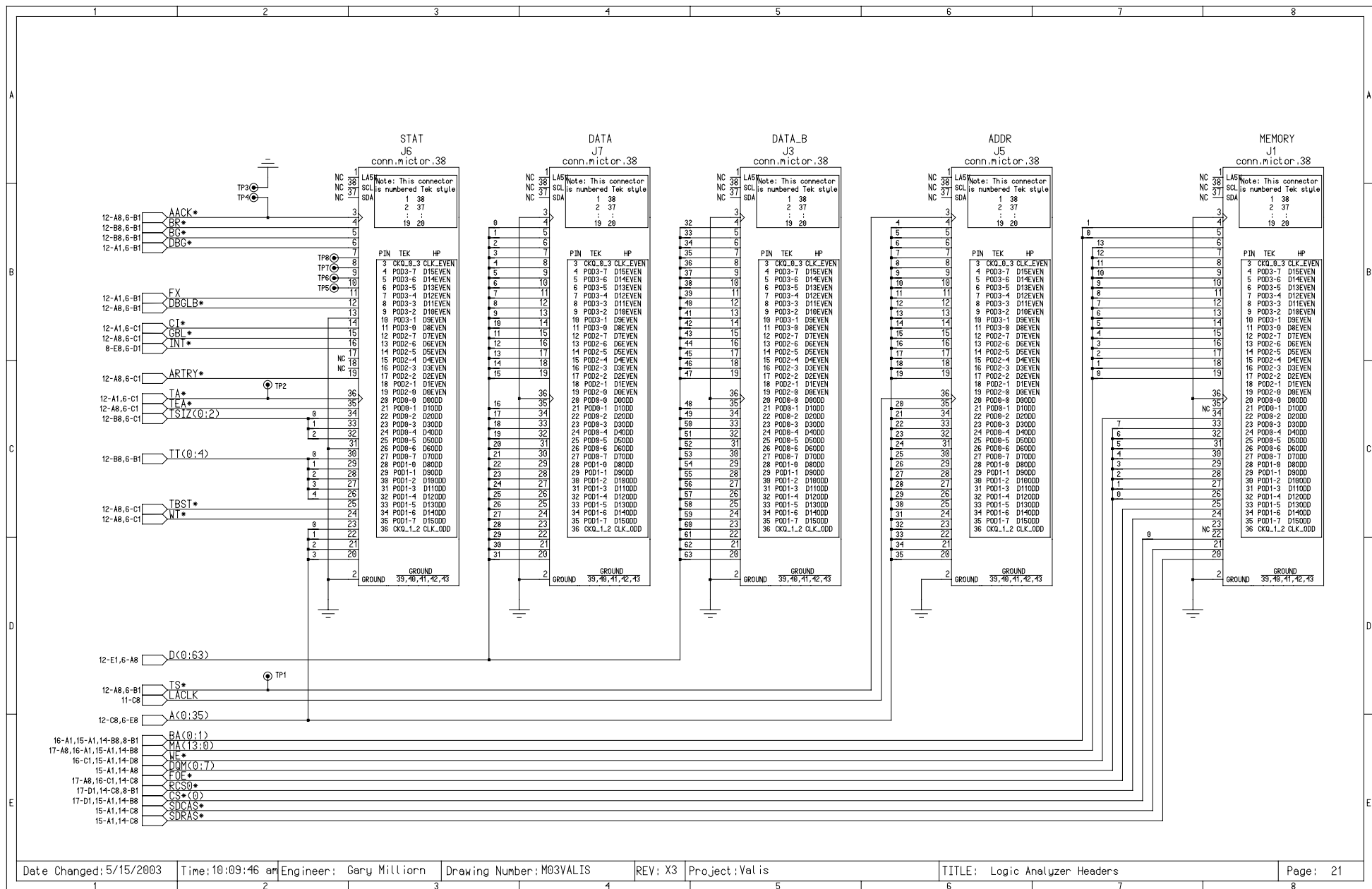




PCI VIO SELECTION
 V1 on 3.3V; MUST match NPMC carrier
 (Sandpoint, Arcadia, etc.)







	1	2	3	4	5	6	7	8											
A																			A
B																			B
C																			C
D																			D
E																			E

	1	2	3	4	5	6	7	8
A								
B								
C								
D								
E								

	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE	NET SH-ZONE
DP(7)	21E1	1901	10E8	16A1	MA(13)	MD(4)	15E8	17C8	MD(60)	15E8	17C8	16A1	QACK*	SDCLK3	TS*	12B8	
6D8	DOM(9:7)	IDSEL107	LACK	18A8	14B8	14A1	16A8	MD(12)	14A1	16A8	MD(58)	MDP(8)	6B1	14D8	6B1	12B8	
12D8	14A8	13E1	11C8	21E1	15A1	15E8	17C8	14A1	15E8	17C8	14A1	14D8	SD8	15A1	12A8	21C1	
DP(4)	15A1	16A8	21D1	MA(9)	16A1	16A8	MD(13)	15E8	16A8	MD(44)	15E8	15E8	12E8	SDCLK4	17B8	VID(6)	
6D8	21E1	14B8	LBCLAJM*	14B8	18A8	17C8	14A1	16A8	17C8	14A1	16A8	16A1	QREQ*	14D8	21D1	SC1	
12D8	FLASH_LED*	6D1	12B8	15A1	21E1	MD(5)	15E8	17C8	MD(57)	15E8	17C8	MDP(5)	6B1	15A1	TSIZ(6)	SA1	
DP(1)	17D8	17D8	17C8	16A1	MA(6)	14A1	15A8	MD(8)	14A1	16A8	MD(45)	14D8	12E8	SDRAW_LED*	6C1	VID(4)	
6D8	18C1	21B1	18A8	14B8	15E8	17C8	14A1	15E8	17C8	14A1	15E8	15E8	RCSB*	17C2	12B8	SC1	
12D8	FOE*	11B1	17D2	18A8	15A1	16A8	MD(23)	15E8	16A8	MD(43)	15E8	16A1	SC1	18C1	17B8	SA1	
DP(8)	14C8	13C8	18A8	18A8	MA(3)	MD(7)	15E8	17C8	14A1	15E8	MDP(1)	14C8	SDRAS*	18C1	21C1	VID(2)	
6D8	16C1	13C8	17D2	15A1	21E1	14A1	16A8	MD(26)	14A1	15E8	MD(56)	17C8	14D8	14C8	TSIZ(2)	SC1	
12D8	18A8	15C8	18C1	16A1	MA(11)	15E8	17C8	14A1	15E8	17C8	MD(18)	15E8	21E1	15A1	6C1	SA1	
DP(5)	21E1	19C8	18C1	16A1	MA(11)	15E8	17C8	14A1	15E8	17C8	MD(56)	17C8	14D8	14C8	TSIZ(2)	SC1	
6D8	FRAME*	13C8	17D2	15A1	21E1	14A1	16A8	MD(27)	15E8	16A8	MD(40)	14C8	14B8	14B8	21C1	SA1	
12D8	19C1	11B1	18C1	18C1	MA(8)	MD(17)	15E8	17C8	MD(24)	15E8	17C8	15E8	17C2	17B2	TSIZ(1)	VID(1)	
DP(3)	FX	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	17C2	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	19C1	11B1	18C1	18C1	MA(13:8)	16A8	MD(23)	15E8	16A8	MD(39)	15E8	14D8	17B2	17B2	VID(4:8)	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
12D8	6C1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
DP(8:7)	21B1	19E8	18A8	14B8	18A8	14A1	16A8	MD(38)	14A1	16A8	MD(46)	16A1	14C8	SENSE_PC1*	6C1	SC1	
6D8	GBL*	19E8	18A8	14B8	18A8												

1	2	3	4	5	6	7	8																
A								A															
B								B															
C								C															
D								D															
E								E															
<table><tr><th>REFDES</th><th>GND</th><th>OVDD</th><th>VCC_3.3</th></tr><tr><td>J1 J3 J5 J6 J7 RN1 RN2 RN4 RN9 RN16 RN12 RN13 RN14 RN16 RN17 RN18 RN19 U1 U2 U3 U4 U5 U6 U7 U8 U9 U12 U15 U16 U17 U18</td><td>39 40 41 42 43 4 54 52 46 41 28 12 6 27 46 11 26 38 43 59 74 86 95 C3 C6 C9 C12 C15 C18 C21 C23 E3 F6 F10 F16 F20 F23 G8 G11 G13 G15 G18 H3 H7 H19 J23 K5 K20 L3 L7 L19 M23 N7 N19 P3 P7 P19 R23 T6 T20 U3 V7 Y19 V23 W8 W11 W13 W15 W18 Y3 Y6 Y10 Y16 Y19 Y20 AA21 AB22 AC3 AC5 AC8 AC11 AC14 AC17 AC20 AC23 AD24 AE25 A22 B12 B14 B16 B18 B20 C21 D13 D15 D17 D19 E21 F10 F12 F14 F16 F19 G17 G21 H13 H15 H19 J17 J21 K15 K19 L17 L21 M19 N17 N21 P15 P19 R17 R21 T15 T19 U17 U21 V19 W17 W21 Y20 AB22 J10 J12 J14 K9 K11 K13 L10 L12 L14 M9 M11 M13 M19 N12 N14 P3 P11 P13 B1 B6 C3 C9 D7 E2 E5 G4 G7 H5 J5 K5 M3 M6 P3 T4 T7 T9 T13 V2 V5 V8 V12 V15 W7 Y3 Y9 Y13 Y15 AA5 AA17 AB1 C1 A1 E1 G1 J1 L1 M1 R1 U1 E3 G3 J3 L3 N3 B4 D4 G4 K4 P4 T4 B6 D6 G6 K6 P6 T6 E7 G7 J7 L7 N7 A5 C5 E5 G5 J5 L5 N5 R5 U5</td><td>9 10 39 91</td><td>9 10 8 49 43 27 14 9 3 1 37</td></tr></table>								REFDES	GND	OVDD	VCC_3.3	J1 J3 J5 J6 J7 RN1 RN2 RN4 RN9 RN16 RN12 RN13 RN14 RN16 RN17 RN18 RN19 U1 U2 U3 U4 U5 U6 U7 U8 U9 U12 U15 U16 U17 U18	39 40 41 42 43 4 54 52 46 41 28 12 6 27 46 11 26 38 43 59 74 86 95 C3 C6 C9 C12 C15 C18 C21 C23 E3 F6 F10 F16 F20 F23 G8 G11 G13 G15 G18 H3 H7 H19 J23 K5 K20 L3 L7 L19 M23 N7 N19 P3 P7 P19 R23 T6 T20 U3 V7 Y19 V23 W8 W11 W13 W15 W18 Y3 Y6 Y10 Y16 Y19 Y20 AA21 AB22 AC3 AC5 AC8 AC11 AC14 AC17 AC20 AC23 AD24 AE25 A22 B12 B14 B16 B18 B20 C21 D13 D15 D17 D19 E21 F10 F12 F14 F16 F19 G17 G21 H13 H15 H19 J17 J21 K15 K19 L17 L21 M19 N17 N21 P15 P19 R17 R21 T15 T19 U17 U21 V19 W17 W21 Y20 AB22 J10 J12 J14 K9 K11 K13 L10 L12 L14 M9 M11 M13 M19 N12 N14 P3 P11 P13 B1 B6 C3 C9 D7 E2 E5 G4 G7 H5 J5 K5 M3 M6 P3 T4 T7 T9 T13 V2 V5 V8 V12 V15 W7 Y3 Y9 Y13 Y15 AA5 AA17 AB1 C1 A1 E1 G1 J1 L1 M1 R1 U1 E3 G3 J3 L3 N3 B4 D4 G4 K4 P4 T4 B6 D6 G6 K6 P6 T6 E7 G7 J7 L7 N7 A5 C5 E5 G5 J5 L5 N5 R5 U5	9 10 39 91	9 10 8 49 43 27 14 9 3 1 37								
REFDES	GND	OVDD	VCC_3.3																				
J1 J3 J5 J6 J7 RN1 RN2 RN4 RN9 RN16 RN12 RN13 RN14 RN16 RN17 RN18 RN19 U1 U2 U3 U4 U5 U6 U7 U8 U9 U12 U15 U16 U17 U18	39 40 41 42 43 4 54 52 46 41 28 12 6 27 46 11 26 38 43 59 74 86 95 C3 C6 C9 C12 C15 C18 C21 C23 E3 F6 F10 F16 F20 F23 G8 G11 G13 G15 G18 H3 H7 H19 J23 K5 K20 L3 L7 L19 M23 N7 N19 P3 P7 P19 R23 T6 T20 U3 V7 Y19 V23 W8 W11 W13 W15 W18 Y3 Y6 Y10 Y16 Y19 Y20 AA21 AB22 AC3 AC5 AC8 AC11 AC14 AC17 AC20 AC23 AD24 AE25 A22 B12 B14 B16 B18 B20 C21 D13 D15 D17 D19 E21 F10 F12 F14 F16 F19 G17 G21 H13 H15 H19 J17 J21 K15 K19 L17 L21 M19 N17 N21 P15 P19 R17 R21 T15 T19 U17 U21 V19 W17 W21 Y20 AB22 J10 J12 J14 K9 K11 K13 L10 L12 L14 M9 M11 M13 M19 N12 N14 P3 P11 P13 B1 B6 C3 C9 D7 E2 E5 G4 G7 H5 J5 K5 M3 M6 P3 T4 T7 T9 T13 V2 V5 V8 V12 V15 W7 Y3 Y9 Y13 Y15 AA5 AA17 AB1 C1 A1 E1 G1 J1 L1 M1 R1 U1 E3 G3 J3 L3 N3 B4 D4 G4 K4 P4 T4 B6 D6 G6 K6 P6 T6 E7 G7 J7 L7 N7 A5 C5 E5 G5 J5 L5 N5 R5 U5	9 10 39 91	9 10 8 49 43 27 14 9 3 1 37																				
<table><tr><td>Date Changed: 5/15/2003</td><td>Time: 8:16:37 am</td><td>Engineer: Gary Million</td><td>Drawing Number: M03VALIS</td><td>REV: X3</td><td>Project: Valis</td><td>TITLE: Power/Ground Tables</td><td>Page: 24</td></tr><tr><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td></tr></table>								Date Changed: 5/15/2003	Time: 8:16:37 am	Engineer: Gary Million	Drawing Number: M03VALIS	REV: X3	Project: Valis	TITLE: Power/Ground Tables	Page: 24	1	2	3	4	5	6	7	8
Date Changed: 5/15/2003	Time: 8:16:37 am	Engineer: Gary Million	Drawing Number: M03VALIS	REV: X3	Project: Valis	TITLE: Power/Ground Tables	Page: 24																
1	2	3	4	5	6	7	8																

1	2	3	4	5	6	7	8								