



# Calypso Customer EVB 176QFP Daughter Card (X-MPC574XG-176DS)

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## Revision Information

Rev	Date	Designer	Comments
X1	11 Mar 2013	Alasdair Robertson	Initial release sent for review based on X-MPC574XG-324DS X2
X2	13 Mar 2013	Alasdair Robertson	Version sent to Pre Layout, incorporating fixes from review
X3	15 Mar 2013	Alasdair Robertson	Component consolodation, Added MCU GND tab. Sent to Layout
X4	29 Mar 2013	Alasdair Robertson	Changes made during layout to Daughtercard Connectors
X5	15 Apr 2013	Alasdair Robertson	LAY RefDes Re-Sequence & SCH Back-Annotate
A	15 Apr 2013	Alasdair Robertson	Post Layout (Back Annotated). Matches PCB RevA
B	22 Jul 2013	Alasdair Robertson	Update to accomodate extra socket pins on MCU
C	19 Nov 2013	Jesus Sanchez	The socket was updated, exposed center PAD is grounded.
D	19 Dec 2013	Jesus Sanchez	Changes on MCU Power to validate Calypso 3M

### Caution:

These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

### Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2. 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points are denoted TPx
- Test point Vias are denoted TPVx

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in *ITALICS*

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Designer: A. Robertson	Drawing Title: <b>Calypso 176 QFP Daughter Card</b>		
Drawn by: A. Robertson	Page Title: <b>Index and Title Page</b>		
Approved: A. Robertson	Size B	Document Number SCH-27898 PDF: SPF-27898	Rev D
Date: Friday, December 20, 2013	Sheet 1 of 8		

**Caution:**

- If VDD\_HV\_A is driven from 5V, the VDD\_HV\_FL A pin must not be supplied from 3.3V (remove the HVA\_FL A jumper)
- Don't attempt to over drive an analogue pad to 5V when the digital VDD\_HV\_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD\_HV\_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD\_HV\_A domain

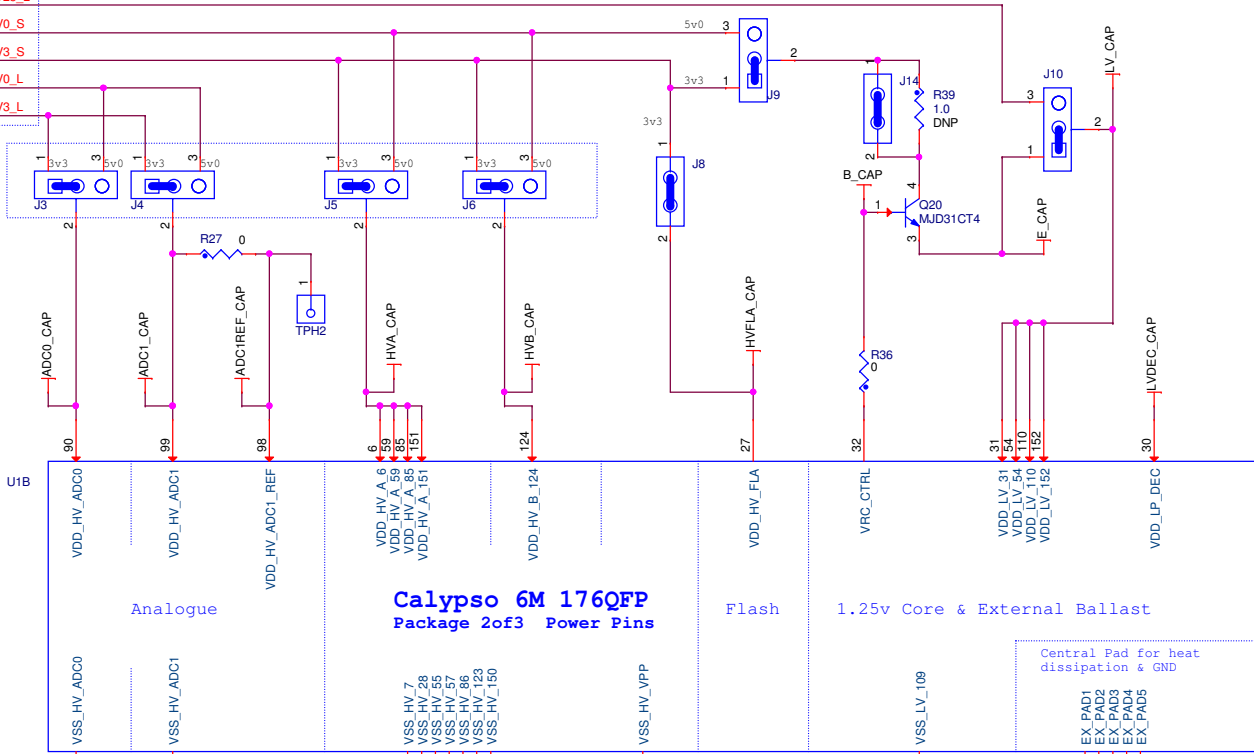
**Default Configuraiton:**

- ALL MCU supply voltages are set to 3.3V (ADC0, ADC1, VDD\_HV\_A, VDD\_HV\_B, VDD\_HV\_C, VBallast)
- VDD\_HV\_FL A = External 3.3V supplied (jumper fitted)
- VDD\_LV Supplied from ballast transistor

This is not necessarily the same as the default shown in the RM. All VDD\_HV\_x domains have at least one peripheral that only functions at 3.3V. Therefore the default is to run these from 3.3V. The analogue pins can only be driven to the same voltage as the VDD\_HV\_x domain they are situated in (ie max 3.3V) so makes sense for the analogue supply and reference to be 3.3V

- From MCU supply jumpers on main board
- 8 MCU\_1V25\_L >> MCU\_1V25\_L
  - 8 MCU\_5V0\_S >> MCU\_5V0\_S
  - 8 MCU\_3V3\_S >> MCU\_3V3\_S
  - 8 MCU\_5V0\_L >> MCU\_5V0\_L
  - 8 MCU\_3V3\_L >> MCU\_3V3\_L

Individual MCU supply control jumpers



Individual MCU supply control jumpers

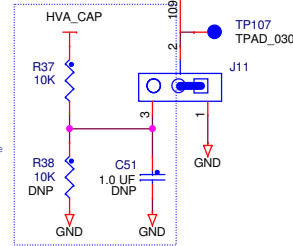
**Differences to 324BGA**

- 2 fewer VDD\_HV\_A on 176QFP
- 1 fewer VDD\_HV\_B
- No VDD\_HV\_C
- 5 Fewer VDD\_LV
- No VIN1\_CMP\_REF
- 15 Fewer VSS\_LV
- 5 Fewer VSS\_HV
- Heat Dissipation GND TAB

Ground Links (0 Ohm Resistors)



Calypso 3M INT\_BAL\_SELECT enable

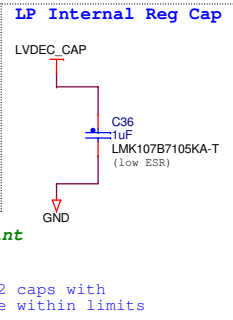
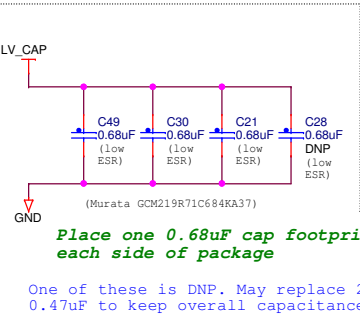
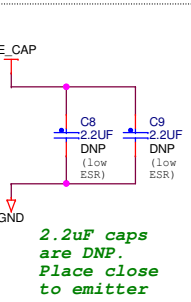
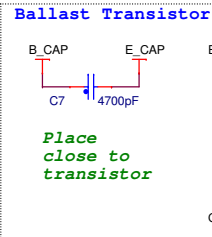
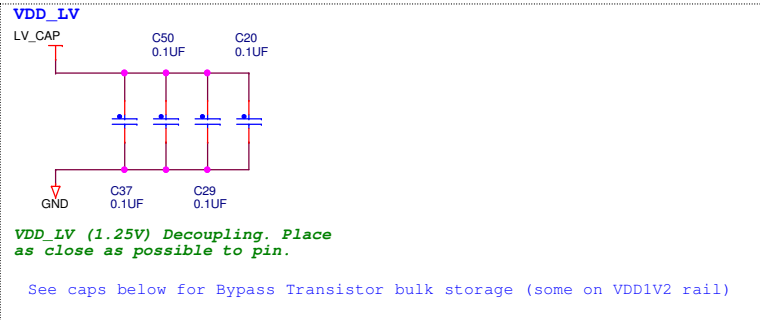
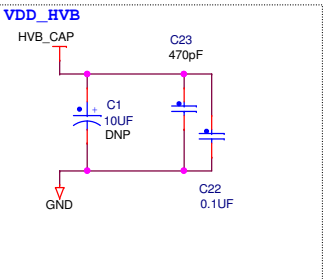
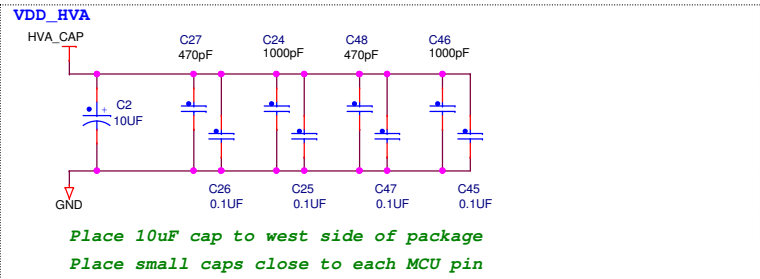
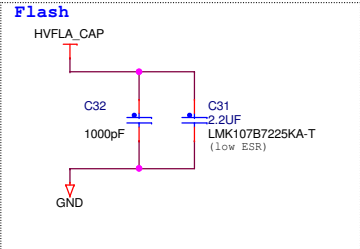
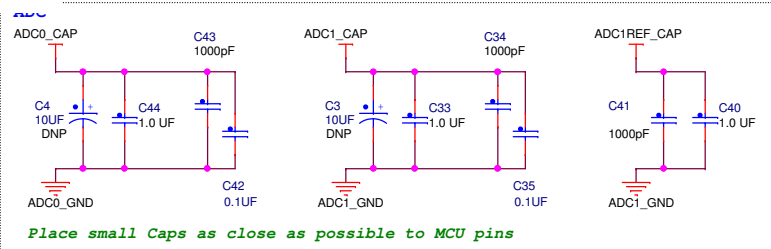


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Drawing Title: <b>Calypso 176 QFP Daughter Card</b>			
Page Title: <b>Calypso MCU Power</b>			
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Capacitor Types:

- 470pF - Ceramic COG, 50v 5% 0402
- 1000pF - Ceramic COG, 50V 5% 0402
- 4700pF - Ceramic X7R, 50V 10% 0402
- 0.01uF - Ceramic X7R, 50V 10% 0402
- 0.1uF - Ceramic X7R, 16V 10% 0402
- 0.68uF - Ceramic X7R 16V 10% 0805 (Murata GCM219R71C684KA37)
- 1.0uF - Ceramic X7R, 10V 10% 0603 (Taiyo Yuden LMK107B7105KA-T)
- 2.2uF - Ceramic X7R, 10V, 10%, 0603 (Taiyo Yuden LMK107B7225KA-TR)
- 4.7uF - TANT, 12.5V 20% ESR=0.08R 7343
- 10uF - TANT, 35V 10% ESR=0.125R CC7343-31
- 4.7uF Alternative (150-78844)- Polymer ALU, 16V 20% ESR=0.08R 7343-18



Differences to 324BGA

- 2 Fewer VDD\_HV\_A capacitor pairs
- 1 fewer VDD\_HV\_B capacitor pair
- No VDD\_HV\_C capacitor pairs
- 5 fewer VDD\_LV capacitor pairs

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U1A

**Calypso 176QFP**  
Package 1of3 GPIO Pins1

\*\* PA1 is also NMI. Routed to I/O Matrix (WKP2 / NMIO) (WKP3)

Key to text colours:  
 Purple - Comms Physical Interfaces  
 Orange - Other Peripherals and I/O  
 Blue - Debug (JTAG & Nexus)  
 Black - Clock, Reset and Control  
 Red - I/O Matrix and other functions (eg LED)  
 Green - I/O Matrix (dedicated)

8	PA0	((SD_CD - WKP19) PA0	24	PA0
8	PA1	((SW1 & GPIO**) PA1	19	PA1
8	PA2	((SW2 & GPIO) PA2	17	PA2
8	PA3	((RMI_RXD1) PA3	114	PA3
8	PA4	((CMP1_13 / IO) PA4	51	PA4
8	PA5	((SAI_GPIO) PA5	146	PA5
8	PA6	((MLB_GPIO) PA6	147	PA6
8	PA7	((MII_RXD2) PA7	128	PA7
8	PA8	((RMI_RXD1) PA8	129	PA8
8	PA9	((RMI_RXD0) PA9	130	PA9
8	PA10	((MII_RXD1) PA10	131	PA10
8	PA11	((RMI_RXD0) PA11	132	PA11
8	PA12	((CMP1_15 / IO) PA12	53	PA12
8	PA13	((CMP1_14 / IO) PA13	52	PA13
8	PA14	((CMP1_12 / IO) PA14	50	PA14
8	PA15	((CMP1_10 / IO) PA15	48	PA15
8	PB0	((CAN0_TX) PB0	39	PB0
8	PB1	((CAN0_RX) PB1	40	PB1
8	PB2	((LINC_TX) PB2	176	PB2
8	PB3	((LINC_RX) PB3	1	PB3
8	PB4	((ADC_POT) PB4	88	PB4
8	PB5	((GPIO) PB5	91	PB5
8	PB6	((GPIO) PB6	92	PB6
8	PB7	((GPIO) PB7	93	PB7
8	PB8	((XTAL32) PB8	61	PB8
8	PB9	((EXTAL32) PB9	60	PB9
8	PB10	((SAI0_SYNC) PB10	62	PB10
8	PB11	((GPIO) PB11	96	PB11
8	PB12	((GPIO) PB12	101	PB12
7	PB13	((MLB_DRN) PB13	103	PB13
7	PB14	((MLB_SN) PB14	105	PB14
7	PB15	((MLB_CN / SIG) PB15	107	PB15
8	PC0	((TDI) PC0	154	PC0
8	PC1	((TDO) PC1	149	PC1
8	PC2	((USB1_CLK) PC2	145	PC2
8	PC3	((USB1_DIR) PC3	144	PC3
8	PC4	((FR_B_TX_EN) PC4	159	PC4
8	PC5	((FR_A_TX) PC5	158	PC5
8	PC6	((LINC_TX) PC6	44	PC6
8	PC7	((LINC_RX) PC7	45	PC7
8	PC8	((RS232_TX) PC8	175	PC8
8	PC9	((RS232_RX) PC9	2	PC9
8	PC10	((CAN1_TX) PC10	36	PC10
8	PC11	((CAN1_RX) PC11	35	PC11
8	PC12	((FR_DBG0) PC12	173	PC12
8	PC13	((FR_DBG1) PC13	174	PC13
8	PC14	((FR_DBG2) PC14	3	PC14
8	PC15	((FR_DBG3) PC15	4	PC15
8	PD0	((HEX1 & GPIO) PD0	77	PD0
8	PD1	((HEX2 & GPIO) PD1	78	PD1
8	PD2	((HEX3 & GPIO) PD2	79	PD2
8	PD3	((HEX4 & GPIO) PD3	80	PD3
8	PD4	((GPIO) PD4	81	PD4
8	PD5	((GPIO) PD5	82	PD5
8	PD6	((GPIO) PD6	83	PD6
8	PD7	((GPIO) PD7	84	PD7
8	PD8	((GPIO) PD8	87	PD8
8	PD9	((GPIO) PD9	94	PD9
8	PD10	((GPIO) PD10	95	PD10
8	PD12	((GPIO) PD12	100	PD12
8	PD13	((GPIO & MLB_ST) PD13	102	PD13
7	PD14	((MLB_DP) PD14	104	PD14
7	PD15	((MLB_SP / DAT) PD15	106	PD15
8	MCU-RSTx	MCU-RSTx	29	RESET
8	PORSTx	PORSTx	153	PORST
6	MCU-XTAL	MCU-XTAL	56	XTAL
6	MCU-EXTAL	MCU-EXTAL	58	EXTAL

PE0	18	PE0	((MLB_I2C1_SCL)	PE0	8
PE1	20	PE1	((MLB_I2C1_SDA)	PE1	8
PE2	156	PE2	((FR_A_TX_EN)	PE2	8
PE3	157	PE3	((FR_A_TX)	PE3	8
PE4	160	PE4	((FR_B_TX)	PE4	8
PE5	161	PE5	((FR_B_RX)	PE5	8
PE6	167	PE6	((SD_CMD)	PE6	8
PE7	168	PE7	((SD_CLK)	PE7	8
PE8	21	PE8	((SAI_I2C2_SDA)	PE8	8
PE9	22	PE9	((SAI_I2C2_SCL)	PE9	8
PE10	25	PE10	((SAI_I2C3_SDA)	PE10	8
PE11	133	PE11	((MII_CRD)	PE11	8
PE12	127	PE12	((MII_RXD3)	PE12	8
PE13	136	PE13	((USB1_D2)	PE13	8
PE14	137	PE14	((USB1_D3)	PE14	8
PE15				PE15	8
PF0	63	PF0	((SAI0_MCLK)	PF0	8
PF1	64	PF1	((SAI0_BCLK)	PF1	8
PF2	65	PF2	((SAI0_D3)	PF2	8
PF3	66	PF3	((SAI0_D2)	PF3	8
PF4	67	PF4	((SAI0_D1)	PF4	8
PF5	68	PF5	((SAI0_D0)	PF5	8
PF6	69	PF6	((SAI1_SYNC)	PF6	8
PF7	70	PF7	((SAI1_MCLK)	PF7	8
PF8	42	PF8	((GPIO)	PF8	8
PF9	41	PF9	((SW3 & GPIO) WKP22)	PF9	8
PF10	46	PF10	((CMP1_8 / IO)	PF10	8
PF11	47	PF11	((SW4 & GPIO) WKP15)	PF11	8
PF12	43	PF12	((GPIO)	PF12	8
PF13	49	PF13	((CMP1_11 / IO)	PF13	8
PF14	128	PF14	((RMI_RXD1)	PF14	8
PF15	125	PF15	((RMI_RXD0)	PF15	8
PG0	122	PG0	((RMI_MDC)	PG0	7
PG1	121	PG1	((RMI_TXCLK)	PG1	8
PG2	16	PG2	((LED1 & GPIO)	PG2	8
PG3	15	PG3	((LED2 & GPIO)	PG3	8
PG4	14	PG4	((LED3 & GPIO)	PG4	8
PG5	13	PG5	((LED4 & GPIO)	PG5	8
PG6	38	PG6	((CLKOUT1 GPIO)	PG6	8
PG7	37	PG7	((CLKOUT0 GPIO)	PG7	8
PG8	34	PG8	((GPIO)	PG8	8
PG9	33	PG9	((MLB_IRQ - WKP21)	PG9	8
PG10	138	PG10	((USB1_D4)	PG10	8
PG11	139	PG11	((USB1_D5)	PG11	8
PG12	116	PG12	((MII_TXD2)	PG12	7
PG13	115	PG13	((MII_TXD3)	PG13	7
PG14	134	PG14	((USB1_D0)	PG14	8
PG15	135	PG15	((USB1_D1)	PG15	8
PH0	117	PH0	((RMI_TXD1)	PH0	7
PH1	118	PH1	((RMI_TXD0)	PH1	7
PH2	119	PH2	((RMI_TXEN)	PH2	7
PH3	120	PH3	((eMIOS1_OC_SH)	PH3	8
PH4	162	PH4	((eMIOS1_OC_SH)	PH4	8
PH5	163	PH5	((eMIOS1_OC_TH)	PH5	8
PH6	164	PH6	((MLB_RST)	PH6	8
PH7	165	PH7	((MLB_PRR)	PH7	8
PH8	166	PH8	((SD_WP)	PH8	8
PH9	155	PH9	((TCK)	PH9	8
PH10	148	PH10	((TMS)	PH10	8
PH11	140	PH11	((USB1_D6)	PH11	8
PH12	141	PH12	((USB1_D7)	PH12	8
PH13	9	PH13	((GPIO)	PH13	8
PH14	10	PH14	((GPIO)	PH14	8
PH15	8	PH15	((GPIO)	PH15	8

(eMIOS1\_EIUC\_11\_H)  
(eMIOS1\_EIUC\_12\_H)  
(eMIOS1\_EIUC\_13\_H)  
(eMIOS1\_EIUC\_14\_H)

Differences to 324BGA  
- Port D 11 Not on 176QFP

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- Purple - Comms Physical Interfaces
- Orange - Other Peripherals and I/O
- Blue - Debug (JTAG & Nexus)
- Black - Clock, Reset and Control
- RED - I/O Matrix and other functions (eg LED)
- Green - I/O Matrix (dedicated)

8	PI0	<<<<<<	(SD_D3)	PI0	172	PI0
8	PI1	<<<<<<	(SD_D2)	PI1	171	PI1
8	PI2	<<<<<<	(SD_D1)	PI2	170	PI2
8	PI3	<<<<<<	(SD_D0)	PI3	169	PI3
8	PI4	<<<<<<	(USB1_STP)	PI4	143	PI4
8	PI5	<<<<<<	(USB1_NXT)	PI5	142	PI5
8	PI6	<<<<<<	(USB0_RST)	PI6	11	PI6
8	PI7	<<<<<<	(USB1_RST)	PI7	12	PI7
7	PI8	<<<<<<	(MLB_GP / CLR)	PI8	108	PI8
		<<<<<<	(GPIO)			
8	PI11	<<<<<<	(ENET_RST)	PI11	111	PI11
8	PI12	<<<<<<	(GPIO & MLB_PS0)	PI12	112	PI12
8	PI13	<<<<<<	(GPIO & MLB_PS1)	PI13	113	PI13
8	PI14	<<<<<<	(SAI2_D0)	PI14	76	PI14
8	PI15	<<<<<<	(SAI2_MCLK)	PI15	75	PI15
8	PJ0	<<<<<<	(SAI2_SYNC)	PJ0	74	PJ0
8	PJ1	<<<<<<	(SAI2_BCLK)	PJ1	73	PJ1
8	PJ2	<<<<<<	(SAI1_D0)	PJ2	72	PJ2
8	PJ3	<<<<<<	(SAI1_BCLK)	PJ3	71	PJ3
8	PJ4	<<<<<<	(GPIO)	PJ4	5	PJ4

U1C



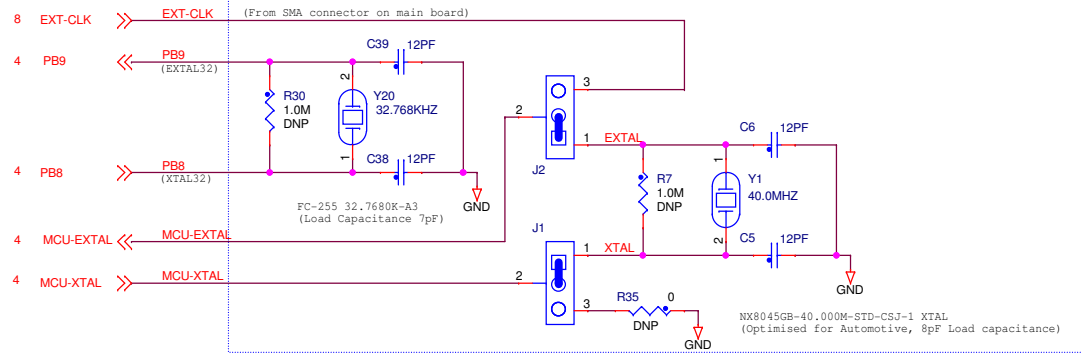
Calypso 176QFP  
Package 3of3 GPIO Pins2

Differences to 324BGA  
 - 2 fewer pins on Port I  
 - 12 fewer pins on Port J  
 - No Ports K to Q  
 (And corresponding changes to daughtercard connectors)

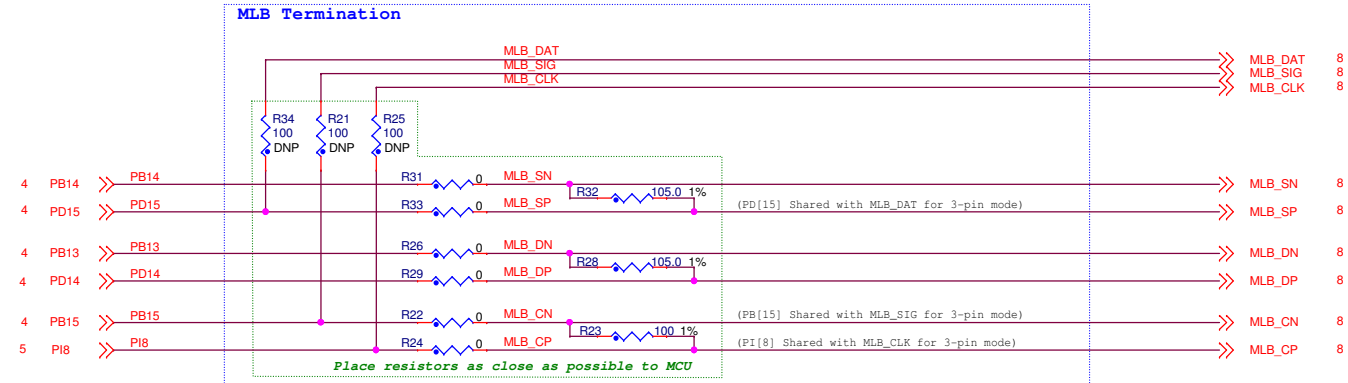
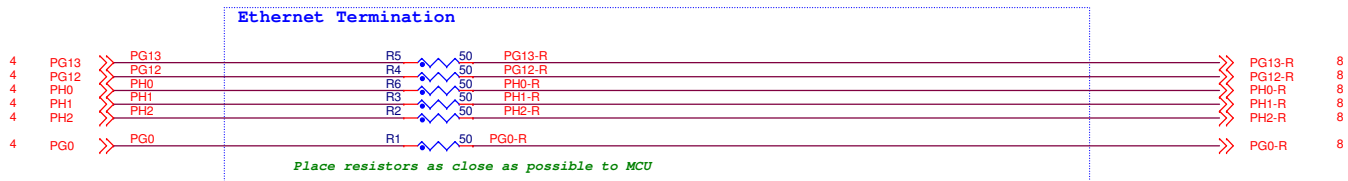
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### Oscillators and External Clock

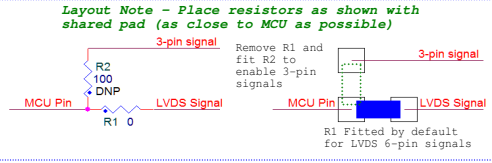


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From MCU

To Daughtercard



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Way to fit these connectors onto a B sized sheet so unfortunately the sheet size has been increased to C so will need to be printed on larger paper.

- The Crystal Signals are NOT routed via the daughtercard connectors
- The Specific MCU power pins are not routed via the daughter card however the jumpered MCU supply lines are brought up from the main board (see the top pins of the connector on the left)

The connector schematic symbols have been horizontally mirrored so they match the main EVB connector. This has no bearing on the PCB placement or footprint. Pin1 on the receptacle mates with pin 1 on the plug.

Connectors on Main board (Shown for reference)

