Calypso Customer EVB 256 BGA Daughter Card (X-MPC574XG-256DS)

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Revision Information

Rev	Date	Designer	Comments
X1	11 Mar 2013	Alasdair Robertson	Initial release sent for review based on X-MPC574XG-324DS X2
X2	13 Mar 2013	Alasdair Robertson	Version sent to Pre Layout, incorporating fixes from review
X3	15 Mar 2013	Alasdair Robertson	Component consolodation, Few minor changes. Sent to Layout
X4	29 Mar 2013	Alasdair Robertson	Changes made during layout to Daughtercard Connectors
X5	15 Apr 2013	Alasdair Robertson	LAY RefDes Re-Sequence & SCH Back-Annotate
A	15 Apr 2013	Alasdair Robertson	Post Layout (Back Annotated). Matches PCB RevA

Caution:

These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

Using Bolero 3M with the Calypso 256BGA daughter card:

- Pin C8 PORST on Calypso is VSS_LV on B3m. To use with B3M, Ground the PORST header (on the main board)

- Pin H2 VDD_HV_FLA on Calypso is VDD_HV_A on B3M. If VDD_HV_A is 3.3V then fit the VDD_HV_FLA jumper on Calyspo main board. If wanting to run VDD_HV_A at 5V then need to supply 5v to pin2 of the VDD_HV_FLA jumper

- Pin K2 VDD_LP_DEC on Calypso is VSS_LV on B3M. Replace LVDEC_CAP (1uF) with a zero ohm link to short pin to GND

- VSS_HV on Calypso is VDD_LV on B3M. No impact (both common grounds)

- Pin M9 VIN1_CMP_REF on Calypso is a Port on B3M. Remove jumper header from VIN1_CMP_REF pin

- Pin M10 VDD_HV_C on Calypso is a Port on B3M. Remove VDD_HV_C jumper header

- Pin M11 VDD_HV_ADC1 on Calypso is a port on B3M. Remove zero ohm link between HV_AD1 and ADC1_REF. There are also 2 caps on this pin that could be removed but should not pose a problem if pin is not used.

- Pin M12 Pm14 is PL11 on B3M. No issues, just be careful of pin assignments.

Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2. 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points are denoted TPx
- Test point Vias are denoted TPVx

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

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Designer: A. Robertson	Drawing Title: Calypso 256 BGA Daughter Card		
Drawn by: A. Robertson	Page Title: Index and Title Page		
Approved: A. Robertson	Size B	Document Number SCH-27899 PDF: SPF-27899	Rev A
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MCU Power Connections

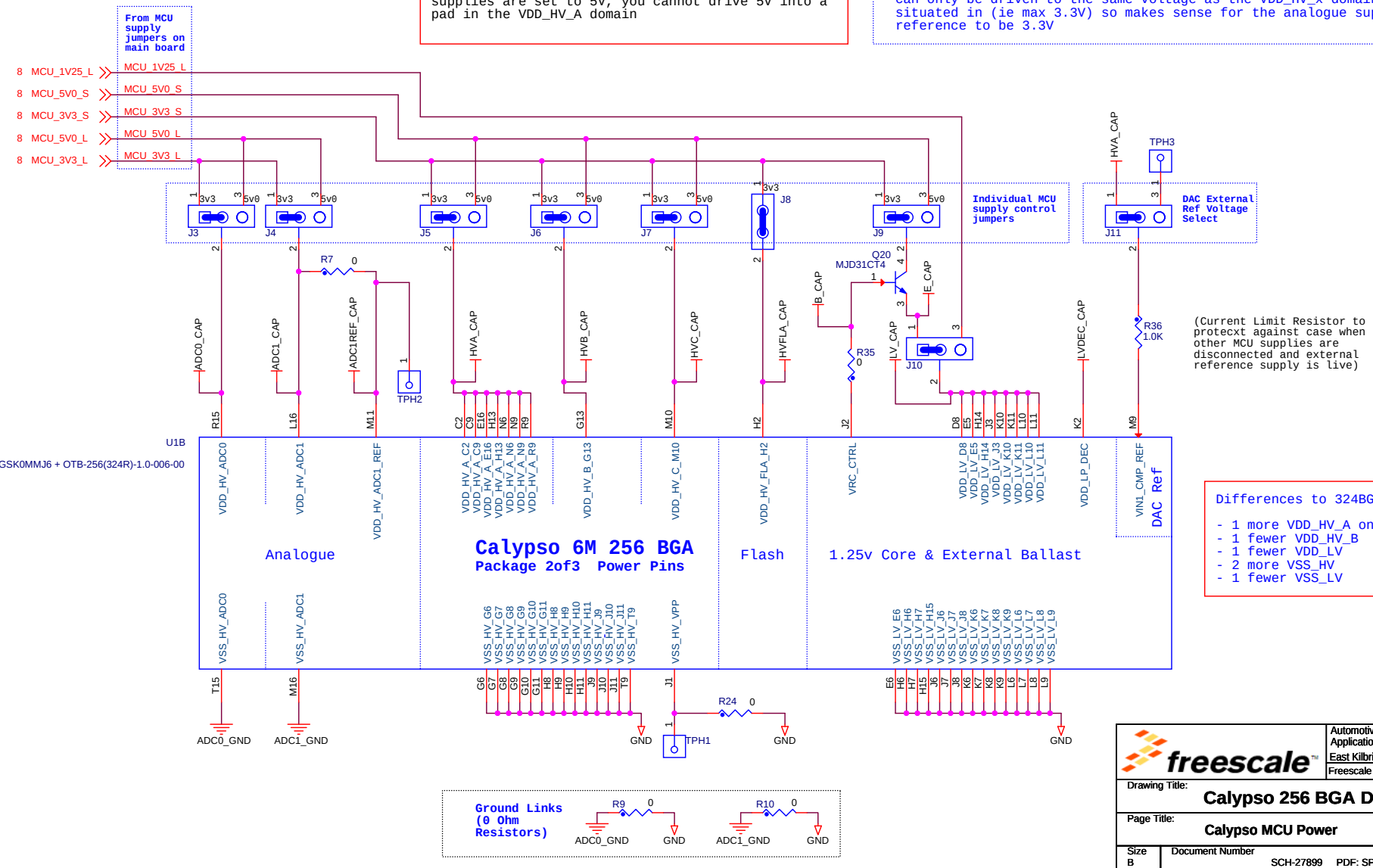
Caution:

- If VDD_HV_A is driven from 5V, the VDD_HV_FLA pin must not be supplied from 3.3V (remove the HVA_FLA jumper)

- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V. This will trigger the ESD protectrion on that pad. For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain

Default Configuraiton:
- ALL MCU supply voltages are set to 3.3V (ADC0, ADC1, VDD_HV_A, VDD_HV_B, VDD_HV_C, VBallast)
- VDD_HV_FLA = External 3.3V supplied (jumper fitted)
- VDD_LV Supplied from ballast transistor

This is not necessarily the same as the default shown in the RM. All VDD_HV_x domains have at least one peripheral that only functions at 3.3V. Therefore the default is to run these from 3.3V. The analogue pins can only be driven to the same voltage as the VDD_HV_x domain they are situated in (ie max 3.3V) so makes sense for the analogue supply and reference to be 3.3V



Differences to 324BGA

- 1 more VDD_HV_A on 256BGA
- 1 fewer VDD_HV_B
- 1 fewer VDD_LV
- 2 more VSS_HV
- 1 fewer VSS_LV

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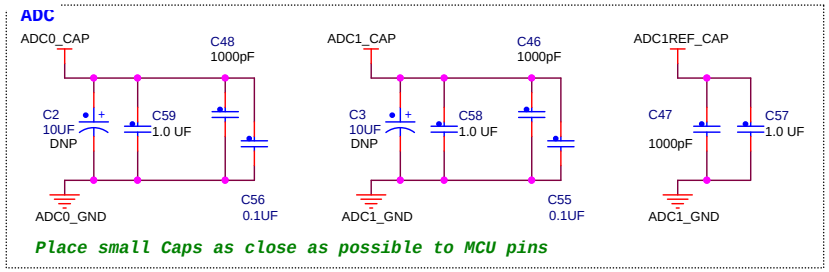
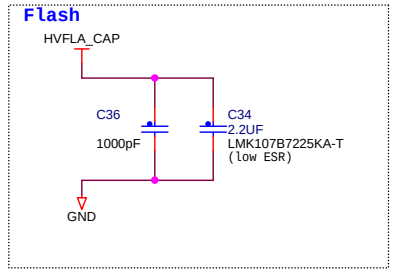
MCU Decoupling and bulk storage





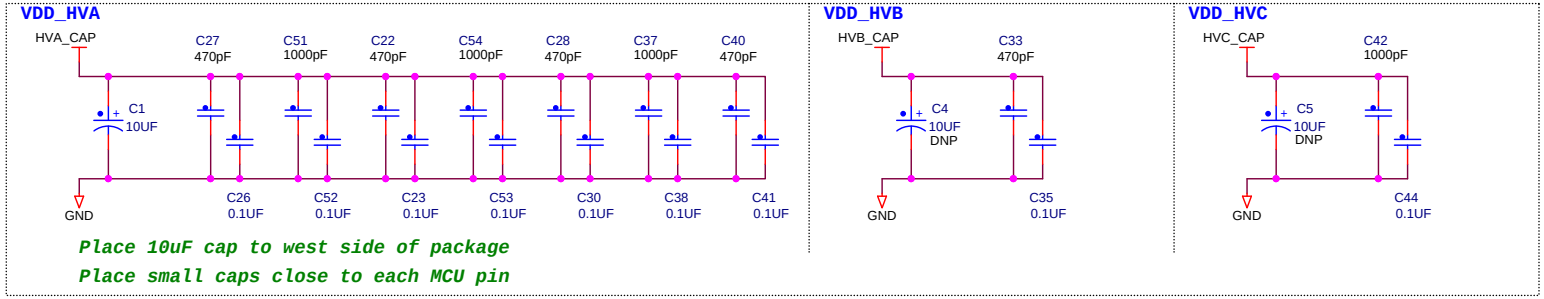
Capacitor Types:

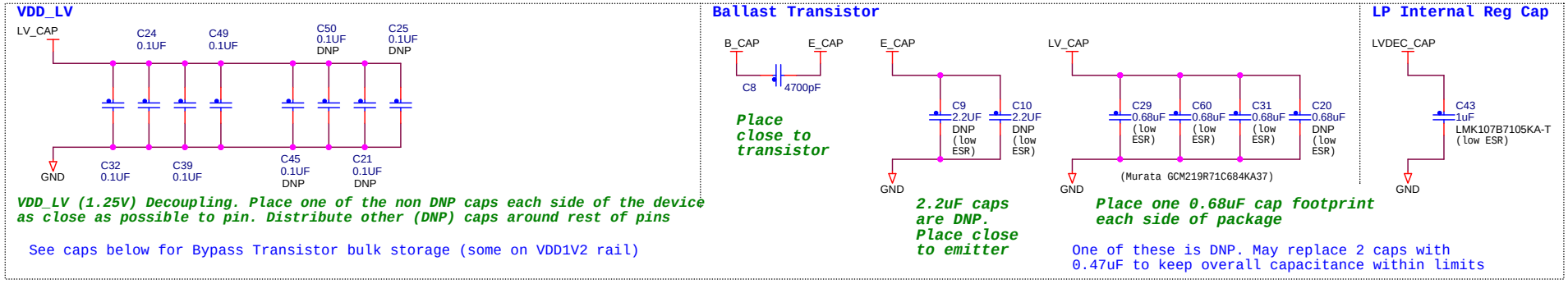
470pF - Ceramic COG, 50v 5% 0402
1000pF - Ceramic COG, 50V 5% 0402
4700pF - Ceramic X7R, 50V 10% 0402

0.01uF - Ceramic X7R, 50V 10% 0402
0.1uF - Ceramic X7R, 16V 10% 0402
0.68uF - Ceramic X7R 16V 10% 0805 (Murata GCM219R71C684KA37)
1.0uF - Ceraminc X7R, 10V 10% 0603 (Taiyo Yuden LMK107B7105KA-T)
2.2uF - Ceraminc X7R, 10V, 10%, 0603 (Taiyo Yuden LMK107B7225KA-TR)

4.7uF - TANT, 12.5V 20% ESR=0.08R 7343
10uF - TANT, 35V 10% ESR=0.125R CC7343-31

4.7uF Alternative (150-78844)- Polymer ALU, 16V 20% ESR=0.08R 7343-18





Differences to 324BGA

- 1 more VDD_HV_A capacitor pair
- 1 fewer VDD_HV_B capacitor pair
- 1 fewer VDD_LV capacitor (one of DNP caps)

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GPIO 1 of 2

U1A

Calypso 256 BGA

Package 1of3 GPIO Pins1

** PA1 is also NMI. Routed to I/O Matrix

(WKPU2 / NMI0)
(WKPU3)

Key to text colours:
- Purple - Comms Physical Interfaces
- Orange - Other Peripherals and I/O
- Blue - Debug (JTAG & Nexus)
- Black - Clock, Reset and Control
- RED - I/O Matrix and other functions (eg LED)
- Green - I/O Matrix (dedicated)

8	PA0	(SD_CD - WKPU19)	PA0	G4	PA0	G2	PE0	(MLB_I2C1_SCL)	PE0	8
8	PA1	(SW1 & GPIO**)	PA1	F3	PA1	F4	PE1	(MLB_I2C1_SDA)	PE1	8
8	PA2	(SW2 & GPIO)	PA2	F1	PA2	A7	PE2	(FR_A_TX_EN)	PE2	8
8	PA3	(MII_RXCLK)	PA3	G16	PA3	A10	PE3	(FR_A_RX)	PE3	8
8	PA4	(CMP1_13 / IO)	PA4	T2	PA4	A8	PE4	(FR_B_TX)	PE4	8
8	PA5	(SAI_GPIO)	PA5	C10	PA5	B8	PE5	(FR_B_RX)	PE5	8
8	PA6	(MLB_GPIO)	PA6	D11	PA6	B6	PE6	(SD_CMD)	PE6	8
8	PA7	(MII_RXD2)	PA7	C15	PA7	A5	PE7	(SD_CLK)	PE7	8
8	PA8	(RMII_RXD1)	PA8	B16	PA8	G1	PE8	(SAI_I2C2_SDA)	PE8	8
8	PA9	(RMII_RXD0)	PA9	B15	PA9	H1	PE9	(SAI_I2C2_SCL)	PE9	8
8	PA10	(MII_COL)	PA10	A15	PA10	G3	PE10	(SAI_I2C3_SDA)	PE10	8
8	PA11	(RMII_RXER)	PA11	B14	PA11	H3	PE11	(SAI_I2C3_SCL)	PE11	8
8	PA12	(CMP1_15 / IO)	PA12	P6	PA12	C14	PE12	(MII_CRS)	PE12	8
8	PA13	(CMP1_14 / IO)	PA13	R5	PA13	C16	PE13	(MII_RXD3)	PE13	8
8	PA14	(CMP1_12 / IO)	PA14	P4	PA14	A14	PE14	(USB1_D2)	PE14	8
8	PA15	(CMP1_10 / IO)	PA15	R2	PA15	C12	PE15	(USB1_D3)	PE15	8
8	PB0	(CAN0_TX)	PB0	L3	PB0	P7	PF0	(SAI0_MCLK)	PF0	8
8	PB1	(CAN0_RX)	PB1	M2	PB1	T6	PF1	(SAI0_BCLK)	PF1	8
8	PB2	(LIN0_TX)	PB2	A2	PB2	R6	PF2	(SAI0_D3)	PF2	8
8	PB3	(LIN0_RX)	PB3	D4	PB3	R7	PF3	(SAI0_D2)	PF3	8
8	PB4	(ADC_POT)	PB4	T16	PB4	R8	PF4	(SAI0_D1)	PF4	8
8	PB5	(GPIO)	PB5	N13	PB5	P8	PF5	(SAI0_D0)	PF5	8
8	PB6	(GPIO)	PB6	N14	PB6	N8	PF6	(SAI1_SYNC)	PF6	8
8	PB7	(GPIO)	PB7	R16	PB7	P9	PF7	(SAI1_MCLK)	PF7	8
6	PB8	(XTAL32)	PB8	T11	PB8	N2	PF8	(GPIO)	PF8	8
6	PB9	(EXTAL32)	PB9	T10	PB9	M4	PF9	(SW3 & GPIO) WKPU22	PF9	8
8	PB10	(SAI0_SYNC)	PB10	N7	PB10	P2	PF10	(CMP1_8 / IO)	PF10	8
8	PB11	(GPIO)	PB11	M13	PB11	R1	PF11	(SW4 & GPIO) WKPU15	PF11	8
8	PB12	(GPIO)	PB12	L14	PB12	P1	PF12	(GPIO)	PF12	8
7	PB13	(MLB_DN)	PB13	L15	PB13	P3	PF13	(CMP1_11 /IO)	PF13	8
7	PB14	(MLB_SN)	PB14	K15	PB14	D14	PF14	(RMII_MDIO)	PF14	8
7	PB15	(MLB_CN / SIG)	PB15	K16	PB15	D15	PF15	(RMII_RXDV)	PF15	8
8	PC0	(TDI)	PC0	B10	PC0	E13	PG0	(RMII_MDC)	PG0	7
8	PC1	(TDO)	PC1	D9	PC1	E14	PG1	(RMII_TXCLK)	PG1	8
8	PC2	(USB1_CLK)	PC2	B11	PC2	E4	PG2	(LED1 & GPIO)	PG2	8
8	PC3	(USB1_DIR)	PC3	C11	PC3	E1	PG3	(LED2 & GPIO)	PG3	8
8	PC4	(FR_B_TX_EN)	PC4	A9	PC4	F2	PG4	(LED3 & GPIO)	PG4	8
8	PC5	(FR_A_TX)	PC5	B9	PC5	D1	PG5	(LED4 & GPIO)	PG5	8
8	PC6	(LIN1_TX)	PC6	N3	PC6	M1	PG6	(CLKOUT1 GPIO)	PG6	8
8	PC7	(LIN1_RX)	PC7	N4	PC7	L2	PG7	(CLKOUT0 GPIO)	PG7	8
8	PC8	(RS232_TX)	PC8	B3	PC8	K3	PG8	(GPIO)	PG8	8
8	PC9	(RS232_RX)	PC9	C3	PC9	J4	PG9	(MLB_IRQ - WKPU21)	PG9	8
8	PC10	(CAN1_TX)	PC10	L1	PC10	B13	PG10	(USB1_D4)	PG10	8
8	PC11	(CAN1_RX)	PC11	K4	PC11	A16	PG11	(USB1_D5)	PG11	8
8	PC12	(FR_DBG0)	PC12	B4	PC12	F15	PG12	(MII_TXD2)	PG12	7
8	PC13	(FR_DBG1)	PC13	A3	PC13	F16	PG13	(MII_TXD3)	PG13	7
8	PC14	(FR_DBG2)	PC14	B2	PC14	C13	PG14	(USB1_D0)	PG14	8
8	PC15	(FR_DBG3)	PC15	A1	PC15	D13	PG15	(USB1_D1)	PG15	8
8	PD0	(HEX1 & GPIO)	PD0	R12	PD0	E15	PH0	(RMII_TXD1)	PH0	7
8	PD1	(HEX2 & GPIO)	PD1	T13	PD1	F13	PH1	(RMII_TXD0)	PH1	7
8	PD2	(HEX3 & GPIO)	PD2	N11	PD2	D16	PH2	(RMII_TXEN)	PH2	7
8	PD3	(HEX4 & GPIO)	PD3	R13	PD3	F14	PH3	(eMIOS1_UC_5H)	PH3	8
8	PD4	(GPIO)	PD4	P12	PD4	D7	PH4	(eMIOS1_UC_6H)	PH4	8
8	PD5	(GPIO)	PD5	T14	PD5	B7	PH5	(eMIOS1_UC_7H)	PH5	8
8	PD6	(GPIO)	PD6	R14	PD6	C7	PH6	(MLB_RST)	PH6	8
8	PD7	(GPIO)	PD7	P13	PD7	C6	PH7	(MLB_PWR)	PH7	8
8	PD8	(GPIO)	PD8	P14	PD8	A6	PH8	(SD_WP)	PH8	8
8	PD9	(GPIO)	PD9	N16	PD9	A11	PH9	(TCK)	PH9	8
8	PD10	(GPIO)	PD10	M14	PD10	D10	PH10	(TMS)	PH10	8
8	PD11	(GPIO)	PD11	M15	PD11	A13	PH11	(USB1_D6)	PH11	8
8	PD12	(GPIO)	PD12	L13	PD12	B12	PH12	(USB1_D7)	PH12	8
8	PD13	(GPIO & MLB_ST)	PD13	K14	PD13	B1	PH13	(GPIO)	PH13	8
7	PD14	(MLB_DP)	PD14	K13	PD14	C1	PH14	(GPIO)	PH14	8
7	PD15	(MLB_SP / DAT)	PD15	J13	PD15	E3	PH15	(GPIO)	PH15	8
8	MCU-RSTx		MCU-RSTx	K1	RESET					
8	PORSTx		PORSTx	C8	PORST					
6	MCU-XTAL		MCU-XTAL	T7	XTAL					
6	MCU-EXTAL		MCU-EXTAL	T8	EXTAL					

PG0	(eMIOS E1UC_11_H)
PG1	(eMIOS E1UC_12_H)
PG2	(eMIOS E1UC_13_H)
PG3	(eMIOS E1UC_14_H)

Differences to 324BGA

(none on this page)

PPC5748GSK0MMJ6 + OTB-256(324R)-1.0-006-00

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GPIO 2 of 2

Key to text colours:
- Purple - Comms Physical Interfaces
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- RED - I/O Matrix and other functions (eg LED)
- Green - I/O Matrix (dedicated)

U1C

Calypso 256 BGA

Package 3of3 GPIO Pins2

8	PI0	(SD_D3)	PI0	C5	PI0
8	PI1	(SD_D2)	PI1	A4	PI1
8	PI2	(SD_D1)	PI2	D6	PI2
8	PI3	(SD_D0)	PI3	B5	PI3
8	PI4	(USB1_STP)	PI4	A12	PI4
8	PI5	(USB1_NXT)	PI5	D12	PI5
8	PI6	(USB0_RST)	PI6	D2	PI6
8	PI7	(USB1_RST)	PI7	E2	PI7
7	PI8	(MLB_CP / CLK)	PI8	J14	PI8
8	PI9	(GPIO)	PI9	J15	PI9
8	PI10	(GPIO)	PI10	J16	PI10
8	PI11	(ENET_RST)	PI11	H16	PI11
8	PI12	(GPIO & MLB_PS0)	PI12	G15	PI12
8	PI13	(GPIO & MLB_PS1)	PI13	G14	PI13
8	PI14	(SAI2_D0)	PI14	T12	PI14
8	PI15	(SAI2_MCLK)	PI15	P11	PI15
8	PJ0	(SAI2_SYNC)	PJ0	R11	PJ0
8	PJ1	(SAI2_BCLK)	PJ1	N10	PJ1
8	PJ2	(SAI1_D0)	PJ2	R10	PJ2
8	PJ3	(SAI1_BCLK)	PJ3	P10	PJ3
8	PJ4	(GPIO)	PJ4	D3	PJ4
8	PJ5	(GPIO)	PJ5	N12	PJ5
8	PJ6	(GPIO)	PJ6	N15	PJ6
8	PJ7	(GPIO)	PJ7	P16	PJ7
8	PJ8	(GPIO)	PJ8	P15	PJ8
8	PJ9	(GPIO)	PJ9	P5	PJ9
8	PJ10	(GPIO)	PJ10	T5	PJ10
8	PJ11	(GPIO)	PJ11	R3	PJ11
8	PJ12	(GPIO)	PJ12	T1	PJ12
8	PJ13	(GPIO)	PJ13	N5	PJ13
8	PJ14	(GPIO)	PJ14	T4	PJ14
8	PJ15	(GPIO)	PJ15	R4	PJ15
8	PK0	(GPIO)	PK0	T3	PK0
8	PK1	(GPIO)	PK1	H4	PK1
8	PK2	(GPIO)	PK2	L4	PK2
8	PK3	(GPIO)	PK3	N1	PK3
8	PK4	(GPIO)	PK4	M3	PK4
8	PK5	(GPIO)	PK5	M5	PK5
8	PK6	(GPIO)	PK6	M6	PK6
8	PK7	(GPIO)	PK7	M7	PK7
8	PK8	(GPIO)	PK8	M8	PK8
8	PK9	(GPIO)	PK9	E8	PK9
8	PK10	(GPIO)	PK10	E7	PK10
8	PK11	(GPIO)	PK11	F8	PK11
8	PK12	(GPIO)	PK12	G12	PK12
8	PK13	(GPIO)	PK13	H12	PK13
8	PK14	(GPIO)	PK14	J12	PK14
8	PK15	(GPIO)	PK15	D5	PK15
8	PL0	(GPIO)	PL0	C4	PL0
8	PL1	(GPIO)	PL1	F7	PL1
8	PQ0	(USB0_STP)	PQ0	J5	PQ0
8	PQ1	(USB0_CLK)	PQ1	H5	PQ1
8	PQ2	(USB0_DIR)	PQ2	G5	PQ2
8	PQ3	(USB0_NXT)	PQ3	F5	PQ3
8	PQ4	(USB0_D7)	PQ4	F6	PQ4
8	PQ5	(USB0_D6)	PQ5	E9	PQ5
8	PQ6	(USB0_D5)	PQ6	F10	PQ6
8	PQ7	(USB0_D4)	PQ7	E10	PQ7

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PM3	K12	PM3	(GPIO)	PM3	8	
PM4	L12	PM4	(GPIO)	PM4	8	
PM5	F9	PM5	(GPIO)	PM5	8	
			(GPIO)			
PM14	M12	PM14	(GPIO)	PM14	8	
PO0	K5	PO0	(GPIO)	PO0	8	
PO1	L5	PO1	(GPIO)	PO1	8	
PP12	E12	PP12	(USB0_D3)	PP12	8	
PP13	F12	PP13	(USB0_D2)	PP13	8	
PP14	E11	PP14	(USB0_D1)	PP14	8	
PP15	F11	PP15	(USB0_D0)	PP15	8	

Differences to 324BGA

- 14 fewer pins on Port L
- 12 fewer pins on Port M
- 16 fewer pins on Port N
- 14 fewer pins on Port O
- 12 fewer pins on Port P

(And corresponding changes to daughtercard connectors)

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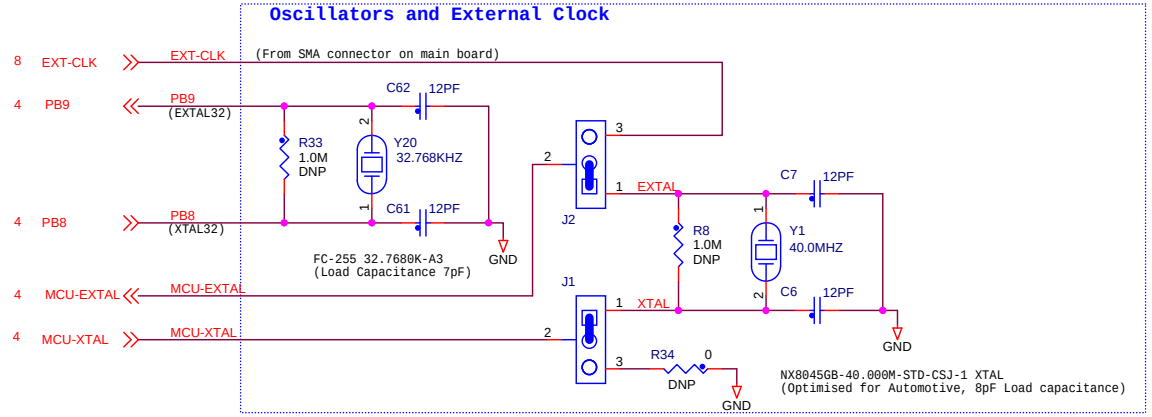

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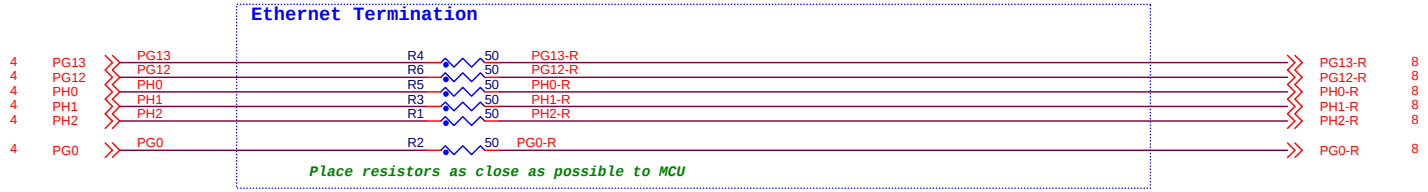
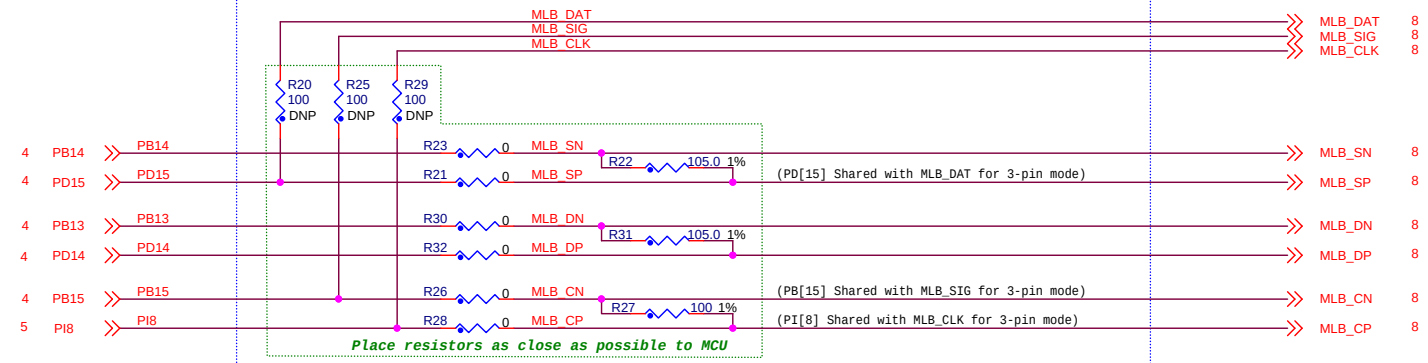
eed Signal Termination

Ethernet Termination



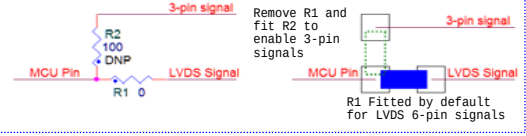
MLB Termination



From MCU

To Daughtercard

Layout Note - Place resistors as shown with shared pad (as close to MCU as possible)



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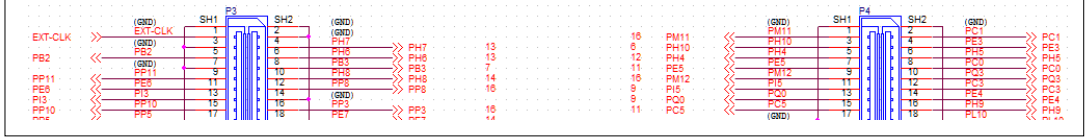
rd Connectors (Plugs)

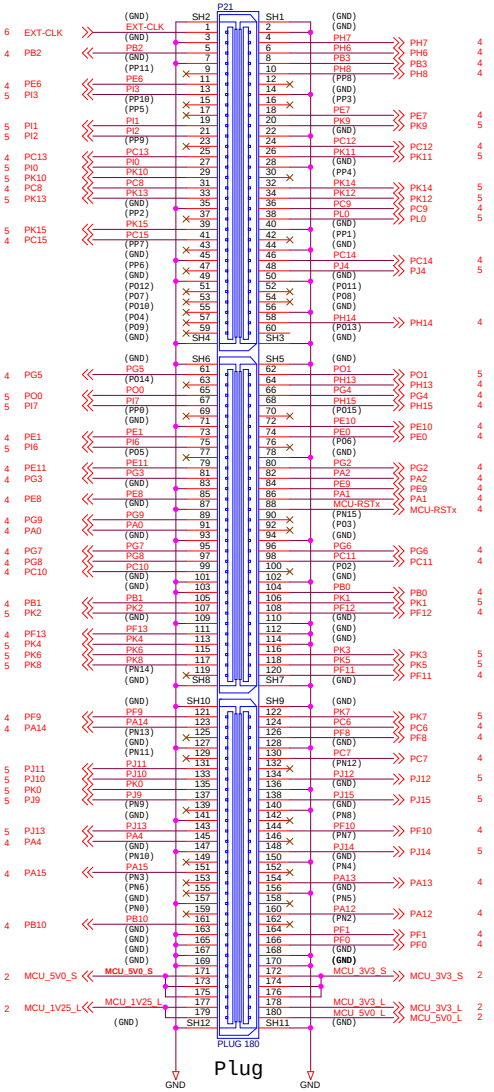
t way to fit these connectors onto a B sized sheet so unfortunately the sheet size has been increased to C so will need to be printed on larger paper.

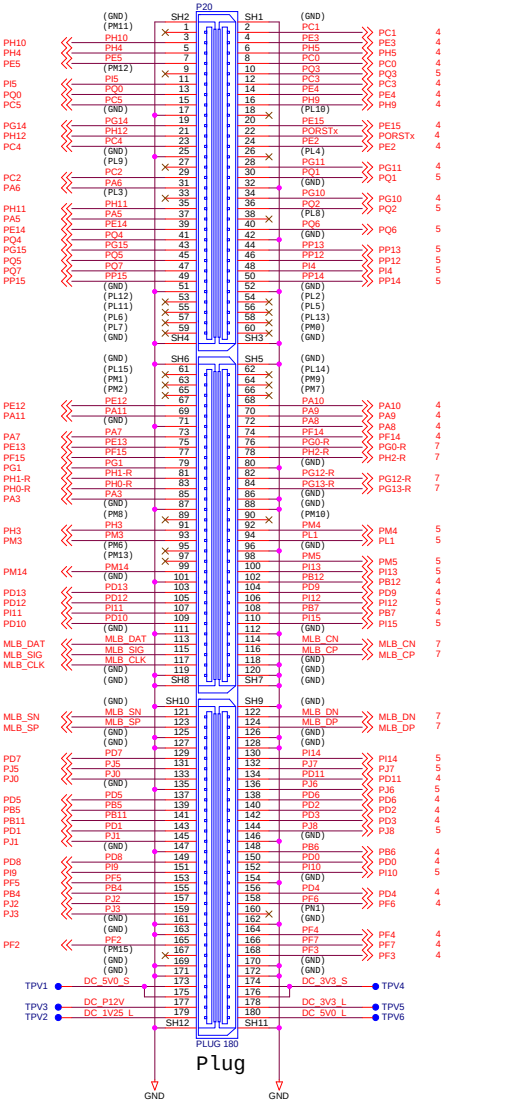
- The Crystal Signals are NOT routed via the daughtercard connectors
- The Specific MCU power pins are not routed via the daughter card however the jumpered MCU supply lines are brought up from the main board (see the top pins of the connector on the left)

- The connector schematic symbols have been horizontally mirrored so they match the main EVB connector. This has no bearing on the PCB placement or footprint. Pin1 on the recepticle mates with pin 1 on the plug.

Connectors on Main board (Shown for reference)







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