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REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	X1	- First Draft - The schematic was changed from SCH-20385_C. - The flash memories U7 & U9 were changed from Spansion, AM29BDS128HE9VK1 to S29WS128N0PBF. - NAND flash card connector P21 was replaced by two RoHS compliant connectors (PM1 & PM2)	05-Oct-05	
	X2	- 2nd Draft - Removed the JS6 & JS7 for QVDD and QVDDX	16-Dec-05	
	X3	Page 3 : Re-design the power supplies for 2.5V, 1.8V & 1.5V.	02-Mar-06	
	X4	Page 4 : Removed the QVDDX and connect them to QVDD.	09-Mar-06	
	X5	Page 3 : Removed the 5V option from 1.8V, 1.5V & 2.5V regulators. Set VCC as the power source for 2.5V regulator. Changed C110 from 4.7uF to 1uF for generating a min. 800ms reset pulse.	12-Mar-06	
	X6	Page 3 : Changed R29 from 2.00K to 1.96K (0.1%).	22-Mar-06	
	A	Release to production	26-July-06	

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Designed by: Eddie Lee	Date: 05-OCT-05
Drawn by: Eddie Lee	Date: 05-OCT-05
Project lead:	Date:
Product Specialist: Lee Kin Heng	Date: 05-OCT-05



Title: M9328MX21ADS CPU Board - ECO Compliant			
Size C	Root: Name: <Name6>	Document Number SCH-75830	Rev A
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- NOTES:
- 1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE IN OHMS, 5%, 1/8 WATT.
ALL CAPACITORS ARE IN UF.
ALL VOLTAGE ARE DC.
 - 2. INTERRUPTED LINES CODES WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
 - 3. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
 - 4. SPECIAL SYMBOL USAGE:
_B DENOTES - ACTIVE LOW SIGNAL.
<> DENOTES - VECTORED SIGNALS.
 - 5. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION, WITH THE EXCEPTION OF LOGIC BLOCK SYMBOLOGY.
 - 6. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:

SHEET

5

C7

<

>

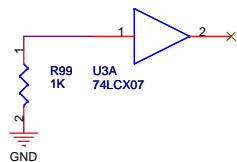
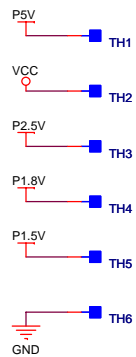
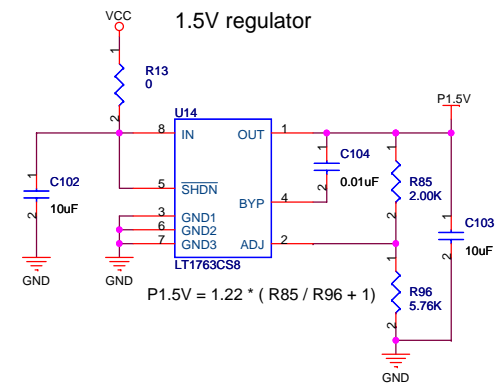
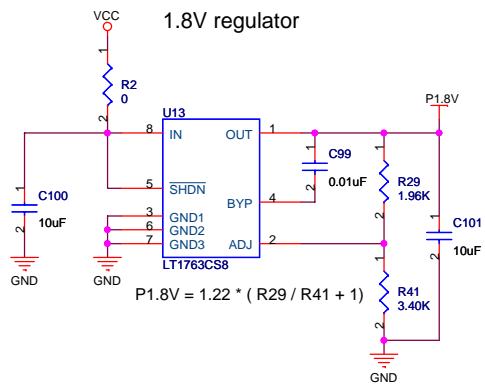
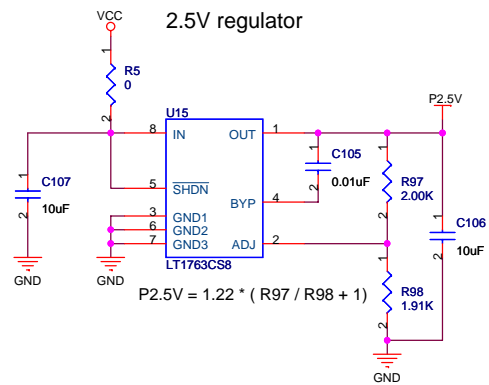
OUTPUT

ZONE

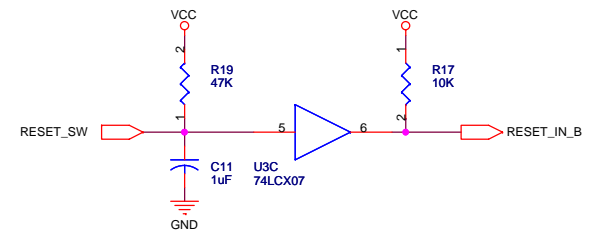
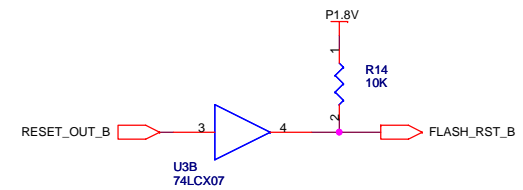
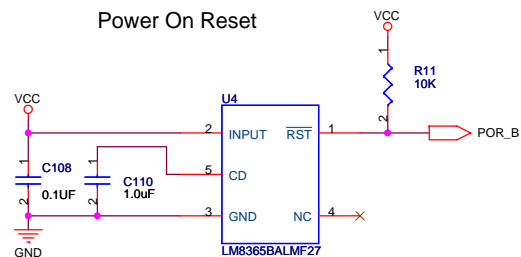
INPUT
 - 7. VCC LOCATIONS
UNLESS OTHERWISE SPECIFIED, VCC IS APPLIED TO:
PIN8 OF ALL 8-PIN ICS
PIN14 OF ALL 14-PIN ICS
PIN16 OF ALL 16-PIN ICS
PIN20 OF ALL 20-PIN ICS
 - 8. GROUND LOCATIONS
PIN4 OF ALL 8-PIN ICS
PIN7 OF ALL 14-PIN ICS
PIN8 OF ALL 16-PIN ICS
PIN10 OF ALL 20-PIN ICS

Notes

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B	Name: <Name6>	SCH-75830	A
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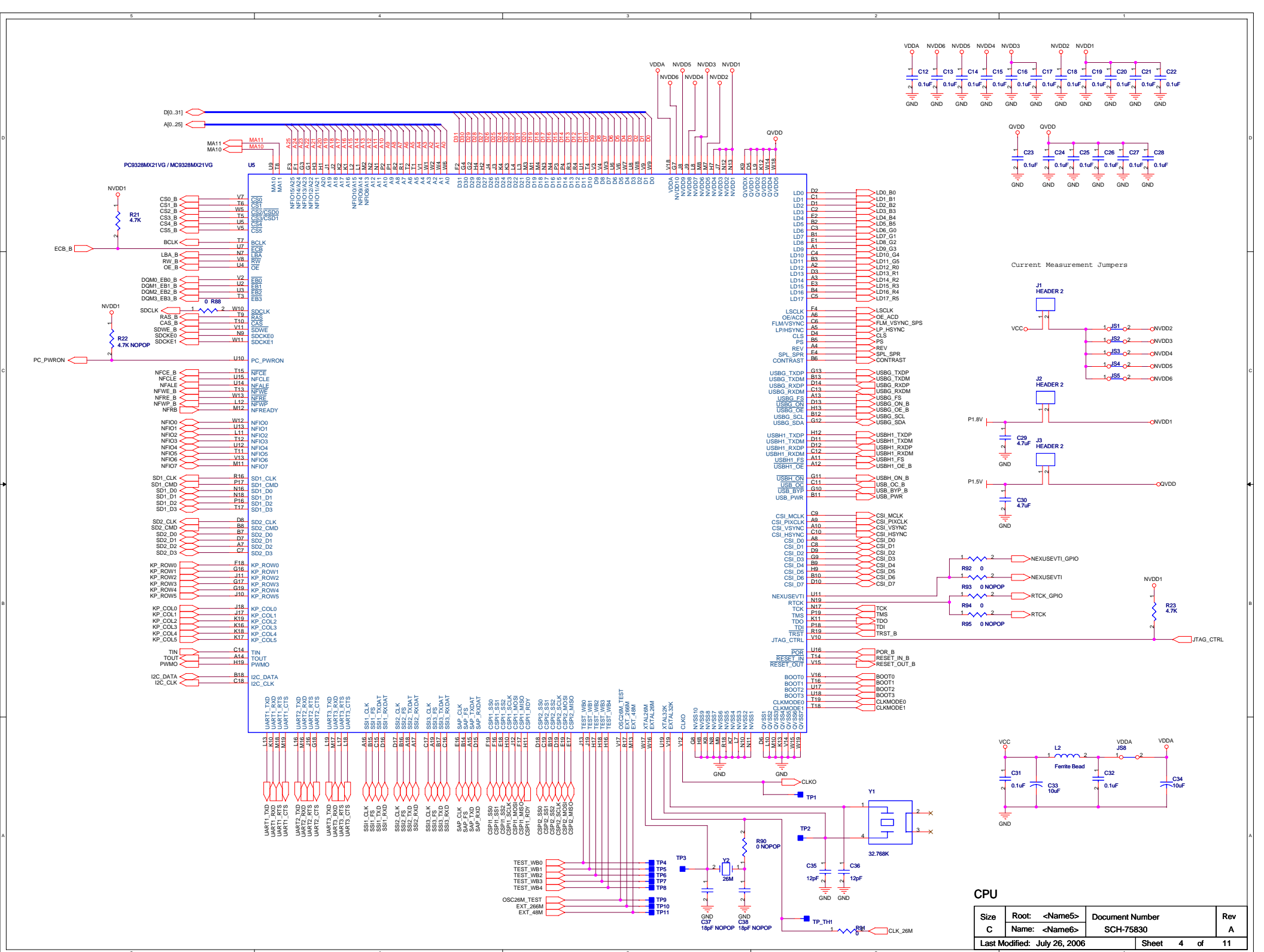


Power On Reset



Regulators

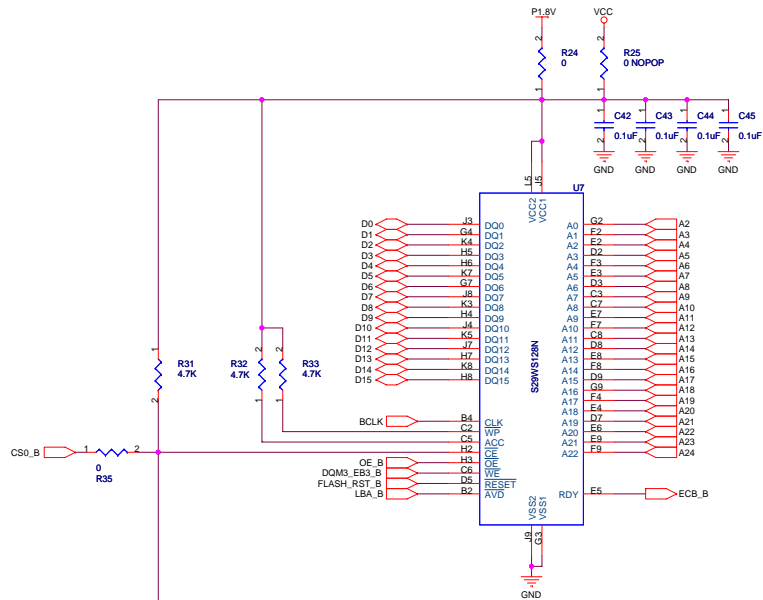
Size B	Root: <Name5>	Document Number SCH-75830	Rev A
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CPU			
Size	Root: <Name>	Document Number	Rev
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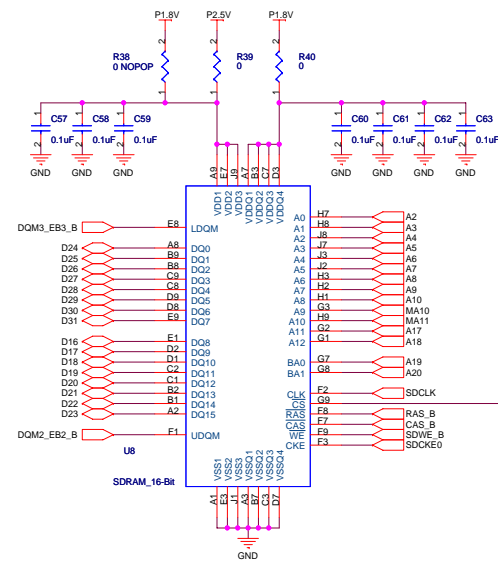
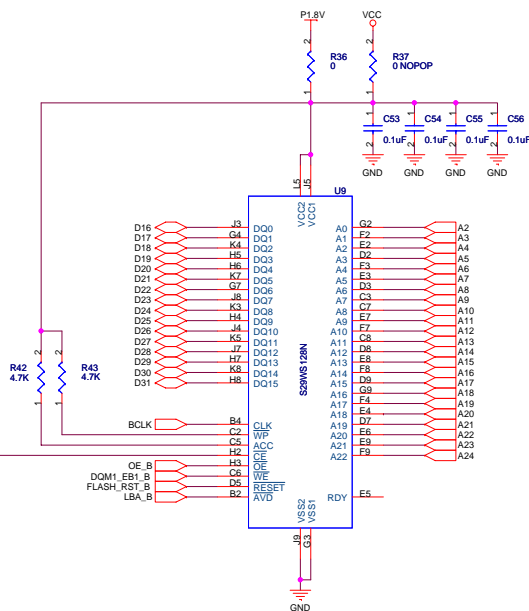
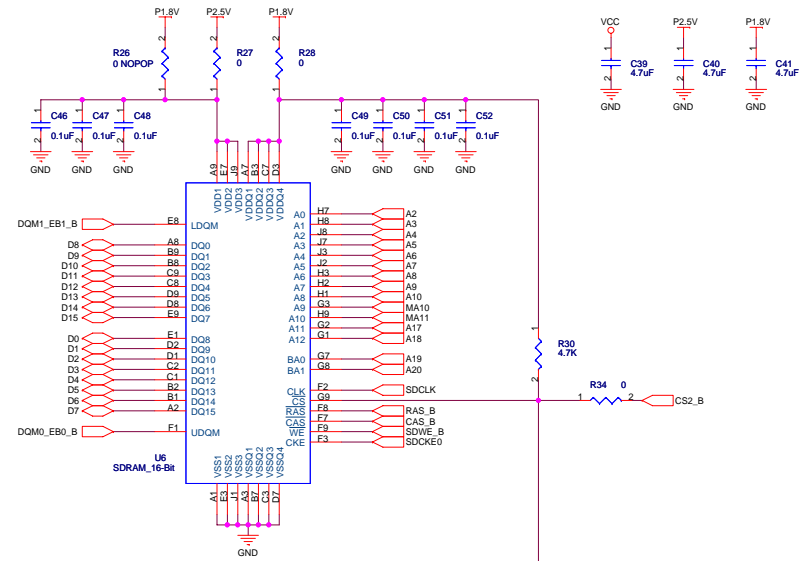
FLASH (32MB)

Address : 0xC000 0000 - 0xC9FF FFFF



SDRAM (64MB)

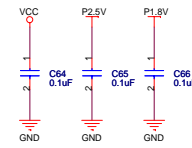
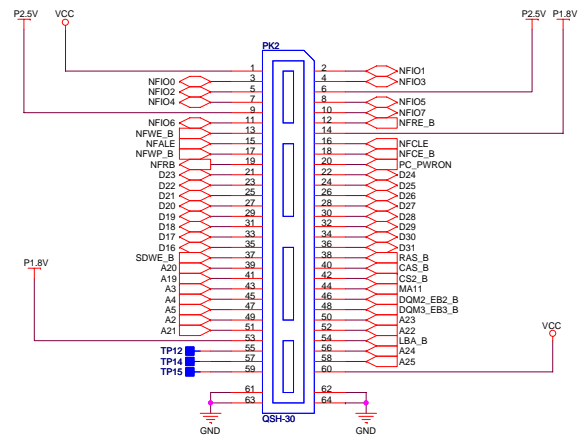
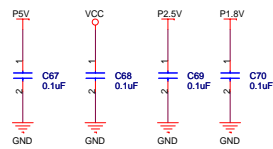
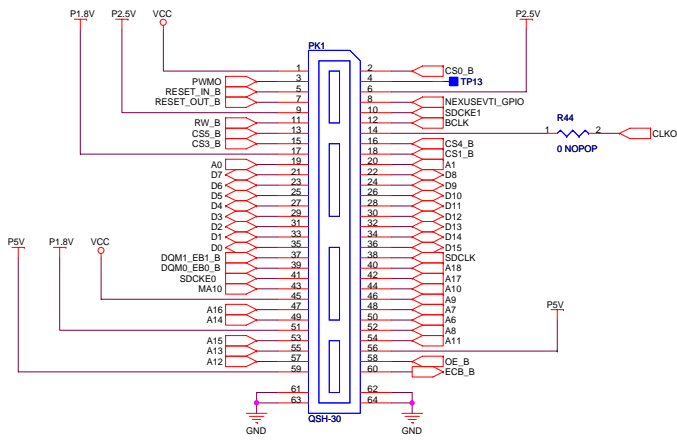
Address : 0xC000 0000 - 0xC9FF FFFF



In order to minimize the trace length on the PCB layout, the data bus & DQM signals in SDRAM were re-arranged as shown above.

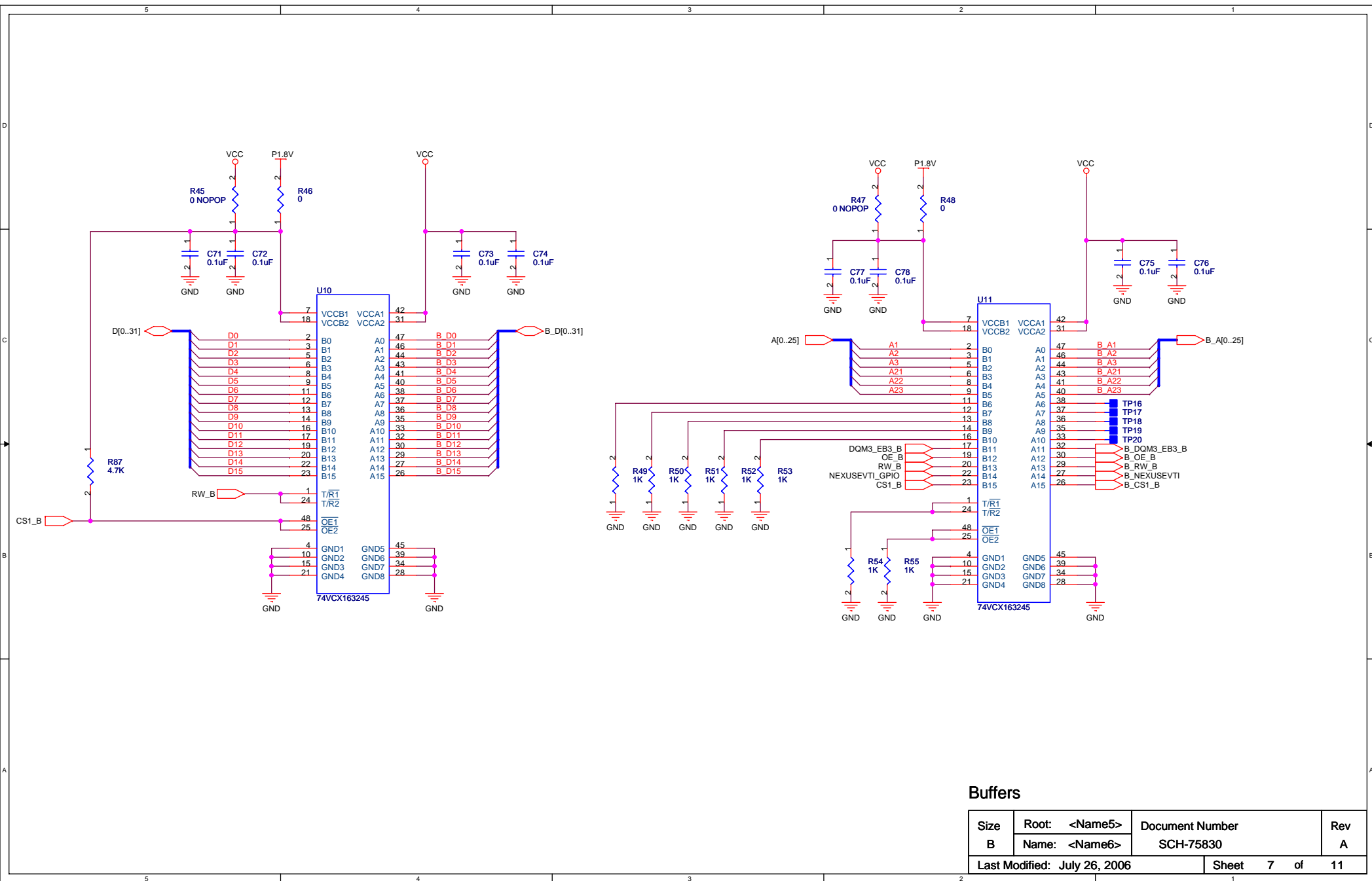
Memories

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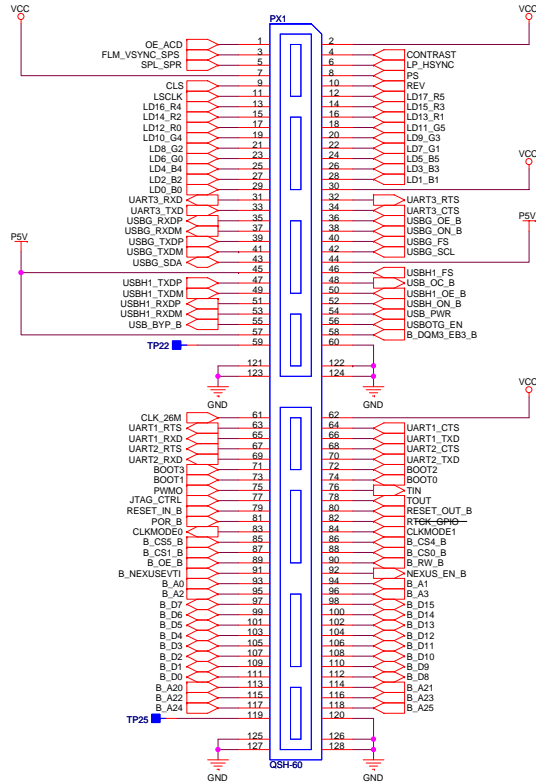
High Speed Connectors

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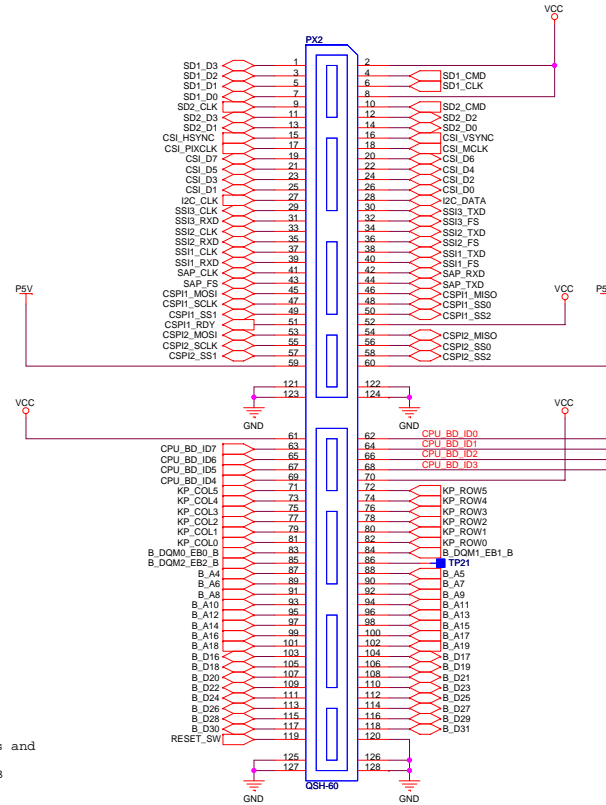


Buffers

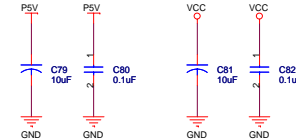
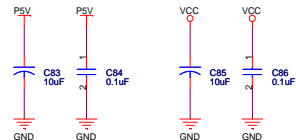
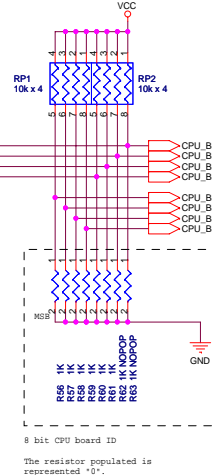
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Un-used address and data pins are reserved by EVB



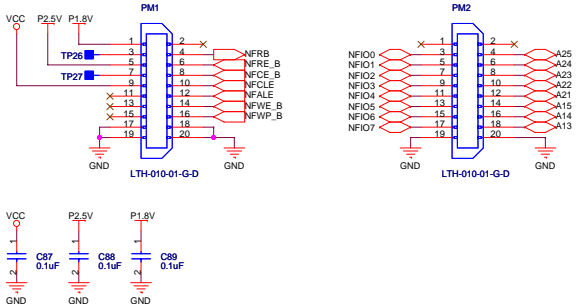
Un-used data pins are reserved by EVB



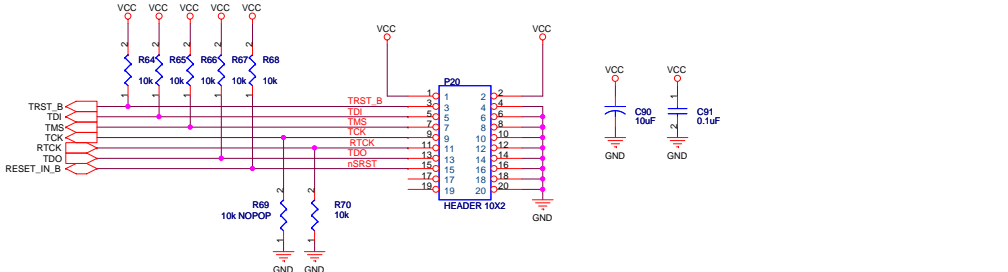
Connectors to Base Board

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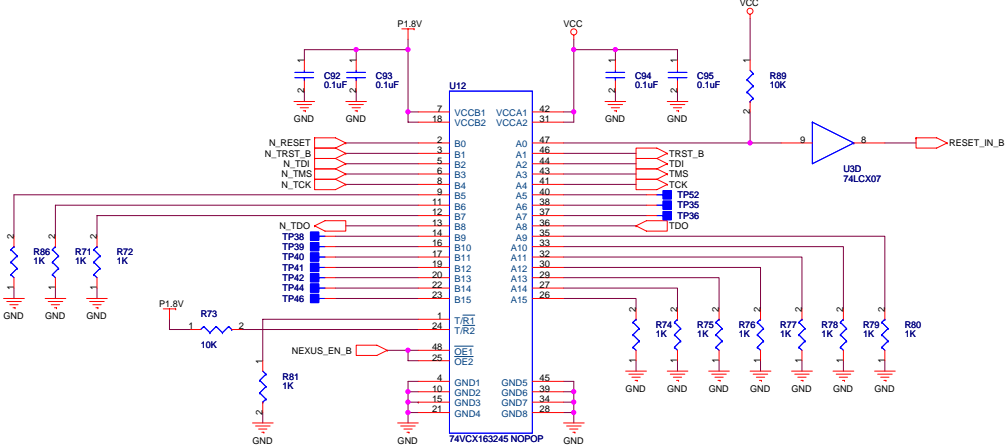
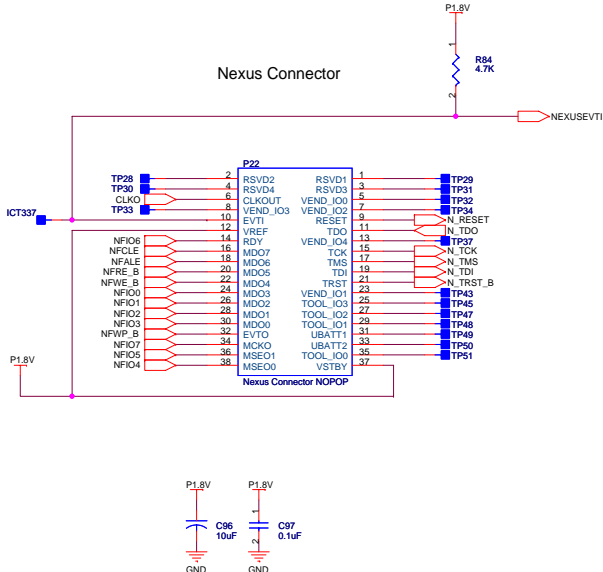
NAND Flash Connectors



Multi-ICE Interface Connector

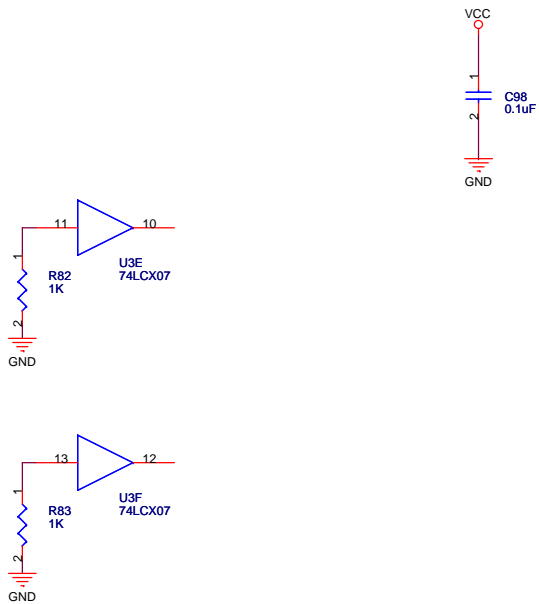


Nexus Connector



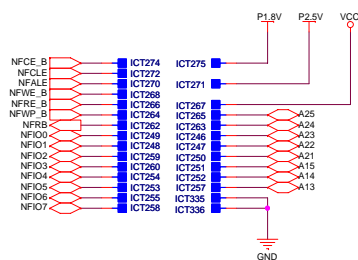
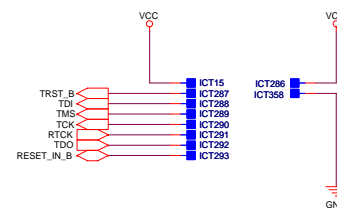
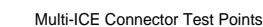
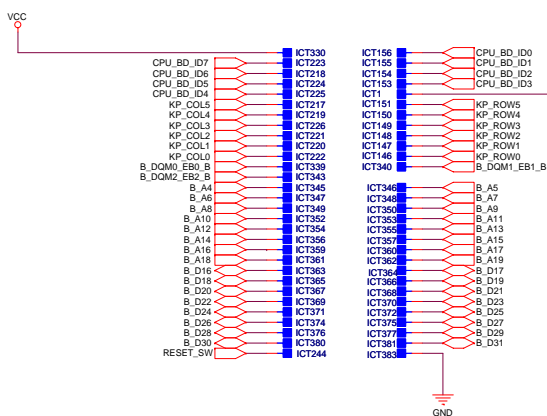
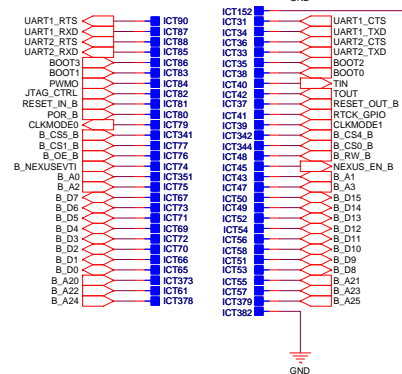
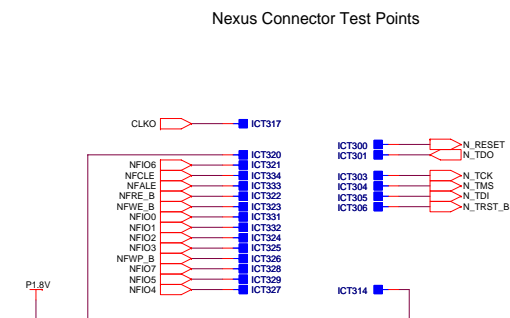
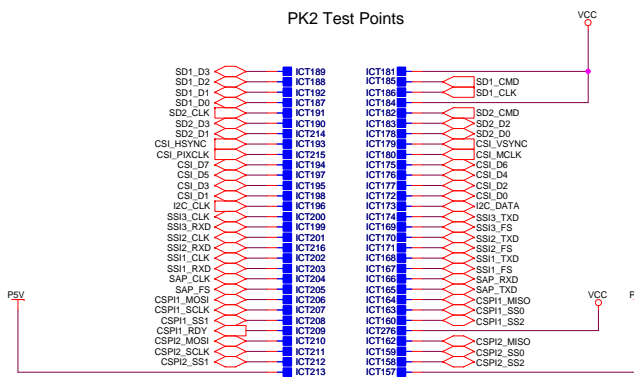
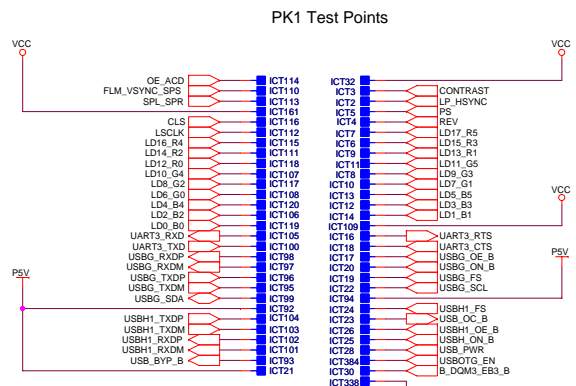
Debug Ports & NAND Flash Connector

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Unused Gates

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ICT

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