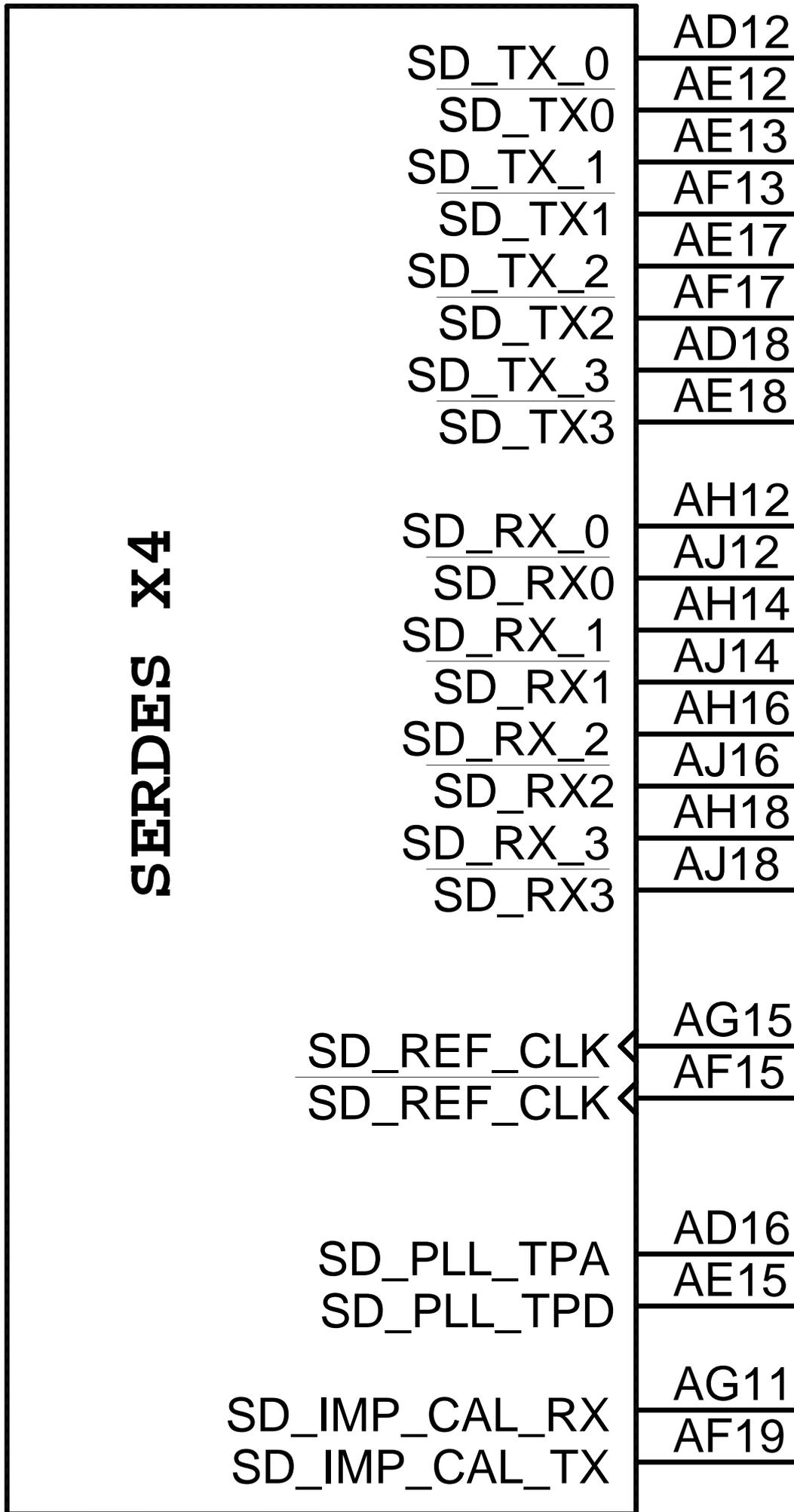
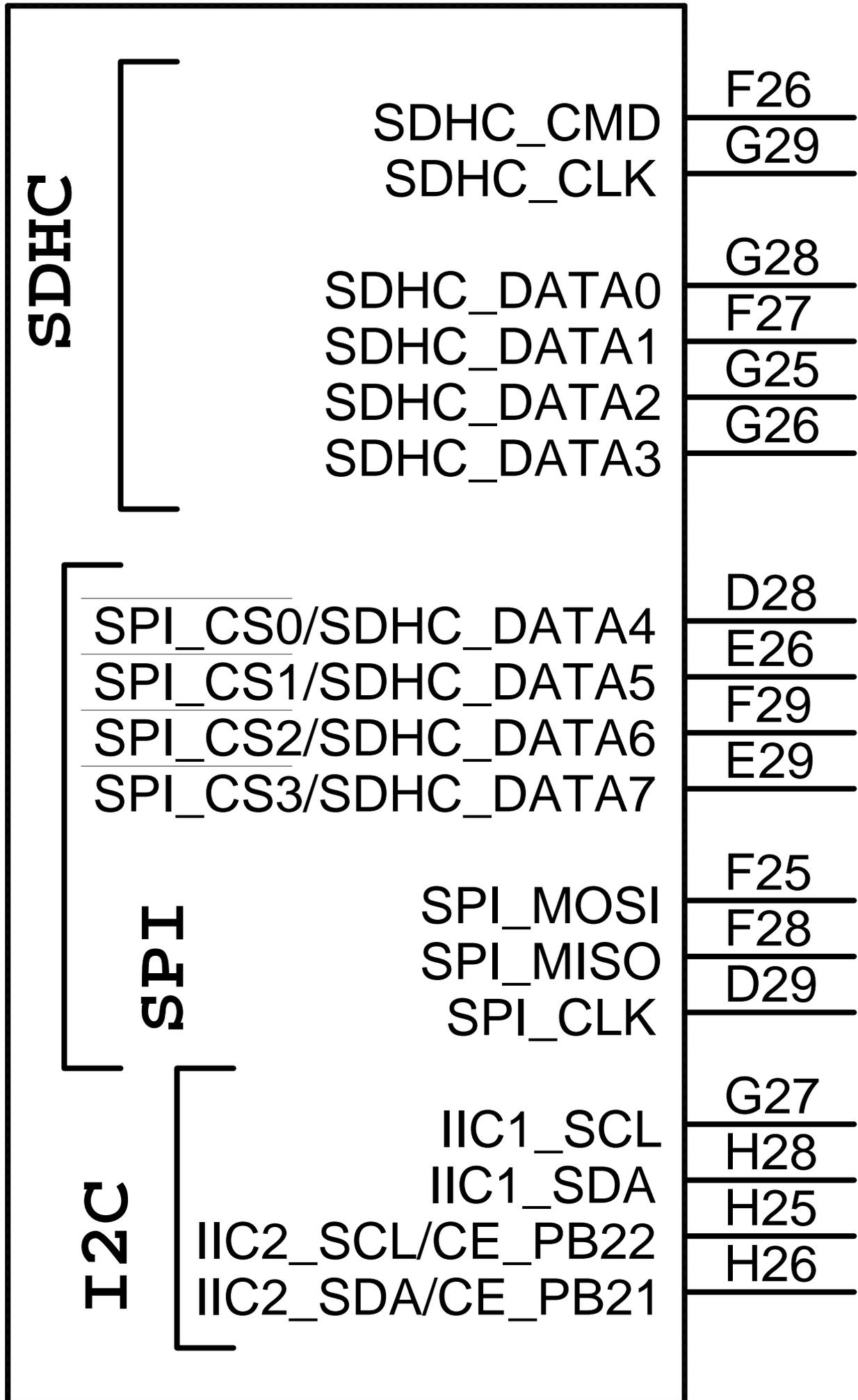


AC5	NC75	MDQ00	AJ8
AC6	NC73	MDQ01	AH8
F5	NC74	MDQ02	AH5
F6	NC76	MDQ03	AJ4
A10	NC53	MDQ04	AJ9
B9	NC52	MDQ05	AH9
B6	NC51	MDQ06	AH6
A5	NC50	MDQ07	AJ5
A11	NC49	MDQ07	AJ6
B10	NC48	MDQS00	AJ7
B7	NC47	MDQS00	AH7
A6	NC46		
D8	NC45	MDQ08	AF8
E8	NC44	MDQ09	AE8
E5	NC43	MDQ10	AF5
C4	NC42	MDQ11	AG4
E9	NC41	MDQ12	AG9
D9	NC40	MDQ13	AF9
E6	NC39	MDQ14	AE6
C5	NC38	MDQ15	AE5
A3	NC37	MDQS01	AF6
B3	NC36	MDQS01	AF7
D2	NC35	MDM01	AE7
D1	NC34		
A4	NC33	MDQ16	AH3
B4	NC32	MDQ17	AH2
C3	NC31	MDQ18	AE1
C1	NC30	MDQ19	AE2
E1	NC29	MDQ20	AH4
F2	NC28	MDQ21	AJ3
H4	NC27	MDQ22	AF2
H5	NC26	MDQ23	AF1
E4	NC25	MDQS02	AG2
E2	NC24	MDQS02	AG1
G3	NC23	MDM02	AH1
G4	NC22		
F3	NC61	MDQ24	AD4
F4	NC65	MDQ25	AC4
B2	NC62	MDQ26	Y5
B1	NC66	MDQ27	W5
D7	NC63	MDQ28	AF3
D6	NC67	MDQ29	AE4
A9	NC64	MDQ30	AB5
A8	NC68	MDQ31	Y4
G1	NC57	MDQS3	AB3
C2	NC58	MDQS03	AB4
F8	NC59	MDM03	AC1
A7	NC60		
J1	NC69	MECC00	AD2
G2	NC70	MECC01	AC2
U6	NC71	MECC02	W1
V2	NC72	MECC03	V3
J4	NC77	MECC04	AB2
F1	NC78	MECC05	AD1
AE10	NC5	MECC06	Y1
AF10	NC6	MECC07	V6
E13	NC10	MDQS08	AA1
E14	NC9	MDQS08	AB1
W6	NC15	MDM08	AA4
Y14	NC2		
Y15	NC3	MA00	L6
Y16	NC4	MA01	M2
AF26	NC83	MA02	M1
AE26	NC82	MA03	M5
AA25	NC85	MA04	N1
AG29	NC84	MA05	P1
AA26	NC87	MA06	N4
AA24	NC88	MA07	P3
AG28	NC89	MA08	P2
AD27	NC90	MA09	R1
AB26	NC91	MA10	K6
AC26	NC92	MA11	R4
AD26	NC93	MA12	T5
AB27	NC94	MA13	J5
AD28	NC95	MA14	T3
AF29	NC96	MA15	U4
AF28	NC97		
AD29	NC98	MBA00	K5
AE28	NC99	MBA01	L5
AC29	NC100	MBA02	T4
Y24	NC86		
		MCS00	J2
		MCS01	J6
		MCKE00	U5
		MCKE01	V1
		MODT00	H1
		MODT01	H6
		MWE	K2
		MRAS	K1
		MCAS	J3
		MCK00	U2
		MCK00	U1
		MCK01	AD8
		MCK01	AD7
		MCK02	D4
		MCK02	D5
		MCK03	T2
		MCK03	T1
		MDIC00	C10
		MDIC01	F10
		MAPAR_OUT	R5
		MAPAR_ERR	N5
		MVREF	R6

LOCAL BUS/QE	
LAD00	B18
LAD01	E20
LAD02	A19
LAD03	B20
LAD04	D19
LAD05	A18
LAD06	B17
LAD07	C20
LAD08/CE_PA0	F19
LAD09	E10
LAD10	B16
LAD11	D14
LAD12	D17
LAD13	E11
LAD14	A16
LAD15	C15
CFG_CPU1_BOOT/CE_PA4/LA16	B21
LA17/CE_PA5	A22
CFG_HOST_AGT1/CE_PA6/LA18	C21
CFG_HOST_AGT2/CE_PA7/LA19	F21
LA20/CE_PA8	E12
LA21/CE_PA9	A21
LA22/CE_PA10	D11
CFG_PLAT_SPEED/CE_PA17/LA23	E22
CFG_CORE0_SPEED/CE_PA18/LA24	F20
CFG_CORE1_SPEED/CE_PA19/LA25	E21
CFG_DDR_SPEED/CE_PA20/LA26	B22
CFG_CPU0_BOOT/CE_PA21/LA27	F18
CFG_SYS_SPEED/CE_PA13/LA28	A23
CFG_SYS_PLL0/CE_PA25/LA29	B23
CFG_SYS_PLL1/CE_PA26/LA30	C23
CFG_SYS_PLL2/CE_PA30/LA31	D23
LCS00	D20
LCS01	A12
LCS02	E19
LCS03	D21
LCS04/CE_PA22	F11
LCS05/CE_PA23	D15
LCS06/CE_PA24	D13
LCS07/CE_PA27	A17
CFG_CORE1_PLL0/LWE0	F12
CFG_HOST_AGT0/CE_PB9/LWE1	D12
LBCTL/CE_PB20	E17
CFG_CORE0_PLL1/LALE	C17
LGPL0/CE_PA1	B12
LGPL1/CE_PA2	C13
CFG_CORE0_PLL2/LGPL2	A20
CFG_BOOT_SEQ0/CE_PA3/LGPL3	D10
LGPL4	B13
CFG_BOOT_SEQ1/CE_PA14/LGPL5	C19
LDP00/CE_PA11	E18
LDP01/CE_PA12	B19
LCLK00/CE_PA28	B15
LCLK01/CE_PA16	A15
CE_PB2	A13
CE_PB3	A14



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	CFG_TSEC1_PRTCL0/TSEC1_TXD0	AD24
	CFG_IO_PORTS2/TSEC1_TXD1	AE25
	CFG_IO_PORTS1/TSEC1_TXD2	AH28
	CFG_IO_PORTS0/TSEC1_TXD3	AJ25
	TSEC1_TX_EN	AH24
	CFG_ROM_LOC3/TSEC1_TX_ER	AF23
	TSEC1_TX_CLK/TSEC1_GTX_CLK125<	AJ24
	TSEC1_GTX_CLK	AG25
		AH25
eTSEC1	TSEC1_RXD0	AD21
	TSEC1_RXD1	AE22
	TSEC1_RXD02	AJ28
	TSEC1_RXD3	AJ26
	TSEC1_RX_DV	AH23
	TSEC1_RX_ER	AG26
	TSEC1_RX_CLK<	
		AE21
	CFG_ROM_LOC2/TSEC3_TXD0	AD23
	CFG_ROM_LOC1/TSEC3_TXD1	AD22
	CFG_ROM_LOC0/TSEC3_TXD2	AF22
	CFG_TSEC1_PRTCL1/TSEC3_TXD3	AB24
	TSEC3_TX_EN	AE27
	TSEC3_TX_CLK<	AB25
	TSEC3_GTX_CLK	
		AE24
eTSEC3	TSEC1_RXD04/TSEC3_RXD00	AJ23
	TSEC1_RXD05/TSEC3_RXD01	AH22
	TSEC1_RXD06/TSEC3_RXD02	AG23
	TSEC1_RXD07/TSEC3_RXD03	AJ27
	TSEC1_CRS/TSEC3_RX_DV	AD25
	TSEC3_RX_ER	AH26
	TSEC1_COL/TSEC3_RX_CLK<	AF24
	(TSEC3) EC_GTX_CLK125<	
		AD20
	CFG_TSEC_REDUCE/EC_MDC	AJ21
	MANAGEMENT EC_MDIO	
		AE20
	CFG_SRDS_REFCLK/TSEC1588_ALARMOUT1	AJ20
	CFG_SGMII3/TSEC1588_ALARMOUT2	
		AH21
	CFG_DDR_PLL1/TSEC1588_PULSEOUT1	AJ22
	CFG_DDR_PLL2/TSEC1588_PULSEOUT2	
		AG22
	CFG_DDR_PLL0/TSEC1588_CLK_OUT	
		AH20
IEEE1588	TSEC1588_TRIGIN1	AG20
	TSEC1588_TRIGIN2	
		AG21
	TSEC1588_CLK_IN<	

U?F

USB	USB_D00	C26
	USB_D01	A26
	USB_D02	A27
	USB_D03	D26
	USB_D04	B25
	USB_D05	B28
	USB_D06	C25
	USB_D07	C28
	USB_DIR	A28
	USB_STP	B29
	USB_NXT	B26
	USB_CLK	D27
	USB_PWRFAULT	C29
	DUART	UART_SIN0
UART_SOUT0		J26
UART_CTS0		J28
CFG_TSEC3_PRTCL0/UART_RTS0		J29
UART_SIN01/CE_PB16		G24
CFG_CORE1_PLL1/CE_PB17/UART_SOUT1		J25
UART_CTS01/CE_PB14		H24
CFG_TSEC3_PRTCL1/CE_PB15/UART_RTS1	J24	

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SYSTEM CONTROL & I/Os

	W27
SCAN_MODE	AA28
TEST_SEL	
	E16
NC20	E15
NC21	
	AB28
TRIG_IN	U28
TRIG_OUT	
	P28
MSRCID00/LB_MSRCID00/PLL_PER_OUT0/CE_PB23	R27
MSRCID01/LB_MSRCID01/PLL_PER_OUT1/CE_PB24	P27
MSRCID02/LB_MSRCID02/PLL_PER_OUT2/CE_PB25	P26
MSRCID03/LB_MSRCID03/PLL_PER_OUT3/CE_PB26	N26
MSRCID04/LB_MSRCID04/PLL_UP_DN/CE_PB27	M24
MDVAL/LB_MDVAL/PLL_PER_VALID/CE_PB28	
	Y28
DMA1_DREQ00	T28
DMA1_DACK00	T26
DMA1_DDONE00	W28
CE_PB18	T29
CFG_MEM_DEBUG/CE_PB19	Y29
CFG_DDR_DEBUG /CE_PA29	
	L24
IRQ00	K26
IRQ01	K29
IRQ02	N25
IRQ03	L26
IRQ04	L29
IRQ05	K27
CE_PB10	N29
IRQ_OUT	
	R28
CE_PB4	R26
CE_PB6	P29
CE_PB11	N24
CE_PB7	U29
CE_PB5	R24
CE_PB0	R29
CE_PA31	R25
CE_PB1	F22
SDHC_CD/CE_PB12	A24
SDHC_WP/CE_PB13	A25
USB_PCTL0/CE_PB8	D24
USB_PCTL1/CE_PA15	F23
CE_PB29	E23
CE_PB30	F24
CE_PB31	E24
CE_PC0	
	M28
LVDD_VSEL	M29
BVDD_VSELO	M27
BVDD_VSEL1	L28
CVDD_VSELO	L27
CVDD_VSEL1	
	AA27
MCP0	M25
MCP1	J27
UDE0	K28
UDE1	
	T25
TDI	V28
TDO	V29
TCK	U26
TMS	V26
TRST	
	AA29
CKSTP_IN0	AB29
CKSTP_IN1	V25
CKSTP_OUT0	Y27
CKSTP_OUT1	
	W25
HRESET	U24
HRESET_REQ	W24
SRESET	
	W29
SYSCLK	AC9
DDRCLK	K24
RTC	
	T24
CLK_OUT	U25
ASLEEP	W26
CFG_CORE1_PLL2/READY_P1	AF27
CFG_DRAM_TYPE	AE29
CFG_IO_PORTS3	



U?H				
K15	VDD6	VDDC (CORE1)	F15	
K16	VDD7		AVDD_CORE1	F16
K17	VDD8		AVDD_CORE0	V24
K18	VDD9		AVDD_PLAT	Y10
K19	VDD10		AVDD_LBIU	AD14
K20	VDD11		AVDD_DDR	F14
L20	VDD13		AVDD_SRDS	
M20	VDD15		NC102	
N10	VDD16			AG16
N20	VDD17		SVDD1	AH13
P10	VDD18		SVDD2	AH17
P20	VDD19		SVDD3	AJ11
R10	VDD20		SVDD4	AJ15
R20	VDD21		SVDD5	AJ19
T10	VDD22		SVDD6	
T20	VDD23			AD13
U10	VDD24		XVDD1	AD17
U20	VDD25		XVDD2	AE11
V10	VDD26		XVDD3	AE19
V20	VDD27		XVDD4	AF14
W10	VDD28		XVDD5	AF16
W20	VDD29		XVDD6	
Y11	VDD30			A2
Y12	VDD31		GVDD1	B8
Y18	VDD32		GVDD2	B11
Y19	VDD33		GVDD3	C7
Y20	VDD34		GVDD4	C9
			GVDD5	D3
			GVDD6	E7
			GVDD7	F9
K14	VDD5		GVDD8	G10
K13	VDD4		GVDD9	H2
K10	VDD1		GVDD10	K3
K11	VDD2		GVDD11	K7
K12	VDD3	GVDD12	L2	
L10	VDD12	GVDD13	L3	
M10	VDD14	GVDD14	L4	
		GVDD15	N3	
		GVDD16	N6	
F13	NC103	GVDD17	P4	
G6	NC1	GVDD18	R2	
		GVDD19	U3	
K23	OVDD1	GVDD20	V5	
L25	OVDD2	GVDD21	W3	
N27	OVDD3	GVDD22	Y2	
P25	OVDD4	GVDD23	AA2	
U27	OVDD5	GVDD24	AA3	
Y26	OVDD6	GVDD25	AA5	
		GVDD26	AA7	
B24	BVDD1	GVDD27	AB6	
C12	BVDD2	GVDD28	AD5	
C14	BVDD3	GVDD29	AD9	
C16	BVDD4	GVDD30	AE3	
C22	BVDD5	GVDD31	AF4	
D18	BVDD6	GVDD32	AG6	
G20	BVDD7	GVDD33	AG8	
		GVDD34	AJ2	
Y23	LVDD1	GVDD35		
AC21	LVDD2		C27	
AC25	LVDD3	CVDD1	E25	
AC27	LVDD4	CVDD2	E27	
AE23	LVDD5	CVDD3		
AF21	LVDD6		AH10	
AF25	LVDD7	FA_VDD/GND		
AH27	LVDD8		AD10	
AH29	LVDD9	FA_ANALOG_G_V/GND		
		FA_ANALOG_PIN/GND	AJ10	

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