Freescale Semiconductor’s MET LDMOS Model

1. Description of the Model

The MET LDMOS model [1] is an electro thermal model that can account for dynamic self-heating effects and was specifically tailored to model RF high power LDMOS transistors and RF ICs used in base station, digital broadcast, land mobile and subscriber applications. It has been implemented in both the Agilent EEs of ADS and AWR Corporation Microwave Office® harmonic balance simulators and is capable of performing small-signal, large-signal, harmonic-balance, noise and transient simulations.

The MET model is an empirical large signal nonlinear model, which is single-piece and continuously differentiable and includes static and dynamic thermal dependencies. This model is capable of accurately representing the current-voltage characteristics and their derivatives at any bias point and operating temperature. A single continuously differentiable drain current equation models the subthreshold, triode, high current saturation and drain to source breakdown regions of operation. A set of static thermal equations governing the electro-thermal behavior of the drain to source nonlinear current model parameters were developed by measuring the nonlinear drain current under pulsed voltage conditions at different operating temperatures, ensuring an isothermal measurement environment.

Pulsed S-parameters were used to develop equations to model the capacitance functions of voltage and temperature, which were described by functions that have no poles and facilitate robust numerical stability. The nonlinear capacitances were extracted with a small signal model that represents the small signal limit of the device nonlinear behavior at any given bias point. Using a thermal analogue circuit, as in many previous circuit models, the MET LDMOS model accommodates thermal effects. The self-consistent temperature determined by this circuit sets the values of current control parameters, capacitance values and source, drain and gate resistances.

2. Equivalent Circuit

The large signal equivalent circuit of the MET LDMOS model is shown in Figure 1. The model has one voltage and temperature dependent nonlinear current source, \( I_{ds} \), as well as a forward diode and a reverse diode. The forward diode is a function of voltage while the reverse diode is temperature and voltage dependent. The reverse diode has a temperature dependent series resistance associated with it. The model also has three voltage and temperature dependent nonlinear charges, \( Q_{gs}, Q_{gd}, \) and \( Q_{ds} \). There are two internal gate conductances, \( G_{gs}, \) and \( G_{dg} \) as well as three temperature dependent parasitic resistances, \( R_g, R_d, \) and \( R_s \). The instantaneous temperature rise is calculated with the use of the thermal sub-circuit, where \( I_{therm} \) is the total instantaneous power dissipated in the transistor, \( R_{th} \) is the thermal resistance, \( C_{th} \) is the thermal capacitance, and \( V_{tsnk} \) is a voltage source that represents the heat sink temperature of the system. The isothermal small signal equivalent circuit model produced by linearizing the MET LDMOS model is shown in Figure 2.
Figure 1. Large Signal Equivalent Circuit of the MET LDMOS model.

\[
I_1 = V_{gs} \cdot G_{m1} \cdot \exp(-j\omega TAU)
\]

Reverse Bias (\(V_{ds} \leq 0, G_{m1} = 0\))

\[
I_2 = V_{gd} \cdot G_{m2} \cdot \exp(-j\omega TAU)
\]

Forward Bias (\(V_{ds} > 0, G_{m2} = 0\))

\[
I_{th} = f(V_{ds}, V_{gs}, V_{gd}, V_{rg}, V_{rd}, V_{rs}, V_{diode_r})
\]

Rs, Rd, Rg, Rdiode = f(T)

Figure 2. Isothermal Small Signal Equivalent Circuit of the MET LDMOS model.

\[
I_{diode_f} = f(V_{diode_r})
\]

\[
I_{diode_r} = f(V_{diode_r}, T)
\]

\[
Q_{ds} = f(V_{ds}, T)
\]

\[
Q_{gs} = f(V_{gs}, T)
\]

\[
Q_{gd} = f(V_{gd}, T)
\]

\[
Q_{rd} = f(V_{rd}, T)
\]

\[
Q_{rg} = f(V_{rg}, T)
\]

\[
Q_{g} = f(V_{gs}, V_{gd}, V_{rg}, V_{rd}, V_{rs}, V_{diode_r})
\]
3. Model Parameters

The following table contains all the MET LDMOS model parameter definitions and their units.

<table>
<thead>
<tr>
<th>PARAMETER NAME</th>
<th>PARAMETER DEFINITION</th>
<th>DEFAULT VALUE</th>
<th>UNITS</th>
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<td>RG_0</td>
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</table>

### 4. Scaling Rules

The model parameters are scaled by two different parameters, AREA, which is the ratio of the desired gate periphery to the gate periphery of the transistor used in the extraction of the model parameters, and N_FING, which is the ratio of the desired number of fingers to the number of fingers of the transistor used in the extraction of the model parameters. [2]

\[
\text{AREA} = \frac{Z_{\text{new}}}{Z_{\text{extracted}}} \quad (1)
\]

\[
N \_ FING = \frac{N_{\text{Gates}_{\text{extracted}}}}{N_{\text{Gates}_{\text{new}}}} \quad (2)
\]

where \(Z_{\text{new}}\) and \(N_{\text{gates}_{\text{new}}}\) are the gate periphery and number of gate fingers respectively of the desired transistor, and \(Z_{\text{extracted}}\) and \(N_{\text{Gates}_{\text{extracted}}}\) are the gate periphery and number of gate fingers of the extracted transistor.

\[
RD \_ 0 = \frac{RD \_ 0}{\text{AREA}} \quad (3)
\]

\[
RS \_ 0 = \frac{RS \_ 0}{\text{AREA}} \quad (4)
\]

\[
RG \_ 0 = RG \_ 0 \times \text{AREA} \times N \_ FING^2 \quad (5)
\]
\[ RD_{-1} = \frac{RD_{-1}}{AREA} \]  \hspace{1cm} (6)  
\[ RS_{-1} = \frac{RS_{-1}}{AREA} \]  \hspace{1cm} (7)  
\[ RG_{-1} = RG_{-1} \ast AREA \ast N_{\text{FING}}^2 \]  \hspace{1cm} (8)  
\[ RDSO = \frac{RDSO}{AREA} \]  \hspace{1cm} (9)  
\[ GGD = GGD \ast AREA \]  \hspace{1cm} (10)  
\[ GGS = GGS \ast AREA \]  \hspace{1cm} (11)  
\[ RTH_{-0} = \frac{RTH_{-0}}{AREA} \]  \hspace{1cm} (12)  
\[ C_{TH} = C_{TH} \ast AREA \]  \hspace{1cm} (13)  
\[ BETA_{-0} = BETA_{-0} \ast AREA \]  \hspace{1cm} (14)  
\[ BETA_{-1} = BETA_{-1} \ast AREA \]  \hspace{1cm} (15)  
\[ CGS1 = CGS1 \ast AREA \]  \hspace{1cm} (16)  
\[ CGS2 = CGS2 \ast AREA \]  \hspace{1cm} (17)  
\[ CGS4 = CGS4 \ast AREA \]  \hspace{1cm} (18)  
\[ CGD1 = CGD1 \ast AREA \]  \hspace{1cm} (19)  
\[ CGD2 = CGD2 \ast AREA \]  \hspace{1cm} (20)  
\[ CDS1 = CDS1 \ast AREA \]  \hspace{1cm} (21)  
\[ CDS2 = CDS2 \ast AREA \]  \hspace{1cm} (22)  
\[ ISS = ISS \ast AREA \]  \hspace{1cm} (23)  
\[ ISR = ISR \ast AREA \]  \hspace{1cm} (24)  
\[ BR = BR \ast AREA \]  \hspace{1cm} (25)  
\[ RDIODE_{-0} = \frac{RDIODE_{-0}}{AREA} \]  \hspace{1cm} (26)  
\[ RDIODE_{-1} = \frac{RDIODE_{-1}}{AREA} \]  \hspace{1cm} (27)  

5. MET LDMOS Model Equations

5.1 The temperature dependency of parasitic resistances is given by:

\[ Rg = RG_{-0} + RG_{-1} \ast (T - TNOM) \]  \hspace{1cm} (28)  
\[ Rd = RD_{-0} + RD_{-1} \ast (T - TNOM) \]  \hspace{1cm} (29)  
\[ Rs = RS_{-0} + RS_{-1} \ast (T - TNOM) \]  \hspace{1cm} (30)  
\[ T = Vth_{rise} + V_{tsnk} + 273 = Vth_{rise} + TSNK + 273 \]  \hspace{1cm} (31)
where $T$ is the actual or total temperature (not the temperature rise) in K and $TNOM$ is the temperature at which the parameters were extracted. The value of $V_{tsnk}$ ($^\circ$C) is numerically equal to the heat sink temperature $TSNK$ ($^\circ$C). Notice that even though $RG_1$, $RD_1$, and $RS_1$ have units of $\Omega$/K, their numerical value will be the same if the units are $\Omega/^\circ$C.

5.2 The forward bias drain to source current equation is given by:

$$V_{to_1} = VTO_0 + VTO_1(T - TNOM)$$ (32)

$$Beta = BETA_0 + BETA_1(T - TNOM)$$ (33)

$$Vbr = VBR_0 + VBR_1(T - TNOM)$$ (34)

To maintain small signal to large signal model consistency, the gate to source voltage used in the calculation of the large signal drain to source current is delayed $TAU$ seconds.

$$V_{gs _ delayed}(t) = Vgs(t - TAU)$$ (35)

$$Vgst2 = Vgs _ delayed - (Vto_1 + (GAMMA * Vds))$$ (36)

$$Vgst1 = Vgst2 - \frac{1}{2}(Vgst2 + \sqrt{(Vgst2 - VK)^2 + DELTA^2} - \sqrt{VK^2 + DELTA^2})$$ (37)

$$Vgst = VST * ln\left(\frac{Vgst1}{VST} + 1\right)$$ (38)

$$Vbref = \frac{Vbr}{2}(1 + Tanh[M1 - Vgst * M2])$$ (39)

$$Vbrefl = \frac{1}{K2}(Vds - Vbref) + M3\left(\frac{Vds}{Vbref}\right)$$ (40)

$$Ids = (Beta)(Vgst^{VEXP})(1 + LAMBDA * Vds)Tan\left[\frac{Vds * ALPHA}{Vgst}\right](1 + K1 * e^{Vbrefl})$$ (41)

5.3 The forward bias drain to source diode is given by:

$$Vt = \frac{k * T}{q}$$ (42)

where $k$ is the Boltzmann’s constant (1.381e-23 J/K), $T$ is the temperature in Kelvin, and $q$ is the electron charge (1.602E-19 C)

$$Idiode _ f = ISS\left(e^{\frac{(Vds-Vbr)}{N*Vt}}\right)$$ (43)
5.4 The reverse bias drain to source current equation is given by:

\[
V_{to_r} = V_{TO_R} + V_{TO_1} (T - T_{NOM})
\]  
\[V_{gst2} = V_{gs\_delay} - (V_{to_r} - (\text{GAMMA} \times V_{ds}))
\]

\[
V_{gst1} = V_{gst2} - \frac{1}{2} \left( V_{gst2} + \sqrt{V_{gst2} - V_{T} e^{-\frac{1}{2}}} \right) - \sqrt{V_{T}^2 + \Delta V_{T}^2}
\]

\[
V_{gst} = V_{ST} \ln \left( e^{\frac{V_{gst1}}{V_{ST}}} + 1 \right)
\]

\[
I_{ds} = (BR) V_{ds} V_{gst}
\]

5.5 The reverse bias drain to source diode is given by:

\[
Vt2 = \frac{k \times T}{q}
\]

\[
I_{sm} = ISR \times \left( \frac{T}{T_{NOM}} \right)^{\frac{3}{NR}} \left( e^{\left( \frac{E_g}{NRV_{MSS2}} \right) \left( 1 - \frac{T}{T_{NOM}} \right)} - 1 \right)
\]

where \( E_g \) is the energy gap for Silicon which is equal to 1.11 \cite{3} and \( T \) is temperature in Kelvin.

\[
I_{diode\_r} = I_{sm} \times \left( \frac{V_{diode\_r}}{e^{\frac{E_g}{NRV_{MSS2}}} - 1} \right)
\]

The reverse diode's series resistance is given by:

\[
R_{diode} = R_{DIODE\_0} + R_{DIODE\_1} (T - T_{NOM})
\]

5.6 The gate to source capacitance equation is given by:

\[
C_{gs} = (CGS1 + CGS2 \times \left[ 1 + \tanh(CGS6 \times (V_{gs} + CGS3)) \right] + CGS4 \times \left[ 1 - \tanh(V_{gs} \times CGS5) \right] \times (1 + CGST \times (T - T_{NOM}))
\]

5.7 The gate to drain capacitance equation is given by:

\[
C_{gd} = \left( CGDI + \frac{CGD2}{1 + CGD3 \times (V_{gd} - CGD4)^2} \right) \times (1 + CGDT \times (T - T_{NOM}))
\]
5.8 The drain to source capacitance equation is given by:

\[ C_{ds} = \left( C_{DS1} + \frac{C_{DS2}}{1 + C_{DS3} \cdot V_{ds}} \right) \cdot (1 + CDST \cdot (T - T\text{nom})) \]  

(55)

5.9 The noise is calculated as shown in [3], as the sum of the thermal channel noise and the flicker noise as shown by the following equation:

\[ \frac{\overline{id_i^2}}{R} = \frac{8 \cdot k \cdot T \cdot g_m}{3} + KF \cdot \left( \frac{I_{ds}^{AF}}{f_{ffe}} \right) \]  

(56)

where \( g_m \) is the transconductance of the device at the operating point, \( T \) is temperature in Kelvin, and \( f \) is the frequency. In addition all resistors are also modeled as thermal noise sources.

\[ \frac{\overline{id_i^2}}{R} = \frac{4 \cdot k \cdot T}{R} \]  

(57)

where \( R \) is the resistance value and \( T \) is the temperature in Kelvin.

5.10 To avoid convergence problems the maximum temperature rise, \( V_{th\_rise} \) (°C) is limited to 300 °C using the following equation:

\[ V_{th\_rise} = \begin{cases} 
0 & 0 \leq V_{th\_rise} \\
V_{th\_rise} & 0 < V_{th\_rise} < 250 \\
250 + 50 \cdot \tanh \left( \frac{V_{th\_rise} - 250}{50} \right) & 250 \leq V_{th\_rise}
\end{cases} \]  

(58)

6. References

