1 Orderable parts

Table 1. Orderable part variations

Part number [1]	Temperature (T_A)	Package
MC33937APEK	-40 °C to 135 °C	54 SOICW-EP

Notes
1. To order parts in Tape & Reel, add the R2 suffix to the part number.

2 Internal block diagram

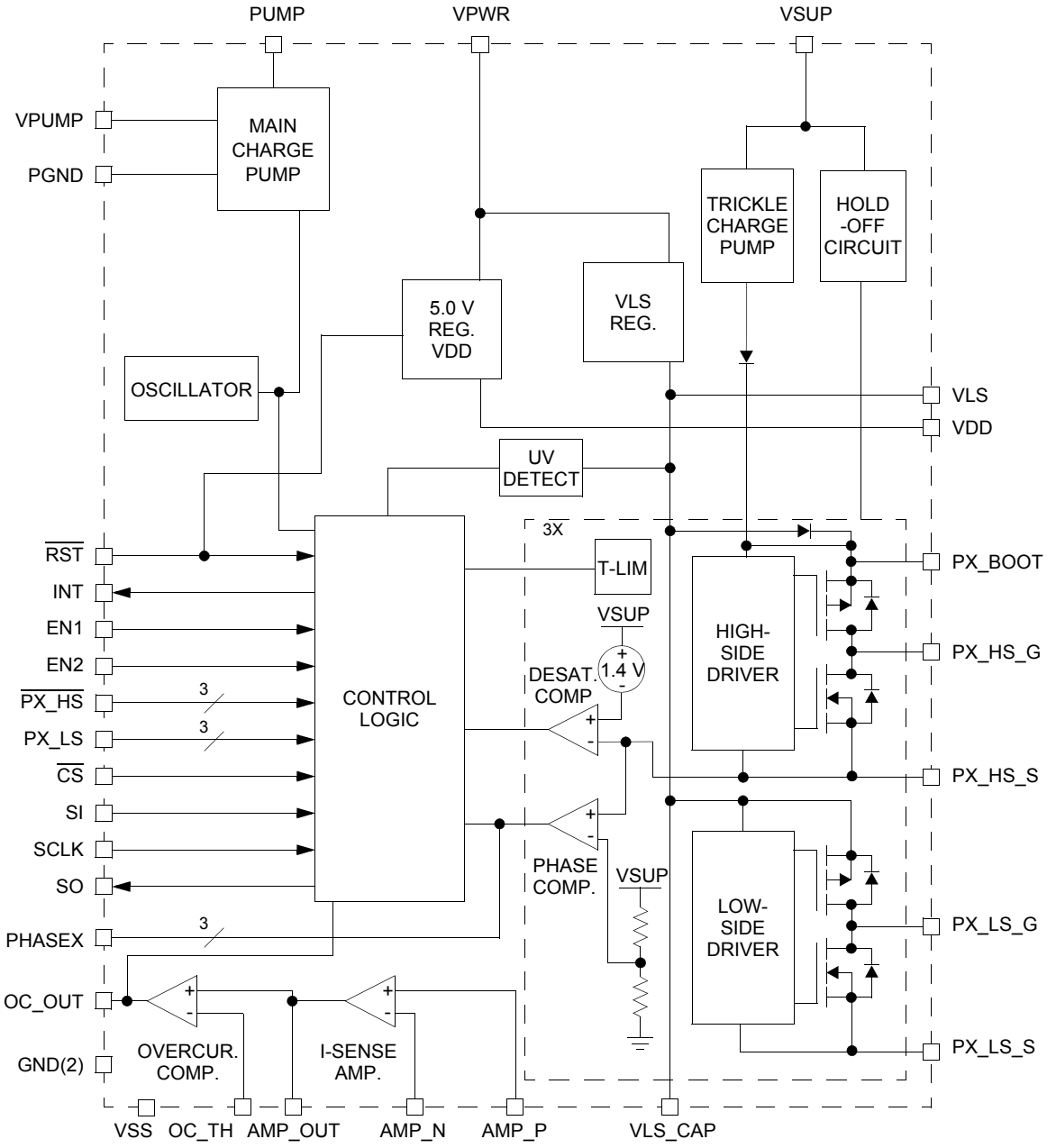

Figure 2. 33937A simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

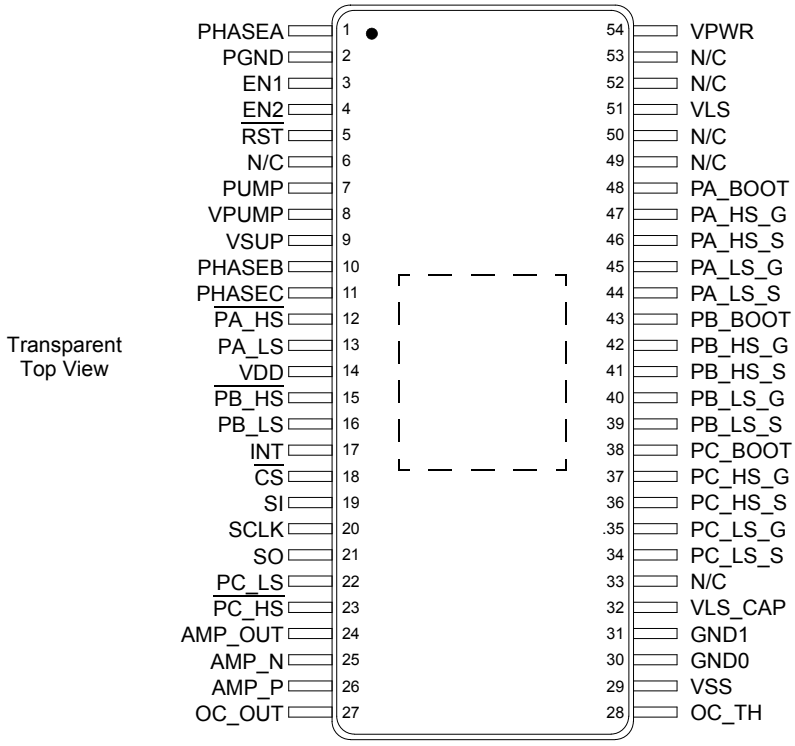

Figure 3. 33937A pin connections

3.2 Pin definitions

A functional description of each pin can be found in the Functional pin description section beginning on page 21.

Table 2. 33937A pin definitions

Pin	Pin name	Pin function	Formal name	Definition
1	PHASEA	Digital Output	Phase A	Totem Pole output of Phase A comparator. This output is low when the voltage on PA_HS_S (Source of High-side FET) is less than 50% of V_{SUP}
2	PGND	Ground	Power Ground	Power ground for charge pump
3	EN1	Digital Input	Enable 1	Logic signal input must be high (ANDed with EN2) to enable any gate drive output.
4	EN2	Digital Input	Enable 2	Logic signal input must be high (ANDed with EN1) to enable any gate drive output
5	$\overline{\text{RST}}$	Digital Input	Reset	Reset input
6, 33, 49, 50, 52, 53	N/C	–	No Connect	Do not connect these pins
7	PUMP	Power Drive Out	Pump	Charge pump output
8	VPUMP	Power Input	Voltage Pump	Charge pump supply
9	VSUP	Analog Input	Supply Voltage	Supply voltage to the load. This pin is to be connected to the common Drains of the external high-side FETs

Table 2. 33937A pin definitions (continued)

Pin	Pin name	Pin function	Formal name	Definition
10	PHASEB	Digital Output	Phase B	Totem Pole output of Phase B comparator. This output is low when the voltage on PB_HS_S (Source of high-side FET) is less than 50% of V_{SUP}
11	PHASEC	Digital Output	Phase C	Totem Pole output of Phase C comparator. This output is low when the voltage on PC_HS_S (Source of high-side FET) is less than 50% of V_{SUP}
12	PA_HS	Digital Input	Phase A High-side	Active low input logic signal enables the high-side driver for Phase A
13	PA_LS	Digital Input	Phase A Low-side	Active high input logic signal enables the low-side driver for Phase A
14	VDD	Analog Output	VDD Regulator	VDD regulator output capacitor connection.
15	PB_HS	Digital Input	Phase B High-side	Active low input logic signal enables the high-side driver for Phase B
16	PB_LS	Digital Input	Phase B Low-side	Active high input logic signal enables the low-side driver for Phase B
17	INT	Digital Output	Interrupt	Interrupt pin output
18	CS	Digital Input	Chip Select	Chip Select input. It frames SPI commands and enables SPI port
19	SI	Digital Input	Serial In	Input data for SPI port. Clocked on the falling edge of SCLK, MSB first
20	SCLK	Digital Input	Serial Clock	Clock for SPI port and typically is 3.0 MHz
21	SO	Digital Output	Serial Out	Output data for SPI port. Tri-state until $\overline{CS}$ becomes low
22	PC_LS	Digital Input	Phase C Low-side	Active high input logic signal enables the low-side driver for Phase C
23	PC_HS	Digital Input	Phase C High-side	Active low input logic signal enables the high-side driver for Phase C
24	AMP_OUT	Analog Output	Amplifier Output	Output of the current-sensing amplifier
25	AMP_N	Analog Input	Amplifier Invert	Inverting input of the current-sensing amplifier
26	AMP_P	Analog Input	Amplifier Non-Invert	Non-inverting input of the current-sensing amplifier
27	OC_OUT	Digital Output	Overcurrent Out	Totem pole digital output of the overcurrent comparator
28	OC_TH	Analog Input	Overcurrent Threshold	Threshold of the overcurrent detector
29	VSS	Ground	Voltage Source Supply	Ground reference for logic interface and power supplies
30, 31	GND	Ground	Ground	Substrate and ESD reference, connect to VSS
32	VLS_CAP	Analog Output	VLS Regulator Output Capacitor	VLS Regulator connection for additional output capacitor, providing low-impedance supply source for low-side gate drive
34	PC_LS_S	Power Input	Phase C Low-side Source	Source connection for Phase C low-side FET
35	PC_LS_G	Power Output	Phase C Low-side Gate Drive	Gate drive output for Phase C low-side
36	PC_HS_S	Power Input	Phase C High-side Source	Source connection for Phase C high-side FET
37	PC_HS_G	Power Output	Phase C High-side Gate Drive	Gate Drive for output Phase C high-side FET
38	PC_BOOT	Analog Input	Phase C Bootstrap	Bootstrap capacitor for Phase C
39	PB_LS_S	Power Input	Phase B Low-side Source	Source connection for Phase B low-side FET
40	PB_LS_G	Power Output	Phase B Low-side Gate Drive	Gate Drive for output Phase B low-side
41	PB_HS_S	Power Input	Phase B High-side Source	Source connection for Phase B high-side FET
42	PB_HS_G	Power Output	Phase B High-side Gate Drive	Gate Drive for output Phase B high-side
43	PB_BOOT	Analog Input	Phase B Bootstrap	Bootstrap capacitor for Phase B
44	PA_LS_S	Power Input	Phase A Low-side Source	Source connection for Phase A low-side FET

Table 2. 33937A pin definitions (continued)

Pin	Pin name	Pin function	Formal name	Definition
45	PA_LS_G	Power Output	Phase A Low-side Gate Drive	Gate Drive for output Phase A low-side
46	PA_HS_S	Power Input	Phase A High-side Source	Source connection for Phase A high-side FET
47	PA_HS_G	Power Output	Phase A High-side Gate Drive	Gate Drive for output Phase A high-side
48	PA_BOOT	Analog Input	Phase A Bootstrap	Bootstrap capacitor for Phase A
51	VLS	Analog Output	VLS Regulator	VLS regulator output. Power supply for the gate drives
54	VPWR	Power Input	Voltage Power	Power supply input for gate drives
	EP	Ground	Exposed Pad	Device will perform as specified with the exposed pad un-terminated (floating) however, it is recommended that the exposed pad be terminated to pin 29 (VSS) and system ground

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to V_{SS} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
V_{SUP}	VSUP Supply Voltage • Normal Operation (Steady-state) • Transient Survival	 58 -1.5 to 80	V	(2)
V_{PWR}	VPWR Supply Voltage • Normal Operation (Steady-state) • Transient Survival	 58 -1.5 to 80	V	(2)
V_{PUMP}	Charge Pump (PUMP, VPUMP)	-0.3 to 40	V	
V_{LS}	VLS Regulator Outputs (VLS, VLS_CAP)	-0.3 to 18	V	
V_{DD}	Logic Supply Voltage	-0.3 to 7.0	V	
V_{OUT}	Logic Output (INT, SO, PHASEA, PHASEB, PHASEC, OC_OUT)	-0.3 to 7.0	V	(3)
V_{IN}	Logic Input Pin Voltage (EN1, EN2, $\overline{Px\_HS}$, Px_LS, SI, SCLK, $\overline{CS}$, $\overline{RST}$) 10 mA	-0.3 to 7.0	V	
V_{IN_A}	Amplifier Input Voltage • (Both Inputs-GND), (AMP_P - GND) or (AMP_N - GND) 6.0 mA source or sink	-7.0 to 7.0	V	
V_{OC}	Overcurrent comparator threshold 10 mA	-0.3 to 7.0	V	
V_{BOOT} V_{HS_G} V_{LS_G}	Driver Output Voltage • High-side bootstrap (PA_BOOT, PB_BOOT, PC_BOOT) • High-side (PA_HS_G, PB_HS_G, PC_HS_G) • Low-side (PA_LS_G, PB_LS_G, PC_LS_G)	 75 75 16	V	(4)
V_{HS_G} V_{HS_S} V_{LS_G} V_{LS_S}	Driver Voltage Transient Survival • High-side (PA_HS_G, PB_HS_G, PC_HS_G, PA_HS_S, PB_HS_S, PC_HS_S) • Low-side (PA_LS_G, PB_LS_G, PC_LS_G, PA_LS_S, PB_LS_S, PC_LS_S)	 -7.0 to 75.0 -7.0 to 75.0 -7.0 to 18.0 -7.0 to 7.0	V	(5)
V_{ESD}	ESD Voltage • Human Body Model - HBM (All pins except for the pins listed below) Pins: PA_Boot, PA_HS_S, PA_HS_G, PB_Boot, PB_HS_S, PB_HS_G, PC_Boot, PC_HS_S, PC_HS_G, VPWR • Charge Device Model - CDM • Corner pins • All other pins	 ±2000 ±1000 ±750 ±300	V	(6)

Notes

2. The device will withstand load dump transient as defined by ISO7637 with peak voltage of 80 V.
3. Short-circuit proof, the device will not be damaged or induce unexpected behavior due to shorts to external sources within this range.
4. This voltage should not be applied without also taking voltage at HS_S and voltage at PX_LS_S into account.
5. Actual operational limitations may differ from survivability limits. The V_{LS} - V_{LS_S} differential and the V_{BOOT} - V_{HS_S} differential must be greater than 3.0 V to insure the output gate drive will maintain a commanded OFF condition on the output.
6. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).

Table 3. Maximum ratings (continued)

All voltages are with respect to V_{SS} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Thermal ratings				
T_{STG}	Storage Temperature	-55 to +150	°C	
T_J	Operating Junction Temperature	-40 to +150	°C	
$R_{\theta JC}$	Thermal Resistance • Junction-to-Case	3.0	°C/W	(7)
T_{SOLDER}	Soldering Temperature	Note 9	°C	(8)

Notes

7. Case is considered EP - pin 55 under the body of the device. The actual power dissipation of the device is dependent on the operating mode, the heat transfer characteristics of the board and layout and the operating voltage. See Figure 24 and Figure 25 for examples of power dissipation profiles of two common configurations. Operation above the maximum operating junction temperature will result in a reduction in reliability leading to malfunction or permanent damage to the device.
8. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.NXP.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power inputs						
V_{PWR_ST}	VPWR Supply Voltage Startup Threshold	–	6.0	8.0	V	(10)
I_{SUP}	VSUP Supply Current, V_{PWR} = V_{SUP} = 40 V, $\overline{RST}$ and ENABLE = 5.0 V • No output loads on Gate Drive Pins, No PWM • No output loads on Gate Drive Pins, 20 kHz, 50% Duty Cycle	 – –	 1.0 –	 – 10	mA	
I_{PWR_ON}	VPWR Supply Current, V_{PWR} = V_{SUP} = 40 V, $\overline{RST}$ and ENABLE = 5.0 V • No output loads on Gate Drive Pins, No PWM, Outputs initialized • Output Loads = 620 nC per FET, 20 kHz PWM	 – –	 11 –	 20 95	mA	 (11)
I_{SUP} I_{PWR}	Sleep State Supply Current, $\overline{RST}$ = 0 V • V_{SUP} = 40 V • V_{PWR} = 40 V	 – –	 14 56	 30 100	µA	
V_{GATESS}	Sleep State Output Gate Voltage • IG < 100 µA	–	–	1.3	V	
V_{Boot}	Trickle Charge Pump (Bootstrap Voltage) • V_{SUP} = 14 V	22	28	32	V	(15)
V_F	Bootstrap Diode Forward Voltage at 10 mA	–	–	1.2	V	
VDD internal regulator						
V_{DD}	V_{DD} Output Voltage, V_{PWR} = 8 to 40 V, C = 0.47 µF • External Load I_{DD_EXT} = 0 to 1.0 mA	4.5	–	5.5	V	(12)
I_{DD}	Internal V_{DD} Supply Current, V_{DD} = 5.5 V, No External Load	–	–	12	mA	
VLS regulator						
I_{PEAK}	Peak Output Current, V_{PWR} = 16 V, V_{LS} = 10 V	350	600	800	mA	
V_{LS}	Linear Regulator Output Voltage, I_{VLS} = 0 to 60 mA, V_{PWR} > V_{LS} + 2.0 V	13.5	15	17	V	(13)
V_{THVLS}	VLS Disable Threshold	7.5	8.0	8.5	V	(14)

Notes

10. Operation with the Charge Pump is recommended when minimum system voltage could be less than 14 V. V_{PWR} must exceed this threshold in order for the Charge Pump and V_{DD} regulator to startup and drive V_{PWR} to > 8.0 V. Once V_{PWR} exceeds 8.0 V, the circuits will continue to operate even if system voltage drops below 6.0 V.
11. This parameter is guaranteed by design. It is not production tested.
12. Minimum external capacitor for stable V_{DD} operation is 0.47 µF.
13. Recommended external capacitor for the V_{LS} regulator is 2.2 µF low ESR at each pin VLS and VLS_CAP.
14. When V_{LS} is less than this value, the outputs are disabled and HOLDOFF circuits are active. Recovery requires initialization when V_{LS} rises above this threshold again. A filter delay of approximately 700 ns on the comparator output eliminates responses to spurious transients on V_{LS}.
15. See Figure 11 for typical capability to maintain gate voltage with a 5.0 µA load.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Charge pump						
$R_{DS(on)\_HS}$ $R_{DS(on)\_LS}$ V_{THREG}	Charge Pump • High-side Switch On Resistance • Low-side Switch On Resistance • Regulation Threshold Difference	 – – 250	 6.0 5.0 500	 10 9.4 900	 Ω Ω mV	(16), (18)
V_{CP}	Charge Pump Output Voltage • I_{OUT} = 40 mA, 6.0 V < V_{SYS} < 8.0 V • I_{OUT} = 40 mA, V_{SYS} > = 8.0 V	 8.5 12	 9.5 –	 – –	 V	(17), (18)
Gate drive						
$R_{DS(on)\_H\_SRC}$	High-side Driver On Resistance (Sourcing) • V_{PWR} = V_{SUP} = 16 V, -40 °C ≤ T_A ≤ 25 °C • V_{PWR} = V_{SUP} = 16 V, 25 °C < T_A ≤ 135 °C	 – –	 – –	 6.0 8.5	 Ω	
$R_{DS(on)\_H\_SINK}$	High-side Driver On Resistance (Sinking) • V_{PWR} = V_{SUP} = 16 V	–	–	3.0	Ω	
I_{HS_INJ}	High-side Current Injection Allowed Without Malfunction	–	–	0.5	A	(18), (19)
$R_{DS(on)\_L\_SRC}$	Low-side Driver On Resistance (Sourcing) • V_{PWR} = V_{SUP} = 16 V, -40 °C ≤ T_A ≤ 25 °C • V_{PWR} = V_{SUP} = 16 V, 25 °C < T_A ≤ 135 °C	 – –	 – –	 6.0 8.5	 Ω	
$R_{DS(on)\_L\_SINK}$	Low-side Driver On-Resistance (Sinking) • V_{PWR} = V_{SUP} = 16 V	–	–	3.0	Ω	
I_{LS_INJ}	Low-side Current Injection Allowed Without Malfunction	–	–	0.5	A	(18), (19)
V_{GS_H} V_{GS_L}	Gate Source Voltage, V_{PWR} = V_{SUP} = 40 V • High-side, I_{GATE} = 0 • Low-side, I_{GATE} = 0	 13 13	 14.8 15.4	 16.5 17	 V	(20)
$V_{HS\_G\_HOLD}$	Reverse High-side Gate Holding Voltage Gate Output Holding Current = 2.0 µA Gate Output Holding Current = 5.0 µA, V_{SUP}<26 V Gate Output Holding Current = 5.0 µA, V_{SUP}<40 V	 – – –	 10 10 –	 15 15 15	 V	(21)

Notes

16. When VLS is this amount below the normal VLS linear regulation threshold, the charge pump is enabled.
17. V_{SYS} is the system voltage on the input to the charge pump. Recommended external components: 1.0 µF MLC, MUR 120 diode.
18. This parameter is a design characteristic, not production tested.
19. Current injection only occurs during output switch transitions. The IC is immune to specified injected currents for a duration of approximately 1.0 µs after an output switch transition. 1.0 µs is sufficient for all intended applications of this IC.
20. If a slightly higher gate voltage is required, larger bootstrap capacitors are required. At high duty cycles, the bootstrap voltage may not recover completely, leading to a higher output on-resistance. This effect can be minimized by using low ESR capacitors for the bootstrap and the VLS capacitors.
21. High-side Gate Holding voltage is the voltage between the Gate and Source of the high-side FET when held in an on condition. The trickle charge pump supplies bias and holding current for the High-side FET gate driver and output to maintain voltages after bootstrap events. See Figure 11 for typical 100% high-side gate voltage with a 5.0 µA load. This parameter is a design characteristic, not production tested.