Magnetoresistive Random Access Memory

Freescale Semiconductor, Inc.

Introduction

Magnetoresistive Random Access Memory (MRAM) combines a magnetic device with standard silicon-based microelectronics to obtain the combined attributes of non-volatility, high-speed operation and unlimited read and write endurance not found in any other existing memory technology. In this paper we provide an overview of Freescale's MRAM technology and describe the MR2A16A, a 4 Mbit MRAM device. As shown in Figure 1, the memory is based on a 1-transistor, 1-magnetic tunnel junction (1T1MTJ) memory cell that employs a novel bit structure and approach for operation. The MR2A16A is fabricated with a 0.18µm CMOS process using five levels of metal, including program current lines clad with highly permeable material for magnetic flux concentration. We describe how the cell architecture, bit structure, and the toggle switching mode are combined to provide significantly improved operational performance and manufacturability as compared to MRAM based on conventional switching.

MRAM Description

MRAM is based on magnetic memory elements integrated with CMOS. Each memory element uses a magnetic tunnel junction (MTJ) device for data storage. The MTJ is composed of a fixed magnetic layer, a thin dielectric tunnel barrier, and a free magnetic layer. When a bias is applied to the MTJ, electrons that are spin polarized by the magnetic layers traverse the dielectric barrier through a process known as tunneling. The MTJ device has a low resistance when the magnetic moment of the free layer is parallel to the fixed layer and a high resistance when the free layer moment is oriented anti-parallel to the fixed layer moment. This change in resistance with the magnetic state of the device is an effect known as magnetoresistance, hence the name "Magnetoresistive" RAM.

Unlike most other semiconductor memory technologies, the data is stored as a magnetic state, rather than charge, and sensed by measuring the resistance without disturbing the magnetic state. Using a magnetic state for storage has two main benefits: 1) the magnetic polarization does not leak away with time like charge does, so the information is stored even when the power is turned off; and 2) switching the magnetic polarization between the two states does not involve actual movement of electrons or atoms and thus has no known wear-out mechanism. The magnetoresistive device used in MRAM is very similar to the device used for the reader in hard disk drives.

To make a high-density memory, the MRAM cells shown in Figure 1 are arranged in a matrix with each write line spanning hundreds or thousands of bits as shown in Figure 2. During the write operation, current pulses are passed through a digit line and a bit line, writing only the bit at the cross point of those two lines. During the read operation the isolation transistor of the target bit is turned on to bias the MTJ and the resulting current is compared to a reference to determine if the resistance state is low are high.

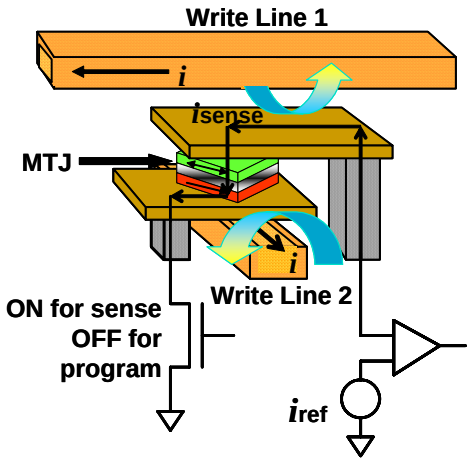

Figure 1. Schematic of a 1-transistor, 1-MTJ memory cell showing the write lines above and below the bit and the read current path.

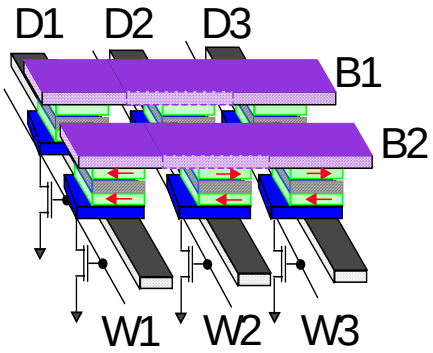

Figure 2. A memory array consisting of many MRAM cells with digit and bit lines for cross-point writing and isolation transistors controlled by word lines.

Toggle MRAM

Freescale's Toggle approach to bit programming effectively eliminates the single-line disturb phenomenon present in previous approaches to MRAM switching. Through the use of a new free layer structure, bit orientation and current pulse sequence, the MRAM bit state can be programmed via a "Toggle" mode we have named "Savtchenko switching" after its late inventor. "Toggle" means that the exact same pulse sequence is used to write from the "0" state to the "1" state and for "1" to

"0;" each time the sequence is executed the device changes from its current magnetic state to the opposite state. This type of switching is significantly different from the simple type of switching where the magnetic moment of the free layer simply follows the applied field. Because the switching mode is fundamentally different, the selectivity using this mode is greatly enhanced as described below.

Savtchenko switching relies on the unique behavior of a synthetic antiferromagnet (SAF) free layer that is formed from two ferromagnetic layers separated by a non-magnetic coupling spacer layer. This is shown schematically in Figure 3. The moment-balanced SAF free-layer responds to an applied magnetic field differently than the single ferromagnetic layer of conventional MRAM. Rather than following an applied magnetic field, the two antiparallel layer magnetizations will rotate to be approximately orthogonal to the applied field. A current pulse sequence is used to generate a rotating magnetic field that moves the free-layer moments through the 180-degree switch from one state to the other, as shown in Figure 4.

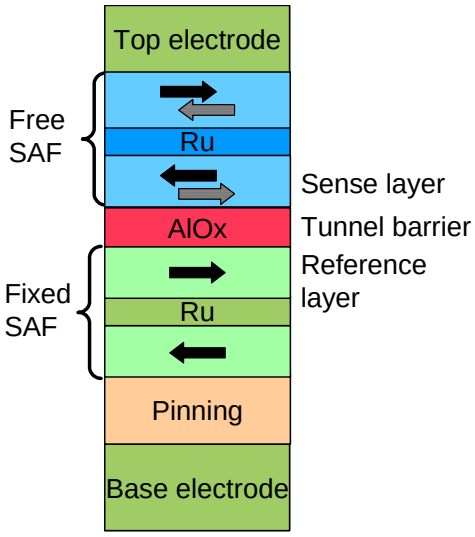

Figure 3. The magnetic tunnel junction (MTJ) material stack used for Toggle MRAM. The Free SAF magnetic moments switch between two states when the proper magnetic field sequence is applied. Electrons tunnel across the alumina (AlOx) tunnel barrier, resulting in a magnetoresistance that is sensitive to the magnetic moment direction of the sense layer.

To exploit the unique field response of this free layer, a two-phase programming pulse sequence, shown in Figure 5, is applied to effectively rotate the magnetic moments of the SAF by 180 degrees. Because of the inherent symmetry, this sequence toggles the bit to the opposite state regardless of existing state. A pre-read is therefore used to determine if a write is required. Because of the way a SAF responds to applied fields, a single line alone cannot switch the bit, providing greatly enhanced selectivity over the previous approaches to MRAM switching.

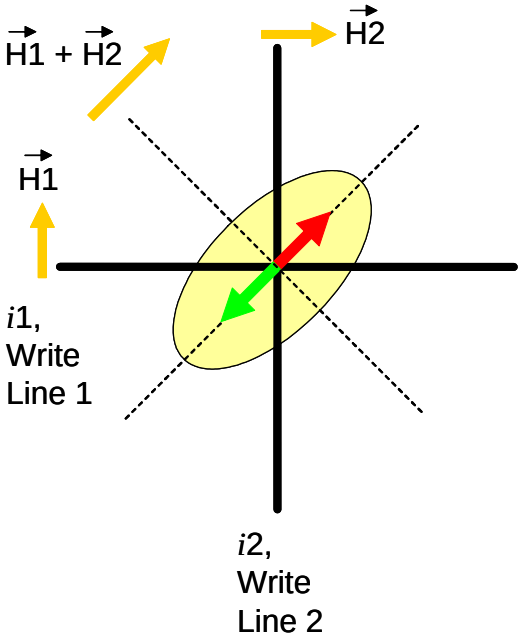

Figure 4. Schematic of a toggle MRAM bit with the field sequence used to switch the free layer from one state to the other. The fields, H1, H1+H2, and H2, are produced by passing currents, *i1* and *i2*, through the write lines.

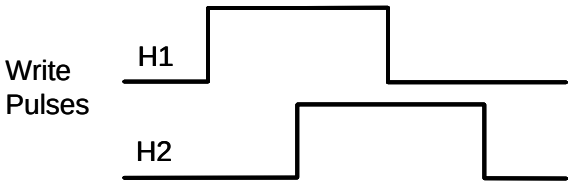

Figure 5. The current pulse sequence used to produce the sequence of magnetic fields used for toggle switching.

Figure 6 is a switching characteristic map versus current for an entire 4-Mbit memory. In the region below the switching threshold, no bits changed state and hence there were no disturbs from half selects. A large operating region is observed above the threshold consistent with the single bit characteristic presented above. The contours in the transition region just at the threshold are a measure of the bit-to-bit switching distribution. Note that there are no disturbs all the way up to the highest currents, displaying the remarkable resistance to single-line disturbs with this approach.

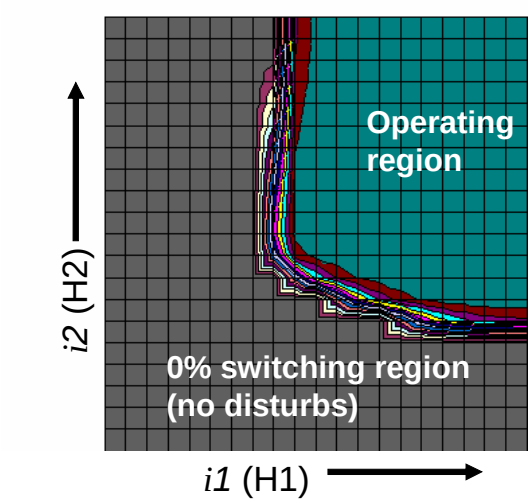

Figure 6. Measured toggling characteristic map of an entire 4-Mbit die showing the large operating region.

Integration of Magnetic Devices with CMOS

A schematic cross-sectional view of our integrated MRAM cell for a 1T1MTJ cell architecture is shown in Figure 7. In this case, the MRAM process module is integrated between the last two layers of metal in an otherwise standard semiconductor process flow. The MRAM module is termed a "back-end" module because it is inserted after all of the associated CMOS circuitry is fabricated. This integration scheme requires no alteration to the front-end CMOS process flow. This back-end approach separates the specialized magnetic materials processing from the standard CMOS process.

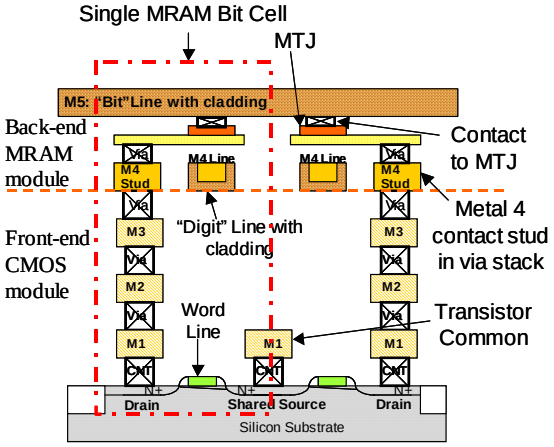

Figure 7. A schematic cross-sectional view of our integrated MRAM cell for a 1T1MTJ cell architecture. The MRAM module is inserted after the front-end CMOS (above the horizontal red line).

This integration scheme lends itself to embedded applications, where the memory core is part of a non-memory circuit such as a processor or controller. For example, a processor may need to have some fast memory and some non-volatile memory on board; MRAM could provide both capabilities. Because the MRAM module is independent of the front-end CMOS, the MRAM capability can be added without perturbing the CMOS logic process. This approach may provide cost and performance advantages in many system-on-chip applications.

Comparison to Other Memory Technologies

Comparison of MRAM with other memory technologies suggests that it can be competitive in overall performance. Since MRAM is nonvolatile, it retains the data when completely turned off. System power can be significantly reduced compared to DRAM by shutting down the MRAM when inactive since there is no background refreshing required. The straightforward integration scheme used for MRAM makes it easier to embed.

Comparison with SRAM shows that MRAM will compete favorably in cost because of its smaller cell size. It also is non-volatile, which is only available in more complex and expensive battery backup solutions for SRAM.

When compared with Flash, MRAM achieves much better performance in write characteristics since no high-voltage tunneling mode is required and MRAM write cycle is much faster. MRAM consumes much less energy in a write cycle because the energy/bit is several orders of magnitude lower than Flash. In addition, MRAM endurance is unlimited, with no known or expected deterioration mechanism, while typical Flash endurance is only 10^5 write cycles.

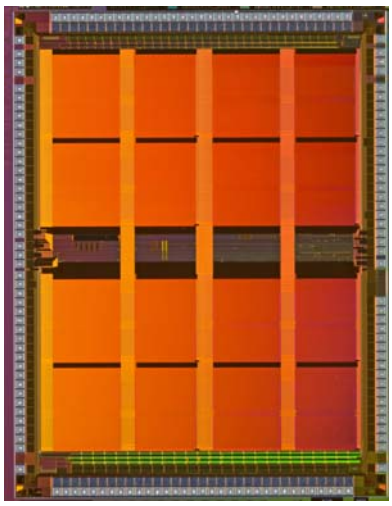

Figure 8. Micrograph of the MR2A16A MRAM device.