Differences Between S12 And S12X Cores

	S12X Cores			S12 Core
Attribute	S12XD-- New! (XB and XD Families)	S12XE -- New! (XE Family)	S12XS -- New! (XS Family)	S12 -- Legacy (C, D, H, Q, and R Families)
Bus Speed	40 MHz	50 MHz	40 MHz	25 MHz
CPU	16-bit CPU12XV1	16-bit CPU12XV2	16-bit CPU12XV2	16-bit CPU12
Debug	- BDM (enhanced to support global paging accesses) - DBG Debugger monitor CPU - XGATE busses and four comparators	- BDM (enhanced to support global paging accesses) - DBG Debugger monitor CPU - XGATE busses and four comparators	- BDM (enhanced to support global paging accesses) - DBG Debugger monitor CPU	- BDM (Single-wire background debug)
System Protection Features	- Low-voltage detect/interrupt	- Memory Protection Unit (MPU) to protect undesired accesses - Low-voltage detect/interrupt on all devices in family - Error Correction Code	- Low voltage detect/interrupt on all devices in family - Error Correction Code	- Low voltage detect/interrupt
Oscillator Choices	- Loop controlled or full swing Pierce (XOSC) circuitry enhanced to dynamically control gain of the output amplitude for low harmonic distortion - Low power and good noise immunity - Eliminates bias resistor	- Loop controlled or full swing Pierce (XOSC) circuitry enhanced to dynamically control gain of the output amplitude for low harmonic distortion - Low power and good noise immunity - Eliminates bias resistor	- Loop controlled or full swing Pierce (XOSC) circuitry enhanced to dynamically control gain of the output amplitude for low harmonic distortion - Low power and good noise immunity - Eliminates bias resistor	- Colpitts of Full swing Pierce
Clock	- Phased Lock Loop (PLL)	- Phase Lock Loop (PLL) enhanced circuitry for elimination of external components	- Phase Lock Loop (PLL) enhanced circuitry for elimination of external components	- Phase Lock Loop (PLL)
Analog to Digital Converter (ADC)	- 8/10 bit resolution, 7µs conversion time	- 8/10/12 bit resolution, conversion time as low as 2.12µs	- 8/10/12 bit resolution, conversion time as low as 2.12µs	- 8/10 bit resolution, 7µs conversion time
EEPROM	- Small sector Flash to emulate EEPROM	- Emulated EEPROM with Data Flash and RAM buffer	- Small sector Flash to emulate EEPROM	- Small sector Flash to emulate EEPROM
Timer	Enhanced Capture Time (ECT) - Timer (TIM) - Periodic Interrupt Timer (PIT)	Enhanced Capture Time (ECT) - Timer (TIM) - Periodic Interrupt Timer (PIT)	Enhanced Capture Time (ECT) - Timer (TIM) - Periodic Interrupt Timer (PIT)	- Enhanced Capture Timer (ECT) - Timer (TIM)
XGATE	- XGATE programmable high performance I/O co-processor module (up to 80 MIPS RISC performance)	- XGATE programmable high performance I/O co-processor module (up to 80 MIPS RISC performance)	Not applicable	Not applicable
Interrupt Nesting	- Enhanced Interrupt Module with eight levels	- Enhanced Interrupt Module with eight levels	- Enhanced Interrupt Module with eight levels	- Standard Interrupt module