Errata to

MPCFPE32BAD/AD
Rev. 0, 10/2002

Errata to Programming Environments Manual for 32-Bit Implementations of the PowerPC Architecture, Rev. 2

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This errata describes corrections to the *Programming Environments Manual for 32-Bit Implementations of the PowerPC Architecture, Rev 2*. For convenience, the section number and page number of the errata item in the programming manual are provided.

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Section, Page No.	Changes
4.4.3.1,4-63	In Table 4-37, add the following two sentences to the end of the **dcbi** operation: Note that some implementations may execute this instruction as a **dcbf**. This instruction is optional.
7.1,7-1	Replace the fourth paragraph with the following: The segment information, used to generate the interim virtual addresses, is stored as segment descriptors. These descriptors may reside in on-chip segment registers (32-bit implementations).
7.3.1.1, 7-3	Remove this section.

8.2, 8-24	Replace the target address CTR || 0b00 of **bcctr** with CTR[0–29] || 0b00, the code sequence should read as follows:
	`cond_ok ← BO[0] | (CR[BI] ≡ BO[1])`
	`if cond_ok then`
	`NIA ←iea CTR[0-29] || 0b00`
	`if LK then LR ←iea CIA + 4`

8.2, 8-26	In the first sentence after Table 8-9, replace the target address CTR || 0b00 of **bcctr** with CTR[0–29] || 0b00. The sentence should read as follows: The branch target address is CTR[0–29] || 0b00.

8.2, 8-26	Replace the target address LR || 0b00 of **bclr** with CTR[0–29] || 0b00, the code sequence should read as follows:
	`if ¬ BO[2] then CTR ← CTR - 1`
	`ctr_ok ← BO[2] | ((CTR ≠ 0) ⊕ BO[3])`
	`cond_ok ← BO[0] | (CR[BI] ≡ BO[1])`
	`if ctr_ok & cond_ok then`
	`NIA ←iea LR[0-29] || 0b00`
	`if LK then LR ←iea CIA + 4`

8.2, 8-25	In the first sentence after Table 8-11, replace the target address LR || 0b00 of **bclr** with LR[0–29] || 0b00. The sentence should read as follows: The branch target address is LR[0–29] || 0b00.
8.2, 8-43	Add the following two sentences to the end of the **dcbi** description: Note that some implementations may execute this instruction as a **dcbf**. This instruction is optional.

Section, Page No.	Changes
8.2, 8-44	After the third paragraph, add the following paragraph: The coherency state of a cache block after a write access (caused by a **dcbst**) is implementation-dependent. For example, some implementations may mark the cache block exclusive, where others may mark it invalid.
8.2, 8-163	Replace the first sentence of the only paragraph, the sentence should read as follows: The contents of **r**S are shifted right the number of bits specified by **r**B[27–31].

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