Dual-Metal Gate CMOS with HfO₂ Gate Dielectric


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Abstract

We report for the first time on a novel dual-metal gate CMOS integration on HfO₂ gate dielectric using TiN (PMOS) and TaSiN (NMOS) gate electrodes. Compared to a single metal integration, the dual-metal integration does not degrade gate leakage, mobility and charge trapping behavior. Promising preliminary TDDB data was obtained from dual-metal gate MOSFETs, while still delivering much improved gate leakage ($10^4$ - $10^5$X better than SiO₂).

Introduction

We report for the first time on a novel dual-metal gate HfO₂ CMOS integration with TaSiN (NMOS) and either PVD or CVD TiN (PMOS). As CMOS dimensions are scaled down, some of the issues like gate depletion, boron penetration and resistance increase associated with polysilicon (poly) gates can be addressed through the use of metal gates. It is well established now that for bulk CMOS at sub-50nm gate lengths, two different metal gates with work-functions within about 0.2eV of the band-edges will be required as replacements to n+ and p+ poly (1,2). Fabricating CMOS circuits with gate electrodes made of two different materials in a cost-effective manner is non-trivial. Simple approaches to dual-metal gate integration like work-function engineering of Mo and TiN through N implantation have been proposed, but there are problems like enhanced gate leakage from N penetration of the dielectric and insufficient work-function shift (3-5).

Lu et al. reported a self-aligned dual-metal gate integration on Si₃N₄ gate dielectric with Ti (NMOS) and Mo (PMOS) gates, but they found that the dielectric was etched in the PMOS regions (6). HfO₂ is a leading high K gate dielectric candidate. PVD Ta₅Si₃N (TaSiN) and PVD and CVD TiN have been reported as useful dual-metal gate candidates on HfO₂ (7,8).

Experiment

The HfO₂ gate dielectric in this study was deposited by either MOCVD (Metal-organic chemical vapor deposition) or ALCVD (Atomic layer chemical vapor deposition). PVD TaSiN and PVD TiN gates were reactively sputtered. CVD TiN was deposited using Tetrakis-dimethylamino-titanium. A 0.13µm CMOS process flow was modified for the dual-metal gate integration. The basic integration has proved successful on several different lots, each with a different combination of gate electrode and gate dielectric thickness.

Results and Discussion

(a) Dual-metal Gate Integration

Fig. 1 shows the key steps in creating two different metal gate stacks in the NMOS and PMOS regions of the die. SEM images of an SRAM array in different stages of the process integration are also shown.
After the HfO\textsubscript{2} deposition, the PMOS metal, (CVD or PVD) TiN is deposited all across the wafer. An oxide hard mask is patterned using the p-well mask to expose the NMOS regions of the die. The exposed TiN is etched off using a wet clean. After etching off the oxide, the NMOS metal, TaSiN and a poly capping layer are deposited. The HfO\textsubscript{2} gate dielectric in the NMOS areas is exposed to TiN deposition and wet-cleans prior to the TaSiN deposition. HfO\textsubscript{2} in this study was found to be robust enough to result in <1Å difference in inversion capacitance equivalent thickness (CET\textsubscript{inv}) between NMOS and PMOS. The gate etch process was optimized to etch through different metal stacks in the NMOS and PMOS regions of the die and successfully stop on HfO\textsubscript{2} (Fig. 2).

(b) Transistor Characterization

P- and N-MOSFET high frequency CV characteristics are shown in Fig. 3. There is no gate depletion as expected with metal gates. There is <30mV shift in V\textsubscript{fb} in both n- and p-MOSFETs between forward (accumulation to inversion) and reverse V\textsubscript{g} sweeps (not shown). Fig. 4 shows well-behaved long channel n-MOSFET (TaSiN gate) and p-MOSFET (CVD TiN gate) output characteristics. Fig. 5 shows sub-threshold characteristics of 10\mu m \times 10\mu m (W \times L) p- and n-MOSFETs with different metal gates on ALD or MOCVD HfO\textsubscript{2}. The sub-threshold swing (SS) for p-MOSFETs is in the 70-80mV/dec range. MOCVD HfO\textsubscript{2} n-MOSFETs with TaSiN gates show an improvement in SS from previously reported degraded values of 150 mV/dec to 110 mV/dec (8).
Figs. 6a and 6b show gate leakage as a function of CETinv for dual-metal gate n- and p-MOSFETs respectively measured at 1V beyond Vt. There is a $\sim 10^{4}$ X and $10^{5}$ X lower gate leakage in dual-metal gate HfO$_2$ n- and p-MOSFETs respectively compared to poly/SiO$_2$ MOSFETs. The effective hole mobility ($\mu_{eff}$) as a function of effective field ($E_{eff}$) for different TiN/HfO$_2$ long channel p-MOSFETs is shown in Fig. 7. Note that the $E_{eff}$ for metal-gated devices is much lower compared to p+poly/SiO$_2$ devices due to lower channel doping and lower work-function of the gate electrode.

We plot $\mu_{eff}$ against inversion charge carrier density ($N_{inv}$) in such cases for better comparison. Fig. 8 is the same $\mu_{eff}$ data as in Fig. 7, plotted against $N_{inv}$. We find that at similar $N_{inv}$ the effective hole mobilities of metal-gated HfO$_2$ devices are comparable to poly/SiO$_2$ devices. Effective electron mobility for TaSiN/HfO$_2$ n-MOSFETs was found to be 39% lower than poly/SiON at an $E_{eff}$=1 MV/cm (Fig. 9). The electron $\mu_{eff}$ data from dual-metal gates is comparable to or better than the single metal gate data at similar $N_{inv}$ suggesting that the new integration does not further degrade mobility (Fig. 10).

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**Fig. 6** Gate leakage versus CETinv data for (a) n-MOSFETs and (b) p-MOSFETs measured at 1V beyond Vt.

**Fig. 7** Effective hole mobility of dual-metal gate HfO$_2$ p-MOSFETs, (b) PVD TiN/MOCVD HfO$_2$, (c) PVD TiN/ALD HfO$_2$, (d) CVD TiN/ALD HfO$_2$ compared to (a) p+poly/SiON device.

**Fig. 8** Plot of effective hole mobility versus inversion carrier density. The mobility data and legends are same as in Fig. 7.

**Fig. 9** Effective electron mobility for TaSiN/MOCVD HfO$_2$ dual-metal gate n-MOSFETs compared to poly/SiON device.

**Fig. 10** Plot of effective electron mobility versus inversion carrier density for different gate stacks as shown.
Constant gate voltage stressing (CETinv=19.4Å, Vg=2V:~10MV/cm) of TaSiN/ALD HfO2 n-MOSFETs causes a <40 mV variation in Vt and ~1% decrease in peak Gm after 1000s stressing (Fig. 11). In CVD TiN/ALD HfO2 p-MOSFETs similar gate voltage stressing (CETinv=23.5Å, Vg=-2.4V:~10MV/cm) causes a <30 mV variation in Vt and ~15% decrease in peak Gm after 1000s stress. There is negligible change in CV and stress-induced leakage current (SILC) characteristics (not shown) in both n- and p-MOSFETs after the 1000s stress in the cases above. MOCVD HfO2 dual-metal gate n- and p-MOSFETs behave very similarly. The charge trapping behavior in dual-metal gate n- and p-MOSFETs is comparable to single metal gate devices confirming that the dual-metal integration does not degrade the dielectric properties. Fig. 13 shows the first time dependent dielectric break-down (TDDB) data for dual-metal gate MOSFETs on MOCVD HfO2 compared to poly/SiON data. The data are quite encouraging.

Summary

A novel dual-metal gate CMOS integration with HfO2 gate dielectric is reported. The integration maintains the gate leakage, mobility or charge trapping behavior compared to single metal gate devices. Measurements of dielectric lifetimes in dual-metal-gated devices with HfO2 are encouraging.

References