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A 4-Mb Toggle MRAM Based on a Novel Bit and Switching Method

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***Abstract*—A 4-Mb magnetoresistive random access memory (MRAM) with a novel magnetic bit cell and toggle switching mode is presented. The circuit was designed in a five level metal, 0.18-μm complementary metal–oxide–semiconductor process with a bit cell size of 1.55 μm^2. The new bit cell uses a balanced synthetic antiferromagnetic free layer and a phased write pulse sequence to provide robust switching performance with immunity from half-select disturbs. This switching mode greatly improves the operational performance of the MRAM as compared to conventional MRAM. A detailed description of this 4-Mb toggle MRAM is presented.**

***Index Terms*—Magnetic film memories, magnetic tunnel junction, magnetoresistive device, magnetoresistive random access memory (MRAM), micromagnetic switching, MRAM integration, random access memories (RAMs).**

I. Introduction

MAGNETORESISTIVE random access memory (MRAM) combines a magnetic device with standard silicon-based microelectronics to obtain the combined attributes of nonvolatility, high-speed operation, and unlimited read and write endurance not found in any other existing memory technology. In this paper, we present details of a new, fully functional 4-Mb MRAM chip shown in Fig. 1 that employs a novel bit structure and approach for operation. The memory is based on a 1-transistor, 1-magnetic tunnel junction (1T1MTJ) memory cell created with a 0.18-μm complementary metal–oxide–semiconductor (CMOS) dual gate process using five levels of metal and with program current lines clad with highly permeable material for magnetic flux concentration [1]. We introduce a new cell architecture, bit structure, and switching mode which are combined to provide significantly improved operational performance and manufacturability as compared to the conventional MRAM discussed previously [2].

II. 4-Mb Memory Cell and Process Integration

The 4-Mb memory cell is composed of a thin oxide pass transistor, a single MTJ, top and bottom sense electrodes, and two orthogonal program lines, as shown in Fig. 2.

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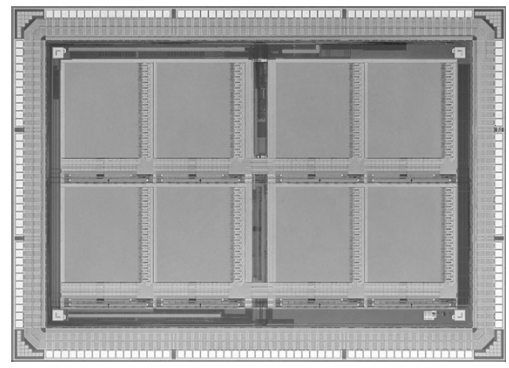

Fig. 1. Photograph of the 4-Mb MRAM. The configuration is 256 K × 16 bits built in 0.18-μm CMOS technology.

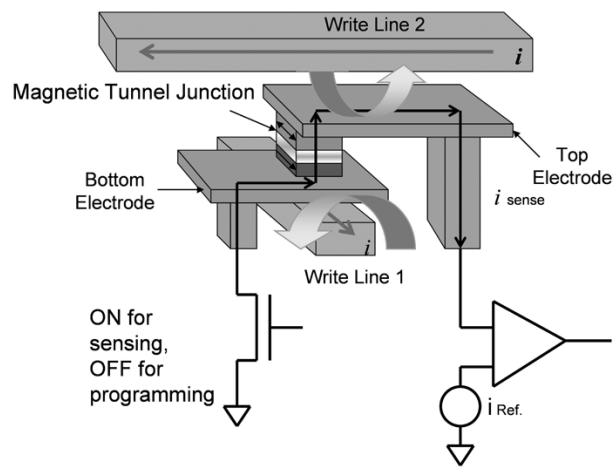

Fig. 2. MRAM bit cell structure, showing the sense path and programming lines.

A connection is made from the base contact of the bit to ground through a via stack connected to an isolation transistor in the underlying CMOS. Flowing current through the program conductors produces the magnetic fields necessary to switch the state of the bit. In this architecture, the program lines are physically separated from the MTJ, which reduces the parasitic delay. The MTJ is composed of a pinned magnetic layer, a tunnel barrier, and a free magnetic layer. Electrons spin polarized by the magnetic layers traverse the tunnel barrier. A parallel alignment of the free layer with respect to the pinned layer results in a low resistance state, while an antiparallel alignment results in a high resistance state [2]. The sense circuitry is composed of a thin oxide pass transistor, which is electrically connected to the MTJ by the bottom and top electrode conductors. In order to read the

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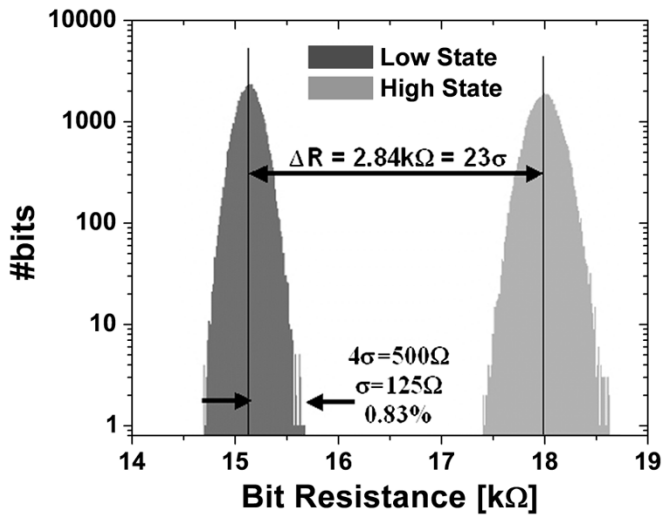

Fig. 3. Low and high state resistance distributions measured at operating bias and with series transistor resistance. Data are from a 64-Kb sample of a 4-Mb device showing 23-sigma separation.

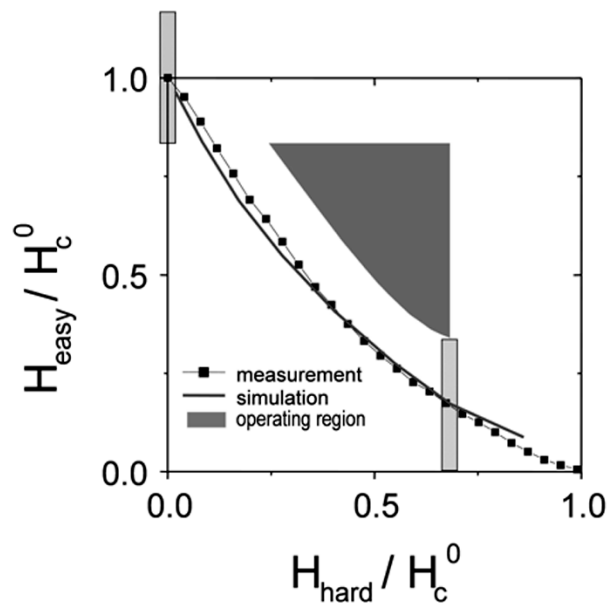

Fig. 4. Schematic representation of "conventional" MRAM operating region for switching.

bit, the isolation transistor is turned on, and a small current of about 10 μA (depending on the resistance of the material, size of the bit, and desired bias condition) is passed through the bit to sense the resistance. The within-die read distributions of the 4-Mb circuit are extremely narrow, with more than 20-sigma separation between the means of the high- and low-resistance state distributions as shown in Fig. 3. This should be compared to the minimum 12-sigma required to read a multimegabit array with an ideal midpoint reference, providing ample margin in the actual 4-Mb circuit. The MRAM module is inserted late in the CMOS process flow, making the MRAM module and the CMOS independent from one another.

III. Bit Switching

A. "Conventional" MRAM

In "conventional" MRAM, information is stored by selectively switching the magnetic moment direction of the free layer of individual bits. The bit state is programmed to a "1" or "0" depending on the polarity of the current that generates the magnetic field along the bit's easy axis (bit line). All other bits are exposed only to fields from a single line (half-selected bits), or no lines. Due to process and material variations, an array of memory cells has a distribution of switching fields with a deviation $\sigma_{\rm sw}$. Therefore, to program all the bits in a large array with the same current, the applied field needs to be larger than the mean "selected" switching field by greater than $6\sigma_{\rm sw}$. In addition, the applied field must be kept below a maximum value, or the state of the half-selected bits along the lines, but outside the intersection, may be disturbed during programming. Thus, for error-free programming, "conventional" MRAM must keep these two distributions well-separated. As a result, there is an operating window for programming fields; inside this window, all the bits can be programmed without errors or disturbs. A schematic of the operating window superposed on the switching astroid is shown in Fig. 4. The requirement of maintaining sufficient separation of two distinct distributions is one of the main challenges facing manufacturing of the conventional MRAM approach.

B. New "Toggling" Approach to MRAM Switching

We present here a new approach to bit programming that effectively eliminates the half-select disturb phenomenon present in conventional MRAM. Through the use of a new free layer structure, bit orientation and current pulse sequence, the MRAM bit state can be programmed via a "toggling" mode we have named "Savtchenko switching" after its late inventor [3]. The selectivity using this mode is greatly enhanced because a single current line pulse alone cannot switch the bit. This unique behavior results in a wide operating region with a threshold onset for switching.

Savtchenko switching relies on the unique behavior of a synthetic antiferromagnet (SAF) free layer that is formed from two ferromagnetic layers separated by a nonmagnetic coupling spacer layer. This is shown schematically in Fig. 5. The moment-balanced SAF free-layer responds to an applied magnetic field differently than the single ferromagnetic layer of conventional MRAM. For a synthetic antiferromagnet having some net anisotropy H_k in each layer, there exists a critical spin flop field $H_{\rm sw}$ at which the two antiparallel layer magnetizations will rotate (flop) to be orthogonal to the applied field H with each layer scissoring slightly in the direction of H [4]. For fields $H \geq H_{\rm sw}$, the SAF can lower its total magnetic energy by decreasing its dipole energy with a flop and scissor, even though the antiferromagnetic exchange energy is increased by the same scissoring. To derive $H_{\rm sw}$ for the case where H is parallel to H_k, we first derive an expression for the flop energy created by the applied field in the absence of H_k.

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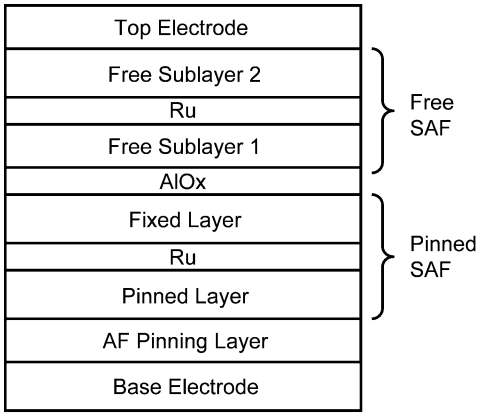

Fig. 5. Bit cell material stack showing the synthetic antiferromagnetic free layer.

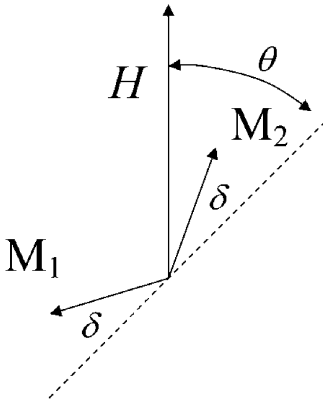

Fig. 6. Schematic of the magnetic moment vectors in a synthetic antiferromagnet. The dashed line is the antiparallel (AP) axis, θ is the angle of the applied field with respect to the AP axis, and δ is the deviation angle between the magnetizations of each layer and the AP axis. For simplicity, $M_1 = M_2$.

In Fig. 6, we consider an SAF with magnetizations M_s in a field H and no H_k. The energy for the system may be written as

$$E(\theta) = -K_s \cos(2\delta) - 2M_s H \sin(\theta)\sin(\delta) \tag{1}$$

where K_s is the strength of the antiferromagnetic exchange anisotropy between the two layers. Minimizing with respect to δ, we can solve for $\sin(\delta)$ in terms of θ and enter it back in to the expression for $E(\theta)$ which results in

$$E(\theta) = -\frac{M_s^2 H^2}{2K_s}\sin^2(\theta) + C \tag{2}$$

where C is a constant term independent of θ. Thus, the flop energy can be expressed as a field-dependent anisotropy orthogonal to H. It is this effective orthogonal anisotropy that provides stabilization against disturb of the half-selected bits, giving the increased selectivity. Returning to the case where H is parallel to a finite H_k, we add the anisotropies resulting in

$$E(\theta) = M_s H_k \left(1 - \frac{H^2}{H_k H_{\text{sat}}}\right)\sin^2(\theta) \tag{3}$$

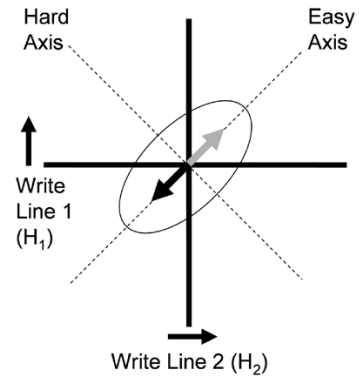

Fig. 7. Schematic of 45° orientation of the bit with respect to the programming current lines.

where we have defined the saturation field of the SAF as $H_{\text{sat}} = 2K_s/M_s$. Thus, the critical flop field and hence the toggle field is

$$H_{\text{sw}} = (H_k H_{\text{sat}})^{\frac{1}{2}}. \tag{4}$$

To use this phenomenon, the bit is patterned with its magnetic easy axis oriented 45° with respect to the programming current lines. This is depicted in Fig. 7.

The programming pulse sequence and resulting magnetic behavior are depicted in Fig. 8. The arrows represent the magnetic moment of the two sublayers in the SAF free layer. In this example, the darker arrow is the layer that is adjacent to the tunnel barrier and is therefore the information storage layer that determines the resistance. To toggle the bit from an initial "0" to a final "1," the currents I_1 and I_2 are pulsed with a phase relationship such that I_2 follows I_1. The effect of this phasing can be seen in the time evolution in the figure. At time t_1, only I_1 is flowing and the magnetic field H_1 is applied 45° to the bit 8 easy axis. The SAF responds by orienting nominally orthogonal to this field. At t_2, I_2 is turned on and field H_2 adds to H_1 providing a resultant field at 45° which is along the bit easy axis. It is the magnitude of these combined fields that must be sufficient to overcome the bit's switching (flop) field. At t_3, I_1 is turned off and the only applied field is H_2. It can be seen at this point that the darker arrow is very close to the easy axis, but pointing nearly in the opposite direction to its initial state. Finally at t_4, I_2 is turned off and the bit moment relaxes to its easy axis with the darker arrow pointing 180° from its initial state. Hence, the bit has been switched from "0" to "1." It should be clear that this is a toggling process as a result of the close balance of the sublayer magnetic moments. Due to symmetry, if the process is repeated with the *same* polarity pulses, the bit will reverse again in the same manner. The memory operates with a decision write scheme, where the bit state is read first and only toggled if the new data differs from the existing data. This approach has benefits in limiting the overall power consumption and the unipolar current allows the use of smaller transistors, thereby improving array efficiency.

It should also be noted that if only a single line current is applied (half-selected bits) as in t_1, the 45° field angle cannot switch the state. In fact, the single-line field raises the switching energy barrier of those bits, so that they are stabilized against

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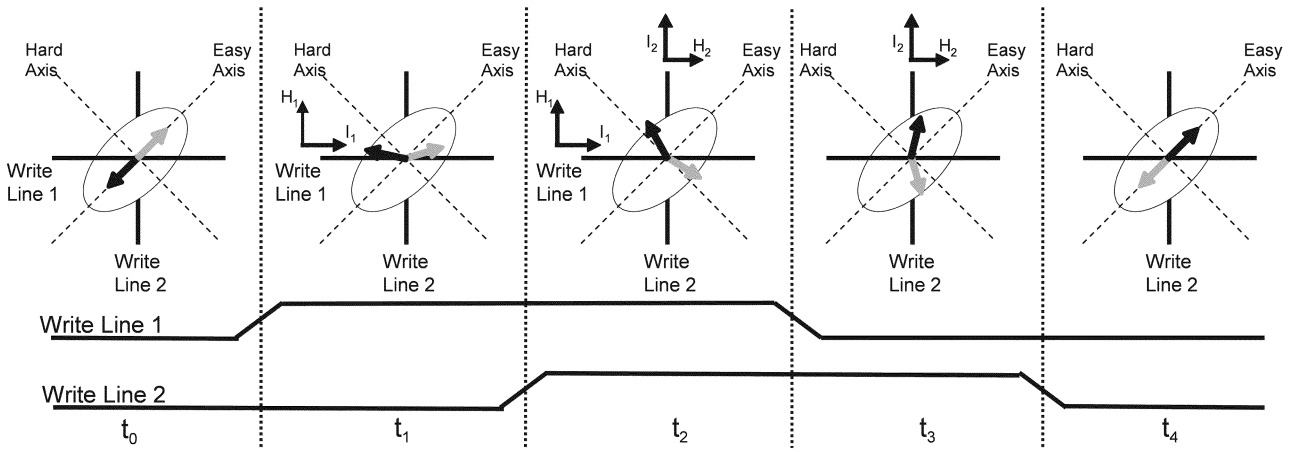

Fig. 8. Schematic of the toggling operation of Savtchenko switching. Pulses are applied in a sequence designed to rotate the SAF 180° to the opposite resistance state.

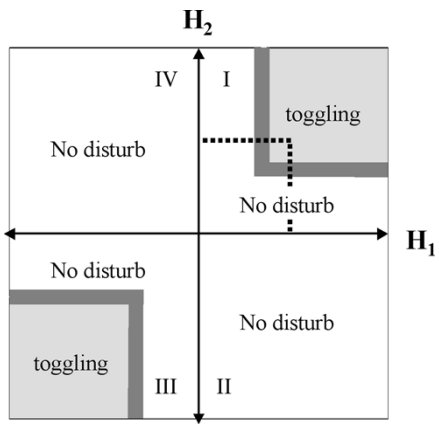

Fig. 9. Switching characteristic map of Savtchenko switching showing two regions of toggling for like polarity pulses. Regions of bit-to-bit toggling distribution are indicated as dark bars at the toggling boundary.

reversal during the field pulse. This is in marked contrast to the conventional approach, where all of the half-selected bits have their switching energy reduced and are therefore more susceptible to disturbance. The phase relationship of the pulses is therefore required for switching resulting in significantly improved bit selectivity in an array.

A schematic of the resulting switching response curve for an array of MRAM bits is shown in Fig. 9. The upper right and lower left quadrants are for like polarity field pulses that will allow toggling. The white regions are insufficient field magnitudes or improper field directions to achieve toggling and, therefore, do not disturb the bits. The light gray regions are above the toggling transition for all bits and result in 100% toggling. The darker gray regions represent the bit-to-bit distribution of switching thresholds that must be overcome for reliable switching of all bits in an array.

Fig. 10 is a quasi-static measurement of the switching characteristic map of a single bit. The fields were applied with an external magnet in the angles and phased sequence described above and the resistance was monitored to determine a switch. Toggling begins at ∼40 Oe for each axis and continues to 300 Oe where the measurement was stopped. Note that below the toggling transition, there are no disturbs all the way up to the highest fields, displaying the remarkable half-select robustness of this approach.

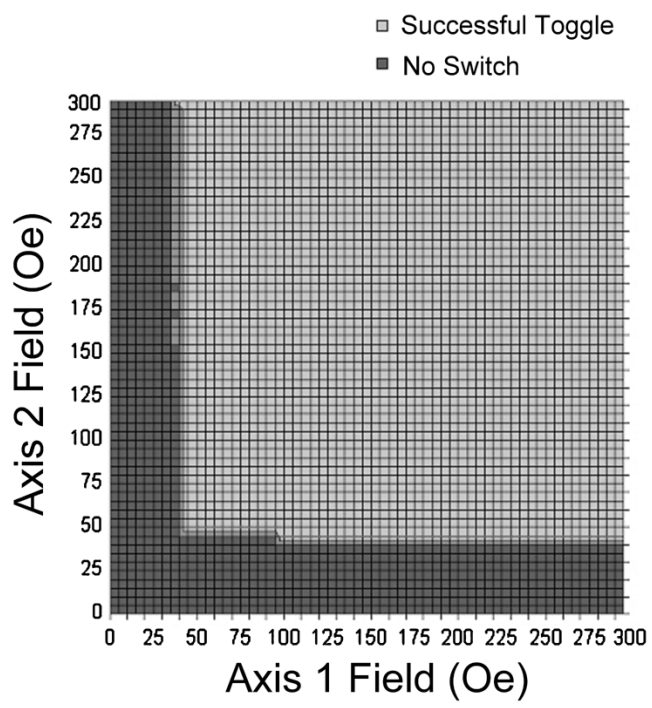

Fig. 10. Measured quasi-static toggling characteristic map of a single $0.6 \times 0.9\ \mu m^2$ bit. No single-axis disturbs were observed to 300 Oe.

IV. 4-Mb Memory Operation

The toggle MRAM presented here uses a "decision" write scheme where the state of the bit is first determined at the start of the write cycle. The existing state is then compared to the desired state and the programming current is enabled only if the two states differ.

Fig. 11 is a switching characteristic map versus current for an entire 4-Mb memory. The test pattern was a checkerboard/inverse checkerboard of alternating "1" and "0" that was written at each current and read back to verify. In the region below the switching threshold, no bits changed state and hence there were

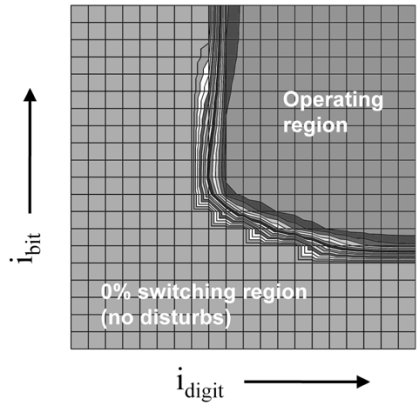

Fig. 11. Switching map of an entire 4-Mb die showing the large operating region. A checkerboard/inverse checkerboard pattern of alternating "1" and "0" was written with 10-ns pulses at each current and read back to verify.

no disturbs from half selects. A large operating region is observed above the threshold consistent with the single bit characteristic presented above. The contours in the transition region just at the threshold are a measure of the bit-to-bit switching distribution.

V. Summary

In this paper, we have presented a novel MRAM bit cell and programming method that solves the half-select and write window limitations of the conventional astroid-based approach. This new approach has enabled our successful demonstration of 4-Mb MRAM based on a 0.18-μm CMOS. The robustness of this switching mode provides the necessary margin for successful manufacturing of MRAM technology for present and future generations.

Acknowledgment

This paper is dedicated to the late Leonid Savtchenko.

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