CVD TiSiN Diffusion Barrier Integration in Sub-130 nm Technology Nodes

Chris Prindle¹, Bill Brennan², Dean Denning¹, Iraj Shahvandi¹, Srinivas Guggilla³, Ling Chen³, Christophe Marcadal³, Dan Deyo⁴, Umesh Bhandary³

¹Motorola Inc., Austin, Texas
²Advanced Micro Devices Inc., Austin, Texas
³Applied Materials Inc., Santa Clara, California
⁴Applied Materials Inc., Austin, Texas

Motorola Inc., Semiconductor Products Sector, Digital DNA™ Laboratory, Dan Noble Center, Advanced Products Research and Development Laboratory, 3501 Ed Bluestein Boulevard, Austin, Texas 78721
(512) 933-3491, FAX (512) 933-6438, christopher.prindle@motorola.com

Abstract

Metalorganic chemical vapor deposition (MOCVD) titanium silicon nitride (TiSiN) has emerged as a strong candidate for a next-generation diffusion barrier material in copper/low-k dielectric back-end-of-line (BEOL) device fabrication. As ionized physical vapor deposition (PVD) Ta(N) barriers currently used in high-volume production begin to exhibit marginal film continuity in high aspect ratio device features, more conformal barrier materials become a requirement. Material, electrical, and reliability properties are strongly influenced by CVD TiSiN film thickness, process sequencing, and incoming surface cleanliness of device features. TiSiN has been shown to possess the necessary material and electrical properties to be successfully integrated in sub-130 nm copper/low-k semiconductor device technology nodes.

Introduction

Copper/low-k dielectric BEOL integration schemes have replaced aluminum/SiO₂ in an ongoing effort to minimize resistance and capacitance in on-chip interconnections for high performance integrated circuits. The 2001 International Technology Roadmap for Semiconductors states that beyond the current 130 nm technology node, diffusion barrier thickness requirements for copper wiring are anticipated to be less than 140 Å (1). Tantalum-based ionized PVD diffusion barriers used across the semiconductor industry may begin to show marginality and lead to device failures as interconnect feature sizes continue to scale down with each new technology generation. More conformal barriers will become necessary for adequate step coverage in high aspect ratio vias and trenches. Extensive work has been done in developing novel barrier materials and associated deposition modes to address the conformality requirements in aggressive device features (2, 3, 4). CVD barrier materials have emerged as viable technology solutions, with TiSiN showing particular commercial promise.

CVD TiSiN is an extension of the commercially available CVD TiN processes used in W plug/Al wiring technologies (5, 6). The TiSiN film is created by exposing in situ the TiN surface to silane (SiH₄), which leads to Si-N bond formation in the TiSiN film. This process results in a diffusion barrier film with conformal step coverage and low electrical resistance (7).

As a novel barrier material, CVD TiSiN introduces new interfaces that can pose possible electrical reliability concerns. Other important BEOL integration considerations include adhesion of the diffusion barrier to patterned dielectric materials, as well as PVD copper seed layer adhesion to the diffusion barrier. This work demonstrates the excellent device feature step coverage capability, Cu wettability, and uniform properties of CVD TiSiN in 130 nm BEOL technology node features, in addition to electrical performance equivalent to and exceeding that achieved with PVD Ta(N) barriers.

Experiment

The TiSiN barrier film was deposited in a 200 mm single wafer CVD chamber on a multi-reactor cluster tool with integrated degas, RF sputter etch, PVD Ta(N) barrier, and PVD Cu seed chambers. CVD TiSiN films are formed by thermal decomposition of tetrakis-dimethyl-amino-titanium (TDMAT) precursor at a substrate temperature of approximately 350°C. A thin TiNₓ(Cₓ) deposition is followed by a H⁺/N⁺ plasma treatment to produce TiN. These thermal deposition and plasma treatment sequences are repeated until the desired film thickness is achieved. The final TiN film thickness is exposed in situ to silane to create the Si-passivated TiN film, or TiSiN.

Ti[N(CH₃)₂]₄ → TiN(C) + HN(CH₃)₂ + H₂N(CH₃) + hydrocarbons

TiN(C) + SiH₄ → TiSiN

TiSiN step coverage in device features was imaged using high-resolution transmission electron microscopy (TEM) cross-sections. PVD Cu seed layer wettability on blanket TiSiN was tested using scanning electron microscopy (SEM) following 400°C 15 minute vacuum anneal, and blanket TiSiN surface roughness was measured using atomic force microscopy.
microscopy (AFM). CVD TiSiN film composition and interfacial contamination were analyzed using x-ray photoelectron spectroscopy (XPS) and time of flight secondary ion mass spectrometry (TOF-SIMS), and the interfacial adhesion strength between TiSiN/dielectric and PVD Cu/TiSiN was measured using a four-point bend test. In addition, the electrical parametrics of integrated TiSiN film (thicknesses and precleans) in sub-130 nm node device features were tested using inline electrical probe.

Results and Discussion

Fig. 1 shows a cross-sectional TEM of CVD TiSiN integrated with PVD Cu seed layer followed by Cu electroplate fill, anneal, and chemical mechanical polish in a 130 nm node via. TiSiN deposits as a conformal and continuous film within the via, with 100% sidewall and 75% bottom step coverage.

Fig. 2 (a) and (b) show TEM energy dispersive x-ray (EDX) maps for Cu and Ti, respectively, at the metal/via interface in a 130 nm node device stack, confirming the conformity and continuity of TiSiN in the via. Fig. 3 shows a high resolution TEM of (a) non-plasma treated region displaying amorphous TiSiN on the via sidewall, and (b) plasma treated nano-crystalline TiSiN on the via bottom and field areas. These crystallinity results have also been confirmed by x-ray diffraction (XRD), indicating very small grains close to the amorphous structure formed by a mixture of TiN and Si-N. This TiSiN material structure is preferred for good Cu barrier performance, with the amorphous phase on sidewall serving as a good barrier to Cu diffusion, and the nano-crystalline phase at via bottom promoting low via resistance (7).

The depth profile elemental composition of the TiSiN film measured by XPS is shown in Fig. 4. There is no evidence of Si diffusion through the TiSiN and Cu films at various sites across the wafer as determined by both depth profile and intensity plots. Both the XPS and TOF-SIMS analysis indicate that Cu is detected through the barrier; however, this is thought to be an artifact of the analytical sputtering technique. Studies are underway to quantify the “true” copper diffusion through the barrier(s).
AFM-measured surface roughness of the as-deposited TiSiN and stacked with PVD Cu produced RMS roughness values of 0.45 nm and 0.44 nm, respectively. Similar roughness values were obtained with PVD Ta(N) barrier materials and PVD Cu film stacks. Four-point bend adhesion test data indicates that the adhesion of CVD TiSiN to oxide dielectrics was very good, while TiSiN adhesion to low-k and ultra-low k dielectric materials was less than that on oxide. The same adhesion strength trend was observed for conventional PVD Ta(N) barrier materials. A Cu dewetting test, in which 100Å PVD Cu seed layer was deposited on the barrier film and annealed at 380°C for 15 minutes, showed good Cu wettability on TiSiN and PVD Ta, whereas Cu did not wet well on PVD TaN.

Fig. 5 shows BEOL electrical probe data comparing the integration of various TiSiN thickness sequences to PVD Ta(N) barrier integration. The electrical data indicate via resistance is lower for thinner CVD TiSiN barrier films; leakage and other parameters were not adversely affected by this experiment. Fig. 6 displays additional electrical probe data comparing integrated TiSiN and conventional PVD Ta(N) diffusion barrier processes with different precleans prior to barrier deposition. The data shows a significant improvement in TiSiN via chain yield with preclean B, as compared to poor yield observed with preclean A. However, preclean A coupled with PVD Ta(N) produces good via chain yield. The surface condition of device features prior to barrier deposition therefore appears to be critical for successful TiSiN integration, and may require optimization of preclean processing for reliable device fabrication. Further materials characterization of Cu texture, thermal stability, and reliability of TiSiN in low-k dielectric (k < 2.8) integration schemes is in progress.

**Conclusion**

CVD TiSiN material properties including film continuity, step coverage conformality, surface roughness, and thermal stability have been demonstrated using a commercially available TiSiN barrier. The electrical via resistance thickness dependence on 130 nm structures has been shown, with thinner TiSiN films producing lower via resistance. The incoming surface condition of device features dictated by preclean appears to be critical for the successful integration of TiSiN. This work shows that CVD TiSiN can successfully replace PVD Ta(N) diffusion barrier films in Cu/low-k interconnect schemes, with particular promise for extendibility to 100 nm semiconductor technology nodes and beyond.

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