A Functional 0.69µm² Embedded 6T-SRAM bit cell for 65nm CMOS platform


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Abstract
This work highlights a 65nm CMOS technology platform for low power and general-purpose applications. A 6-T SRAM bit cell size of 0.69µm² with a 45nm gate length is demonstrated. Electrical data of functional SRAM bit-cell is presented at Vd=0.9Volt using a conventional nitrided gate oxide dielectric. A comparison between offset spacer and PLAsma Doping (PLAD) is made for the transistor characteristics with very promising Vth-Ld and Vth-Wd profiles measured. Lithography employed a combination of both optical lithography and e-beam imaging. The BEOL integration used a conventional low K dielectric with copper metallization.

Introduction
With the arrival of 300nm manufacturing factories, it becomes increasingly important to develop CMOS process technologies that scales efficiently for each developed technology node. This 65nm proposal designed with the thought of addressing long term manufacturing concerns, supporting both low power and general-purpose applications (Table 2). In the absence of commercially available 193nm high NA tools, a combination of optical lithography and e-beam lithography was employed to pattern the individual layers. Table 1 supplies the major 65nm design rules. This allowed the technology development to completely evaluate the transistor behavior, SRAM cell characterization and standard cells library impact. Many papers described a single 45nm transistor behavior [1], but this work presents for the first time fully integrates a full 65nm platform with SRAM characterization and hot-carrier reliability data.

Experimental
In addressing scaling issues, the STI trench depth was set a 3KA with a poly thickness of 1.2KA. A conventional oxy-nitride film stack [2] was used and determined to address both EOT concerns and gate leakage. In the transistor architecture, we focused the study on Source-Drain Extension (SDE) design. A comparison of conventional BF3-off-set spacers solution with respect to the PLAD technique [3] is made to improve the Vth-Ld profile (see Table 3). CoSi was used in conjunction with the industry standard low K dielectric for the BEOL processing. Conventional 90nm processing techniques successfully were able to support the fabrication of the 65nm BEOL layers.

Transistor results
Figure 1 supplies the rectangular 0.69µm² 6T-SRAM bit cell layout including very aggressive rules such as a poly to contact distance of 50nm. We have successfully mixed ebeam imaging with conventional 193nm optical lithography to print a complete 4Mbit SRAM array. Figures 2 show a series of SEM top-view pictures from active patterning up to copper metallisation. An impressive similarity between the designed layout and the silicon is found. An accurate TEM cross-section of 45nm gate is printed in figure 3, demonstrating off-set spacer integration with 1.2nm gate oxide and salicidation. Total spacer width is ~40nm. It is worth pointing out that Lsilicon=Loffset – 25nm. On figure 4, we plotted the Vth-Ld profile with respect to the SDE architecture for both Nmos and Pmos transistors. As expected, for N-channel device, the off-set spacers removal in Process C resulted in a significant increase of Vth roll off. In case of Pmos transistor, we show no difference between both off-set spacers/ BF3 and no off-set/PLAD solutions. Best channel control is obtained with the Process B which includes both off-set spacers and PLAD technic. The consequences are found on both sub-threshold slope and D.I.B.L. plots. As plotted by figure 5, a good P-channel control at Vg=0.9V required both off-set spacers and PLAD option (called Process B), which correspond to a 25nm junction depth. Figure 6 describes the Ith-Vth characteristic in case of Process B. Useful sub-threshold regime is found with a D.I.B.L. lower than 150mV. Output MOS characteristics (figure 7) of Process B supplies a favourable drive current at Vg=0.9V, close to 600µA/µm for Nmos and 260µA/µm for Pmos for Lsilicon = 45nm.

Reliability results
Figure 12 plots the hot carrier DC-drift time for an Nmos transistor using Process B including both Lsilicon=45nm and EOT=1.2nm. This graph exhibits the time evolution of normalized bulk current for the main device parameters: Ion, β and Vp. Independent of the measured parameters, the HCI data satisfies the 10 year lifetime requirement.

Conclusions
We have developed a 65nm CMOS technology platform that enables e-beam and optical lithography to support both low power and general purpose applications. A 0.69µm² 6T-cell SRAM is demonstrated with functional bit-cells and reliable transistors. The present cell layout is scalable towards cell sizes of 0.6µm² upon further process enhancement. A set of transistor targets and 65nm design rules is foundry compatible and enables competitive use in 3rd party IP applications. Standard cell gate densities higher than 780kgs/mm² have been proposed with this platform.

References
**Table 1:** 65nm design rules.

**Table 2:** Transistors target for 65nm platform.

**Table 3:** Process flow description.