Migrating PowerQUICC® III Processors to QorIQ™ Platforms

Jeff Logan  Network Processor Division
Freescale – Leader in Embedded Processors

Best performance at a given power for embedded & infrastructure solutions

► Continued innovation in hardware architectures
  • QorIQ™: Broadest scalable family of processors in the market
    o Evolution from PowerQUICC® family
    o Dual core @ 800 MHz at < 5 Watts
    o Eight cores @ 1.5 GHz/core at 30 Watts
  • StarCore® DSP solutions
    o Up to 1.0GHz in 3-6 core configurations with advanced accelerators
  • Industry leading integration and Communication Engines

► Increasing software investment
  • Optimized Multicore Solutions
  • Hybrid software simulation environment and debug tools
    o Production ready software with VortiQa solutions
  • Fast time to market
    o Simplified migration to multicore architecture
    o More flexibility to create a uniquely differentiated product

► 45nm high-performance technology in production

Service Provider
Enterprise
Consumer Access
Industrial and Aerospace

4-6 Core DSP
MSC8144 DSP MSC8154
MSC8156 DSP

2-8 Core CPU
QorIQ™ P4080
PowerQUICC MPC8572

1-2 Core CPU
QorIQ P2020
PowerQUICC MPC837x
Why We Win…

► Large market presence (>50% SOM)
► Broad spectrum of performance and power offerings
► Energy Efficiency
► Consistent and scalable architecture
► Instructions per clock => RISC architecture 7 stage pipeline, out of order transactions, branch predictions 2.5 MIPS/Mhz
► Highly integrated
► Safe and Secure Computing
► Product Longevity
► Serial to Ethernet convergence and we’ve got Ethernet…..
► Broad ecosystem and tools
Application space for Power Architecture

Medical
- Imaging
- Control/security
- Multi-core
- Trusted Arch
- Networked

Aerospace & Defense
- Signal processing
- Control
- Trusted Architecture
- Multi-core
- Networked

Robotics
- Floating Point/Imaging
- Control /Security
- Trusted Arch
- Networked

Printing and Imaging
- Image Acceleration
- Networking

Video Surveillance
- Analytics – real time interpretation of Pixel movement
- Audio codec’s
- Image Acceleration
- Trusted Arch
- Networked

Networking /Telecom
- L2 Scheduling
- Encryption
- Public Key Crypto
- Trusted Architecture
- Multi-core
• **Flattening of the Network** – Consolidation of services into fewer integrated devices, Increased sustained bandwidth and processing rates. Content delivery and Security mgmt moving to Access network.

• **Moore’s law challenged** – Higher Performance with power constraint. Advent of Multi-core and application specific acceleration, along with required software support.

► Frequency scaling of CPU cores no longer valid due to power constraints

► **Multicore processors** viewed as the most viable approach to achieve required performance gains within power budgets
Agenda

► Multi-processing Use Cases

► PowerQUICC III: MPC8548 & MPC8572

► QorIQ™ 45nm Families

► PowerQUICC III Comparison to QorIQ™ Platforms
  • Software considerations
  • Power supply voltages
  • Frequency & clock ratios

► Migration Scenarios

► Altivec Re-introduction

► Single Board Computing

► RTOS/OS Strategy

► Back Up: QorIQ™ P1000 and P2000 Block Descriptions
**Multiprocessing Use Case**

**SMP**
- Core0
- Core1
- Scaled control plane
- SW transparent
- OS manages entire chip

**Partitioning**
- Core0
- Core1
- Typically AMP
- Control + data plane
- Legacy OS + services on Linux
- Combining two processors

**Offloading**
- Core0
- Core1
- CPU intensive activity on one core
- Security
- Deep packet inspection

**Standby**
- Core0
- Core1
- Redundancy
- Quick in-field SW upgrade
- Future in-field performance upgrade
Many Choices

- **Multicore application differentiators**
  - Frequency
  - IPC
  - Number of cores
    - Threading
  - Cache size and structure
  - HW Acceleration

- **Other differentiators**
  - Power
  - I/O
  - Price
  - Package size
  - ISA
What Application for What Multicore?

- **Control Plane**: 1 - 2
- **Mixed**: 2 - 4
- **Data Plane**: 4+

Potential for acceleration

Number of Cores

Code Footprint
Multiprocessing Configurations

► Symmetric Multiprocessing
- Homogenous OS support
- High-performance option
- Software transparency
- Cores share address space for OS and data
- Resource sharing handled by OS
- Dynamic load balancing by OS

► Asymmetric Multiprocessing
- Heterogeneous OS support
- Two separate OS or two copies of one non-SMP OS
- Collapse two processors into one
- Task offload or division of labor
- Operating systems, data reside in different address spaces
- Resource sharing handled by user
- Static load balancing

► Cooperative AMP
- Application-level awareness between cores
The OS kernel resides at physical memory address 0, addressable by both cores.

The MMU relocates applications and shared memory appropriately.
Asymmetric MP Memory Organization

- Each OS kernel expects to control physical memory beginning at address 0
- Each wants its own interrupt vectors
- The MMU can relocate applications and shared memory appropriately

Diagram:

- Core 0
  - OS "A"
  - Apps "A"
  - Shared memory

- Core 1
  - OS "B"
  - Apps "B"
  - Shared memory

- OS "A"
- Apps "A"
- OS "B"
- Apps "B"
Resource Allocation

► SMP
- Both Core can see all peripherals. Imaginary separation can be made by OS/Software.

► AMP/CAMP
- Each resources are dedicated to designated core. Statically assigned.
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  - Software considerations
  - Power supply voltages
  - Frequency & clock ratios
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- RTOS/OS Strategy
- Back Up: QorIQ™ P1000 and P2000 Block Descriptions
MPC8548/E Block Diagram and Features

► e500 core (1.0-1.5GHz)
  • 512KB L2 Cache w/ ECC
  • 36bit physical addressing
  • Double Precision Floating Point

► System unit
  • 64b DDR/DDR2 up to 533MHz data rate w/ECC
  • 4x 10/100/1000 Ethernet Controllers w/Checksum Offload, QoS, and 8/16b FIFO-mode (up to 3.2Gbps)
  • 2x 32b-PCI or 1x 64b-PCI(X)
  • DUART, 2x I2C, Timers
  • Integrated Security Engine (up to 1Gbps)
    • Support for Kasumi algorithm

► High-speed interfaces
  • x4,x1 Serial RapidIO (20Gbps)
  • Or x8,x4,x2,x1 PCI-Express (32Gbps)
  • Or x4 Serial RapidIO and x4 PCI-Express (36Gbps)

► Local Bus - (3.3V I/O)
  • 32-bit for SDRAM/Boot Flash/Compact Flash

Production: Now
Package: 783 FCPBGA
Dual e500 core, built on Power Architecture® technology (up to 1.5 GHz)
- 36-bit addressing
- 1 MB shared L2 cache/SRAM with ECC
  - With stashing

Dual memory controller
- Dual DDR2/3 SDRAM up to 800 MHz
- 32/64-bit data bus with ECC
- Support for up to 32 GB memory

High-speed interconnect
- One x8/x4/x2/x1 PCIe
- Two x4/x2/x1 PCIe
- One x4/x2/x1 PCIe AND Two x2/x1 PCIe
- One x4/x2/x1 PCIe AND x4/x1 sRapidIO

Ethernet
- 4x 10/100/1000 Ethernet controllers with classification/policing, 8 Rx/Tx queues, checksum offload, QoS, lossless flow control, IEEE® 1588, 4 SGMII
- 1x 10/100 FEC with MII (muxed)

Security engine (SEC 3.0)
- ARC4, 3DES, AES, AES-GCM, SHA-384/512, RSA/ECG, RNG and XOR
- Single pass SSL

Pattern matching (Reg-Ex) and deflate
- 16k patterns up to 128, breaking across packets

Table lookup unit (TLU)
- Up to 7M lookups/sec

90 nm SOI process, 1023 pin package

Frequency, voltage, power (typical)

<table>
<thead>
<tr>
<th>VDD</th>
<th>Core Freq</th>
<th>Plat Freq</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1V</td>
<td>1500</td>
<td>600</td>
<td>17.3W</td>
</tr>
<tr>
<td>1.1V</td>
<td>1333</td>
<td>533</td>
<td>16.3W</td>
</tr>
<tr>
<td>1.1V</td>
<td>1200</td>
<td>400</td>
<td>15.6W</td>
</tr>
</tbody>
</table>
L2 Cache Controller

► Shared 1024kB unified frontside L2 cache w/8-way associativity (Each way: 64KB)

► Assignment Granularity:
  • One, two, four, or all eight “ways” of the cache can be assigned as the following:
  • SRAM
  • Stash-Only
  • CPU0 L2 Only
  • CPU1 L2 Only
  • Both CPU0 & CPU1 L2

► Stash-Only regions can now be defined
  • Prevents stash data from polluting processor data and vice-versa
  • One, two or four “ways” of the cache can be dedicated as stash-only

► Stash Allocate Disable mode added
  • Allows update of all resident cache lines without allocation of new lines
Agenda

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► QorIQ™ 45nm Families

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  • Software considerations
  • Power supply voltages
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45nm SOI Advantage

Ring Delay vs. Active Power

Ring Delay vs. Static Power

Ring Oscillator Delay-Idda(Dynamic)

45nm SOI Delivers Its Promise
- Active & Static Power Improvement
- Delivered frequency performance
- Scaling for unparalleled packaged performance-power ratio

And retains its strong SER reliability advantage vs. bulk!
QorIQ™ Multicore Processors

► Built on 45nm SOI process
  • Low power
  • Aggressively priced
  • Complete processor families that are pin compatible

► Feature DDR3 memory controllers
  • 25% lower power
  • DDR price cross over point has already occurred

► P1000 and P2000 families use proven IP from previous PowerQUICC III families
  making migration easy
  • e500 2.4MIPS/MHz Power Architecture™ core
  • 7 stage pipeline, out-of-order transactions, branch predictions
<table>
<thead>
<tr>
<th>QorIQ™ Platform Levels</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PLATFORMS / PRODUCTS</strong></td>
</tr>
<tr>
<td><strong>QorIQ P5</strong></td>
</tr>
<tr>
<td>PRODUCTS: P5010, P5020</td>
</tr>
<tr>
<td><strong>QorIQ P4</strong></td>
</tr>
<tr>
<td>PRODUCTS: P4080, P4040</td>
</tr>
<tr>
<td><strong>QorIQ P3</strong></td>
</tr>
<tr>
<td>PRODUCTS: P3041</td>
</tr>
<tr>
<td><strong>QorIQ P2</strong></td>
</tr>
<tr>
<td>PRODUCTS: P2020, P2010</td>
</tr>
<tr>
<td><strong>QorIQ P1</strong></td>
</tr>
<tr>
<td>PRODUCTS: P1020, P1011, P1010</td>
</tr>
</tbody>
</table>
Freescale Product Longevity Program

- The embedded market needs **long-term product support**
- Freescale has a longstanding track record of **providing long-term production support** for our products
- Freescale offers a **formal product longevity program** for the market segments we serve
  - For the automotive and medical segments, Freescale will make a broad range of program devices available for a minimum of **15 years**
  - For all other market segments in which Freescale participates, Freescale will make a broad range of devices available for a minimum of **10 years**
  - **Life cycles** begin at the time of launch
- A list of participating **Freescale products** is available at: [www.freescale.com/productlongevity](http://www.freescale.com/productlongevity)
Next Generation Solution Advantage

The industry’s most scalable pin compatible communication processor family

- Performance
  - 1.2 GHz
  - 2x e500 533-800MHz
  - L2 Cache 256KB
  - QUICC Engine, SGMII,
  - PCI-Exp, USB, SD
  - SEC3.3, TDM
- Dual-Core
- Single-Core
- Power
  - 8W
- Reduce development costs through common tool chain and software / hardware reuse.
P1021/P1012 QUICC Engine Feature Overview

► Protocols and Interfaces
  • ATM
  • Serial ATM
  • HDLC/Transparent (bit rate up to 70Mbps)
  • HDLC BUS (bit rate up to 10Mbps)
  • Asynchronous HDLC (bit rate up to 2Mbps)
  • UART
  • BISYNC (bit rate up to 2Mbps)
  • Two TDM interface supporting 64 multichannel, each running at 64Kbps

► ATM Controller
  • Full duplex Segmentation And Reassembly (SAR)
  • AAL5, AAL0 protocols TM4.1, CBR, VBR, UBR, UBR+ traffic types
  • 64K external connections
  • Inverse Multiplexing ATM capability (IMA)
  • ITU-T I.610 based OAM handling
  • One UTOPIA-L2, 8-bit interface (no MPHY support)

► Time Slot Assigner and two TDM Interfaces
  • Independent Rx and Tx routing RAM with 512 routing entries each
  • Time slot assigner with bit or byte resolution
Dual-core P2020 Block Diagram

- **Dual e500 Power Architecture™ core**
  - 800 - 1200 MHz
  - 512KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU

- **System Unit**
  - 64/32b DDR2/DDR3 with ECC to 800MHz datarate
  - Integrated SEC 3.1 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - One USB 2.0 Host Controller with ULPI interface
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE 1588v2 support
    - Two Serial Rapid I/O Controllers with integrated message unit operating up to 3.125GHz
    - Three PCI Express 1.0a Controllers operating at 2.5GHz

- **Process & Package**
  - 45nm SOI, 1.05V +/- 50mV, 0C to 125C Tj
    - with -40C to 125C Tj option
  - 689-pin TePBGAII, 31x31mm

- **8W Max at 1.2GHz**
Single-Core P2010 Block Diagram

- **Single e500 Power Architecture™ core**
  - 800 – 1200 MHz
  - 512KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU

- **System Unit**
  - 64/32b DDR2/DDR3 with ECC to 800MHz datarate
  - Integrated SEC 3.1 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO’s, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - One USB 2.0 Host Controller with ULPI interface
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE 1588v2 support
  - Two Serial Rapid I/O Controllers with integrated message unit operating up to 3.125GHz
  - Three PCI Express 1.0a Controllers operating at 2.5GHz

- **Process & Package**
  - 45nm SOI, 1.05V +/- 50mV, 0C to 125C Tj
    - with -40C to 125C Tj option
  - 689-pin TePBGAII, 31x31mm

- **8W Max at 1.2GHz**
**Dual-Core P1020 Block Diagram**

**Dual e500 Power Architecture™ core**
- 533 – 800 MHz
- 256KB Frontside L2 cache w/ECC, HW cache coherent
- 36 bit physical addressing, DP-FPU

**System Unit**
- 32-bit DDR2/DDR3 with ECC to 800MHz datarate
- Integrated SEC 3.3 Security Engine
- Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO’s, DUART
- 16-bit Enhanced Local Bus supports booting from NAND Flash
- Two USB 2.0Controllers Host/Device support
- SPI controller supporting booting from SPI serial Flash
- SD/MMC card controller supporting booting from Flash cards
- TDM interface
- Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
  - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
  - IEEE1588v2 Support
- Two PCI Express 1.0a Controllers operating at 2.5G Hz
- Power Management

**Process & Package**
- 45nm SOI, XX +/- XX, 0C to 125C Tj
- with -40C to 125C Tj option
- 689-pin TePBGAII, 31x31mm

**5.2W Max at 800MHz**
Single-Core P1011 Block Diagram

- **Single e500 Power Architecture™ core**
  - 533 – 800 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU

- **System Unit**
  - 32-bit DDR2/DDR3 with ECC
  - Integrated SEC 3.3 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO’s, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - Two USB 2.0 Controllers Host/Device support
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - TDM Interface
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE1588v2 Support
    - Two PCI Express 1.0a Controllers operating at 2.5Gb/s
  - Power Management

- **Process & Package**
  - 45nm SOI, XX +/- XX, 0C to 125C Tj
  - with -40C to 125C Tj option
  - 689-pin TePBGAII, 31x31mm

- **4.5W Max at 800MHz**

Samples Q1-10, Qualification Q4-10
Dual-Core P1021 Block Diagram

- Dual e500 core; 533 - 800 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU

- System Unit
  - 32-bit DDR2/DDR3, 800 MHz data rate w/ECC
  - Integrated SEC 3.3 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO’s, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - USB 2.0Controllers Host/Device support
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - IEEE1588v2 Support
    - QUICC Engine for protocol off load and legacy interfaces
      - TDM interfaces with HDLC support
      - UTOPIA-L2 interface for ATM support
  - Two PCI Express 1.0a Controllers operating up to 2.5Gbps
  - Power Management

- Process & Package
  - 45nm SOI, 0.95V+/−50mV, -40C to 125C Tj
  - 689-pin TePBGAII
  - 5.2W Max at 800MHz
Agenda

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  - Software considerations
  - Power supply voltages
  - Frequency & clock ratios
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## Software migration from MPC8548 to P2020

<table>
<thead>
<tr>
<th>IP block</th>
<th>MPC8548E</th>
<th>P2020</th>
<th>Backward Compatible</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Addressing mode</td>
<td>36-bits</td>
<td>36-bits</td>
<td>Yes</td>
<td>As long as 8548 software stays in the low 32-bit address space by default.</td>
</tr>
<tr>
<td>Local Bus Controller</td>
<td>1</td>
<td>1</td>
<td>Yes</td>
<td>P2020 Used enhanced Local bus eLBC</td>
</tr>
<tr>
<td>SRIO</td>
<td>X4</td>
<td>x4</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>PCIe</td>
<td>X8</td>
<td>X4</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>eTSEC</td>
<td>4</td>
<td>3</td>
<td>Yes</td>
<td>P2020 eTSEC 3 signals are muxed with eTSEC1 and eTSEC2</td>
</tr>
<tr>
<td>DDR1 controller</td>
<td></td>
<td>No</td>
<td></td>
<td>DDR1 not supported on P2020</td>
</tr>
<tr>
<td>DDR 2 controller</td>
<td></td>
<td>Yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR 3 controller</td>
<td></td>
<td>No</td>
<td></td>
<td>DDR3 not supported on 8548</td>
</tr>
<tr>
<td>I2C, DUART, eSPI</td>
<td></td>
<td>Yes</td>
<td></td>
<td>P2020 uses enhanced SPI (eSPI)</td>
</tr>
<tr>
<td>eSDHC, USB</td>
<td>0</td>
<td>1</td>
<td>No</td>
<td>This is new IP for P2020.</td>
</tr>
<tr>
<td>DMA Engine</td>
<td>4</td>
<td>4</td>
<td>Yes</td>
<td>P2020 Has external DMA signal on DMA channel 1 and DMA channel 2</td>
</tr>
<tr>
<td>Local Access Windows</td>
<td>10</td>
<td>12</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>L2 Cache Controller</td>
<td></td>
<td>Yes</td>
<td></td>
<td></td>
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<tr>
<td>Interrupt Controller</td>
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### Power Supply Voltage Comparisons

<table>
<thead>
<tr>
<th></th>
<th>MPC8548</th>
<th>P2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>VDD = 1.1 V</td>
<td>VDD = 1.05 V</td>
</tr>
<tr>
<td>PLL</td>
<td>AVDD = 1.1 V</td>
<td>AVDD = 1.05 V</td>
</tr>
<tr>
<td>Power supply for SerDes of SRI0 and PCIE</td>
<td>XVDD = 1.1 V</td>
<td>XVDD = 1.05 V</td>
</tr>
<tr>
<td></td>
<td>SVDD = 1.1 V</td>
<td>SVDD = 1.05 V</td>
</tr>
<tr>
<td>DDR DRAM I/O voltage</td>
<td>GVDD = 2.5 V for DDR1</td>
<td>GVDD = 1.8 V for DDR2</td>
</tr>
<tr>
<td>8548 supports DDR1/DDR2</td>
<td>GVDD = 1.8 V for DDR2</td>
<td>GVDD = 1.5 V for DDR3</td>
</tr>
<tr>
<td>P2020 supports DDR2/DDR3</td>
<td>BVDD = 3.3 V, 2.5 V, or 1.8 V</td>
<td>BVDD = 3.3 V, 2.5 V, or 1.8 V</td>
</tr>
<tr>
<td></td>
<td>CVDD = 3.3 V, 2.5 V, or 1.8 V</td>
<td>CVDD = 3.3 V, 2.5 V, or 1.8 V</td>
</tr>
<tr>
<td>eTSEC I/O</td>
<td>LVDD = 3.3 V or 2.5 V for eTSEC1/2</td>
<td>LVDD = 3.3 V or 2.5 V for eTSEC1/2 and 3</td>
</tr>
<tr>
<td></td>
<td>TVDD = 3.3 V or 2.5 V for eTSEC3/4</td>
<td></td>
</tr>
<tr>
<td>PCI/PCI-X¹, DUART, system control and power management, I2C, GPIOx8 and JTAG I/O voltage</td>
<td>OVDD = 3.3 V</td>
<td>OVDD = 3.3 V</td>
</tr>
<tr>
<td>eLBC I/O voltage and GPIOx8 eSPI, USB², eSDHC²</td>
<td>BVDD = 3.3 V, 2.5 V, or 1.8 V</td>
<td>BVDD = 3.3 V, 2.5 V, or 1.8 V</td>
</tr>
<tr>
<td></td>
<td>CVDD = 3.3 V, 2.5 V, or 1.8 V</td>
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</tr>
</tbody>
</table>

**Note:**
1) PCI/PCI-X only supported on MPC8548 product family.
2) USB, eSDHC only supported on P2020.
## Frequency and Clock Ratio

<table>
<thead>
<tr>
<th></th>
<th>MPC8548E</th>
<th>P2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core frequency</td>
<td>533 MHz to 1.5 GHz</td>
<td>533 MHz to 1.2 GHz</td>
</tr>
<tr>
<td>CCB frequency</td>
<td>266 MHz to 533 MHz</td>
<td>266 MHz to 600 MHz ¹</td>
</tr>
<tr>
<td>DDR data rate</td>
<td>266 MHz to 533 MHz</td>
<td>400 MHz to 800 MHz ²</td>
</tr>
<tr>
<td>Local bus frequency</td>
<td>16.6 MHz to 133 MHz</td>
<td>16.6 MHz to 150 MHz</td>
</tr>
<tr>
<td><strong>P2020 New DDR</strong></td>
<td><strong>-</strong></td>
<td><strong>4:1, 6:1, 8:1, 10:1, 12:1</strong></td>
</tr>
</tbody>
</table>

**Note:**
1) The 600MHz CCB is limited to products that support 1200MHz core speed.
2) For DDR data rate that is higher than the platform frequency, asynchronous mode must be used.
Agenda

- Multi-processing Use Cases
- PowerQUICC III: MPC8548 & MPC8572
- QorIQ™ 45nm Families
- PowerQUICC III Comparison to QorIQ™ Platforms
  - Software considerations
  - Power supply voltages
  - Frequency & clock ratios
- Migration Scenarios
- Altivec Re-introduction
- Single Board Computing
- RTOS/OS Strategy
- Back Up: QorIQ™ P1000 and P2000 Block Descriptions
QorIQ™ Migration Scenarios

- **Improved performance in same power budget**
  - P4080
  - Octal e500 Core
  - To 1500MHz
  - 125kB BS L2/core
  - 2MB L3
  - GE, 10GE, PEX, SRIO
  - Dual DDR2/3
  - Datapath acceleration

- **Reduced Cost Reduced Power**
  - P2020
  - Dual e500 Core
  - 800-1200MHz
  - 512kB L2
  - GE, PEX
  - DDR2/3

- **Dual core performance at single core power DDR3 future proof**
  - P2010
  - Single e500 Core
  - 800-1200MHz
  - 512kB L2
  - GE, PEX
  - DDR2/3

- **Improved frequency in similar power budget 2x the L2 Future-proofed DDR3**
  - 8572
  - Dual e500 Core
  - 1200-1500MHz
  - 1MB L2
  - GE, PEX, SRIO
  - Dual DDR2/3

- **Reduced Cost Reduced Power DDR3 future proof**
  - 8548
  - Single e500 Core
  - 1000-1500MHz
  - 512kB L2
  - GE, PEX, PCI, SRIO
  - DDR1/2

- **Improved performance in similar power budget**
  - 8544
  - Single e500 Core
  - 667-1067MHz
  - 512kB L2
  - GE, PEX, PCI
  - DDR1/2

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# QorIQ™ P1 and P2 Series Comparison

<table>
<thead>
<tr>
<th></th>
<th>P1011</th>
<th>P1020</th>
<th>P2010</th>
<th>P2020</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong></td>
<td>e500 Up to 800MHz 32K I/D</td>
<td>Dual e500 Up to 800MHz 32K I/D</td>
<td>e500 Up to 1200MHz 32K I/D</td>
<td>Dual e500 Up to 1200MHz 32K I/D</td>
</tr>
<tr>
<td><strong>L2 Cache</strong></td>
<td>256KB</td>
<td>256KB</td>
<td>512KB</td>
<td>512KB</td>
</tr>
<tr>
<td><strong>DDR I/F Type/Width</strong></td>
<td>DDR2/3 32-bit</td>
<td>DDR2/3 32-bit</td>
<td>DDR2/3 32/64-bit</td>
<td>DDR2/3 32/64-bit</td>
</tr>
<tr>
<td><strong>10/100/1000 Ethernet (with IEEE1588v2)</strong></td>
<td>3 w/(2) SGMII</td>
<td>3 w/(2) SGMII</td>
<td>3 w/(2) SGMII</td>
<td>3 w/(2) SGMII</td>
</tr>
<tr>
<td><strong>TDM</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>PCI-Exp 1.0a</strong></td>
<td>2 controllers w/ 4 SERDES</td>
<td>2 controllers w/ 4 SERDES</td>
<td>3 controllers w/ 4 SERDES</td>
<td>3 controllers w/ 4 SERDES</td>
</tr>
<tr>
<td><strong>sRIO 1.2</strong></td>
<td>-</td>
<td>-</td>
<td>2 x1 or 1 x4</td>
<td>2 x1 or 1 x4</td>
</tr>
<tr>
<td><strong>USB2.0</strong></td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td><strong>Memory Card</strong></td>
<td>SD/MMC</td>
<td>SD/MMC</td>
<td>SD/MMC</td>
<td>SD/MMC</td>
</tr>
<tr>
<td><strong>Other interfaces</strong></td>
<td>SPI, 2xI2C, DUART</td>
<td>SPI, 2xI2C, DUART</td>
<td>SPI, 2xI2C, DUART</td>
<td>SPI, 2xI2C, DUART</td>
</tr>
<tr>
<td><strong>Accelerators</strong></td>
<td>SEC3.3</td>
<td>SEC3.3</td>
<td>SEC3.1</td>
<td>SEC3.1</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>689 Te PBGAI1</td>
<td>689 Te PBGAI1</td>
<td>689 Te PBGAI1</td>
<td>689 Te PBGAI1</td>
</tr>
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# QorIQ™ P2 and PowerQUICC III

<table>
<thead>
<tr>
<th></th>
<th>MPC8544</th>
<th>P2010</th>
<th>MPC8548</th>
<th>P2020</th>
<th>MPC8572</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>e500 667 – 1067MHz 32K I/D</td>
<td>e500 800 - 1200MHz 32K I/D</td>
<td>e500 1000 - 1333MHz 32K I/D</td>
<td>Dual e500 800 to 1200MHz 32K I/D</td>
<td>Dual e500 1200 to 1500MHz 32K I/D</td>
</tr>
<tr>
<td>L2 Cache</td>
<td>256kB</td>
<td>512KB</td>
<td>512kB</td>
<td>512KB</td>
<td>1MB</td>
</tr>
<tr>
<td>DDR I/F Type/Width</td>
<td>DDR1/2, 64b</td>
<td>DDR2/3, 64-bit</td>
<td>DDR1/2, 64b</td>
<td>DDR2/3, 32/64-bit</td>
<td>Dual DDR2/3, 64b</td>
</tr>
<tr>
<td>10/100/1000 Ethernet</td>
<td>2 w/ all SGMII</td>
<td>3 w/ 2 SGMII</td>
<td>4</td>
<td>3 w/ 2 SGMII</td>
<td>4 w/ all SGMII + 10/100</td>
</tr>
<tr>
<td>PCI</td>
<td>32b PCI + 3 PCIe controllers w/ 9 SerDes</td>
<td>3 PCIe controllers w/ 4 SerDes</td>
<td>64b PCI-X and PCIe w/ 8 SerDes</td>
<td>3 PCIe controllers w/ 4 SerDes</td>
<td>2 PCIe controllers w/ 8 SerDes</td>
</tr>
<tr>
<td>sRIO 1.2</td>
<td>-</td>
<td>2 x1 or 1 x 4</td>
<td>1 x4</td>
<td>2 x1 or 1 x 4</td>
<td>1 x4 or 1 x 1</td>
</tr>
<tr>
<td>USB2.0</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>Local bus controller</td>
<td>32b</td>
<td>16b</td>
<td>32b</td>
<td>16b</td>
<td>32b</td>
</tr>
<tr>
<td>Memory Card</td>
<td>-</td>
<td>SD/MMC</td>
<td>-</td>
<td>SD/MMC</td>
<td>-</td>
</tr>
<tr>
<td>Other interfaces</td>
<td>DUART, 2xI2C</td>
<td>DUART, 2xI2C, SPI</td>
<td>DUART, 2xI2C</td>
<td>DUART, 2xI2C, SPI</td>
<td>DUART, 2xI2C</td>
</tr>
<tr>
<td>Accelerators</td>
<td>SEC2.1</td>
<td>SEC3.1</td>
<td>SEC 3.0</td>
<td>SEC3.1</td>
<td>SEC 3.0, PME, TLU</td>
</tr>
<tr>
<td>Package</td>
<td>783 FC-PBGA</td>
<td>689 Te PBGAII</td>
<td>783 FC-CBGA and FC-PBGA</td>
<td>689 Te PBGAII</td>
<td>1023 FC-PBGA</td>
</tr>
</tbody>
</table>
# QorIQ™ P1 and P2 Series Summary

<table>
<thead>
<tr>
<th>Features</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Best in class ecosystem</td>
<td>Faster time to market</td>
</tr>
<tr>
<td>Migration path</td>
<td>Improved performance/watt/$ migrating from PowerQUICC II, PowerQUICC II Pro, and PowerQUICC III</td>
</tr>
<tr>
<td>High performance e500 2.4MIPS/MHz Power Architecture™ core</td>
<td>High efficiency and frequency cores means fewer cores to get the job done</td>
</tr>
<tr>
<td>Best-in-class power</td>
<td>Enables fanless, “green” and low cost designs, improves reliability</td>
</tr>
<tr>
<td>Integrated Ethernet, TDM, USB, SD Flash controller, IEEE1588, PCI-Express, Serial Rapid IO</td>
<td>Flexibility to address a wide range of applications and reduced system cost</td>
</tr>
<tr>
<td>4.5x performance range in a single package</td>
<td>Common hardware platform to enable wide range of system performance</td>
</tr>
<tr>
<td>Dual and single cores</td>
<td>Move to dual core at your own pace without hardware changes</td>
</tr>
</tbody>
</table>
It’s a smarter approach to multicore. Freescale’s e5500 Core

► Next Generation 64-bit Core Architecture for higher performance, computational intensive applications.
  • 64-bit ISA support (Power Architecture v2.06 compliant)
  • Increased addressable memory space
  • Supports up to 2.2 GHz CPU frequency

► High Performance Classic Floating Point Unit (FPU) for Industrial applications.
  • Supports IEEE Std. 754™FPU Double Precision Floating Point

► Hybrid 32-bit mode to support legacy software and transition to 64-bit architecture.
  • Register settings allow users to utilize 32-bit mode or 64-bit mode, easing transition to 64-bit architecture

Introducing e5500

• Based on the e500mc Architecture with 64-bit ISA

• Core frequency to 2.2 GHz

• Up to 64GB addressable memory space

• Supports up to 512KB backside L2 cache

• High performance classic FPU
# Advantages of e5500- P5020 & P5010

<table>
<thead>
<tr>
<th>Features</th>
<th>Benefits</th>
</tr>
</thead>
</table>
| 64-bit ISA Support                            | • Provides the ability for the core to utilize twice the amount of data per CPU cycle (64-bit vs 32-bit), which increase performance for computational-intensive applications with large data sets  
• Increased addressable memory space makes programming easier as it allows a single process to have a larger address space, and enables more complex applications that need more memory space. |
| 7-stage Pipeline with Out-of-Order Execution  | • Allows the core to continue to do productive work in the event of a stalled instruction or a wrong branch prediction.                                                                                     |
| Floating Point Unit                           | • Classic double precision floating point supported which allows for faster, more accurate computation                                                                                                      |
| Backside L2 Cache                             | • Provides a lower latency cache with higher bandwidth to the core, enabling higher performance, and Reduces the transactions on the shared interconnect and DDR memory                                            |
| Up to 2.2 GHz CPU Frequency                   | • Higher frequency provides additional performance for 32-bit & 64-bit applications. Applications with complex numerical algorithms will particularly see a performance improvement due to 64-bit and higher frequency. |
QorIQ™ P5 Series P5020 Block Diagram

Dual e500mc-64 Power Architecture®
- 2x 64-bit e500mc cores (up to 2 GHz)
- Each with 512 KB backside L2 cache
- Dual 1MB Shared L3 Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Controller
- Dual DDR2/3 SDRAM up to 1.3 GHz
- 32/64 bit data bus w/ECC

High Speed Interconnect
- 4 PCIe 2.0 Controllers
- 2 SRIO 2.1 Controllers
  - Type 9 and 11 messaging
  - 2 SATA 3Gb/s
  - 2 USB 2.0 with PHY

CoreNet Switch Fabric

Ethernet
- 4 x 10/100/1000 Ethernet Controllers
- 1 x 10GE Controller (XAUI)
- 1 GigE maintenance port
- All w/ Classification/Policing, H/W Queuing, policing, and Buffer Management, Checksum Offload, GoS, Lossless Flow Control, IEEE 1588v2, 4 SGMII, QSGMII

Datapath Acceleration
- SEC 4
- PME 2
- RapidIO Messaging

Device
- 45nm SOI Process
- 1295-pin package

Samples Q4-2010, Qualification 2H-11
## P5020 Estimated Power

<table>
<thead>
<tr>
<th>Power Designation</th>
<th>Tj</th>
<th>Pattern</th>
<th>Power (CPU / Platform / DDR MHz) [W] without I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>2000 / 800 / 1333</td>
</tr>
<tr>
<td><strong>“Max”</strong> Power Supply Max</td>
<td>105°C</td>
<td>Contrived Sequence “Smoke Test”</td>
<td>30</td>
</tr>
<tr>
<td><strong>“Typical”</strong> Thermal Max</td>
<td>105°C</td>
<td>Dhrystone</td>
<td>28</td>
</tr>
<tr>
<td><strong>“Typical”</strong> Desktop Operation</td>
<td>65°C</td>
<td>Dhrystone</td>
<td>24</td>
</tr>
</tbody>
</table>

**Power supply max:**
- The device could conceivably draw this much power in short bursts with unusual programming sequences. A power supply should be able to handle this, otherwise it risks drooping.
- These short bursts of increased power won’t impact the temperature of the device which doesn’t respond quickly to increased power. Thus, a thermal solution is not needed for this level of power.

**Desktop Operation**
- 65°C junction temperature likely to be seen with ambient at room temp using simple thermal solution.
- L1-resident Dhrystone is higher power than a “typical” app which access L2 and main memory.

**Thermal Max:**
- This is the highest sustained power expected. It uses the Dhrystone pattern which is an L1-resident pattern. Due to low latency access to L1, stalls and power decreases are minimized.
- Thermal solutions should be designed based on this number.

**Pattern:**
- The contrived sequence, also known as Smoke Test moves data between registers in a core architecture specific way to maximize power consumption. There are no cache or memory access. Any real application would access cache and main memory, and draw less power.
- Dhrystone is an L1-resident pattern correlating well to power observed running EEMBC benchmarks. Stalls are minimized because no L2 or memory accesses occur.
QorIQ™ P5 Series P5010 Block Diagram

Single e500v5 Power Architecture®
- 1x 64-bit e500mc core (up to 2 GHz)
- 512 KB backside L2 cache
- 1MB L3 Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Controller
- DDR2/3 SDRAM up to 1.3 GHz
- 32/64 bit data bus w/ECC

High Speed Interconnect
- 4 PCIe 2.0 Controllers
- 2 SRIO 2.1 Controllers
  - Type 9 and 11 messaging
- 2 SATA 3 Gb/s
- 2 USB 2.0 with PHY

CoreNet Switch Fabric Ethernet
- 4 x 10/100/1000 Ethernet Controllers
- 1 x 10GE Controller (XAUI)
- 1 GigE maintenance port
- All w/ Classification/Policing, H/W Queuing, policing, and Buffer Management, Checksum Offload, QoS, Lossless Flow Control, IEEE 1588v2, 4 SGMII

Datapath Acceleration
- SEC 4
- PME 2
- RapidIO Messaging

Device
- 45nm SOI Process
- 1295-pin package

Samples Q4-2010, Qualification 2H-11
# P5010 Estimated Power

<table>
<thead>
<tr>
<th>Power Designation</th>
<th>Tj</th>
<th>Pattern</th>
<th>Power (CPU / Platform / DDR MHz) [W] without I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>2000 / 800 / 1333</td>
</tr>
<tr>
<td><strong>“Max”</strong> Power Supply Max</td>
<td>105°C</td>
<td>Contrived Sequence “Smoke Test”</td>
<td>23</td>
</tr>
<tr>
<td><strong>“Typical”</strong> Thermal Max</td>
<td>105°C</td>
<td>Dhrystone</td>
<td>22</td>
</tr>
<tr>
<td><strong>“Typical”</strong> Desktop Operation</td>
<td>65°C</td>
<td>Dhrystone</td>
<td>17</td>
</tr>
</tbody>
</table>

- **Power supply max:** The device could conceivably draw this much power in short bursts with unusual programming sequences. A power supply should be able to handle this, otherwise it risks drooping.
- **These short bursts of increased power won’t impact the temperature of the device which doesn’t respond quickly to increased power. Thus, a thermal solution is not needed for this level of power.**

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  - Dhrystone is an L1-resident pattern correlating well to power observed running EEMBC benchmarks. Stalls are minimized because no L2 or memory accesses occur.
Quad e500mc Power Architecture®
- 4 cores (up to 1.5GHz)
- Each with 128KB backside L2 cache
- 1MB Shared L3 Cache w/ECC

Memory Controller
- DDR3/3L SDRAM up to 1.3 GHz
- 32/64 bit data bus w/ECC

High Speed Interconnect
- 4 PCIe 2.0 Controllers
- 2 sRapidIO 2.1 Controllers
  - Type 9 and 11 messaging
- 2 SATA 2.0

CoreNet Switch Fabric

Ethernet
- 5 x 10/100/1000 Ethernet Controllers
  - Or 4x 2.5Gb/s SGMII
- 1 x 10GE Controllers
- All w/ Classification, H/W Queuing, policing, and Buffer Management, Checksum Offload, QoS, Lossless Flow Control, IEEE 1588
- Up to 1 XAUI, 5 SGMII or 2.5Gb/s SGMII, 2 RGMII

Datapath Acceleration
- SEC 4.0
- PME 2.0

Device
- 45nm SOI Process
- 1295-pin package, pin compat with P4040
  - 37.5x37.5mm
- 12W thermal max (est) w/o I/O at 1.2GHz
- 16.5W thermal max (est) w/o I/O at 1.5GHz

First Samples: Q4-10
Qualification Q4-11
## Power Estimates for P3041

<table>
<thead>
<tr>
<th>Power Designation</th>
<th>Tj</th>
<th>Pattern</th>
<th>Power [W] w/o IO</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>1500</td>
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<tr>
<td>“Max” Power Supply Max</td>
<td>105°C</td>
<td>Contrived Sequence “Smoke Test”</td>
<td>17.0</td>
</tr>
<tr>
<td>“Typical” Thermal Max</td>
<td>105°C</td>
<td>Dhrystone</td>
<td>15.7</td>
</tr>
<tr>
<td>“Typical” Desktop Operation</td>
<td>65°C</td>
<td>Dhrystone</td>
<td>11.0</td>
</tr>
</tbody>
</table>

I/O contributes approximately 3.2-3.6W

- **Power supply max:**
  - The device could conceivably draw this much power in short bursts with unusual programming sequences. A power supply should be able to handle this, otherwise it risks drooping.
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  - Dhrystone is an L1-resident pattern correlating well to power observed running EEMBC benchmarks. Stalls are minimized because no L2 or memory accesses occur.
## Core Comparison (e500)

<table>
<thead>
<tr>
<th></th>
<th>e500v1 and v2</th>
<th>e500mc</th>
<th>e5500&lt;sup&gt;4&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Max Frequency</strong></td>
<td>1.5GHz</td>
<td>1.5 GHz</td>
<td>2GHz</td>
</tr>
<tr>
<td><strong>Dhrystone</strong></td>
<td>2.4</td>
<td>2.3</td>
<td>2.4 / 2.9</td>
</tr>
<tr>
<td><strong>Pipeline depth / Width</strong></td>
<td>7 / 2</td>
<td>7 / 2</td>
<td>7 / 2</td>
</tr>
<tr>
<td><strong>Integer Units</strong></td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td><strong>GFLOPs</strong></td>
<td>SP FP = 2 OP/cycle&lt;sup&gt;5&lt;/sup&gt;</td>
<td>SP FP = 1 OP/cycle&lt;sup&gt;2&lt;/sup&gt;</td>
<td>SP FP = 2 OP/cycle&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>DP FP = 1 OP/cycle&lt;sup&gt;2&lt;/sup&gt;</td>
<td>DP FP = 0.5 OP/cycle&lt;sup&gt;2&lt;/sup&gt;</td>
<td>DP FP = 2 OP/cycle&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td><strong>Floating-Point</strong></td>
<td>Embedded</td>
<td>Classic</td>
<td>Classic</td>
</tr>
<tr>
<td><strong>Vector support</strong></td>
<td>SPE</td>
<td>&lt;none&gt;</td>
<td>&lt;none&gt;</td>
</tr>
<tr>
<td><strong>Cache line size</strong></td>
<td>32 bytes</td>
<td>64 bytes</td>
<td>64 bytes</td>
</tr>
<tr>
<td><strong>L1 I and D caches</strong></td>
<td>32K 8-way PLRU</td>
<td>32K 8-way PLRU</td>
<td>32K 8-way PLRU</td>
</tr>
<tr>
<td><strong>Backside private cache</strong></td>
<td>&lt;none&gt;</td>
<td>128KB 8-way backside L2 per core, PLRU replacement</td>
<td>512KB 8-way backside L2 per core, PLRU replacement</td>
</tr>
<tr>
<td><strong>Frontside shared cache</strong></td>
<td>256-1024KB 8-way L2</td>
<td>2MB 32-way CPC&lt;sup&gt;1&lt;/sup&gt;</td>
<td>2MB 32-way CPC&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td><strong>Branch direction prediction</strong></td>
<td>512-entry, two-bit</td>
<td>512-entry, two-bit</td>
<td>512-entry, two-bit</td>
</tr>
</tbody>
</table>

1. **P4080 Implementation**
2. **Pre-silicon calculation**
3. **Includes private backside cache**
4. **64-bit core with 36bit physical addressing**
5. **V2 core with SPE only**
### QorIQ™ Multicore P5, P4 and P3 Series Comparison

<table>
<thead>
<tr>
<th></th>
<th>P5020</th>
<th>P5010</th>
<th>P4080</th>
<th>P4040</th>
<th>P2040</th>
<th>P3041</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong></td>
<td>Dual e5500 to 2200MHz</td>
<td>e5500 to 2200MHz</td>
<td>Octal core e500MC to 1500MHz</td>
<td>Quad core e500MC to 1500MHz</td>
<td>Quad e500MC to 1200MHz</td>
<td>Quad e500MC to 1500MHz</td>
</tr>
<tr>
<td><strong>10/100/1000 Ethernet (with IEEE1588v2)</strong></td>
<td>4x GbE, 1 10GbE, 1 GbE maintenance port</td>
<td>4x GbE, 1 10GbE, 1 GbE maintenance port</td>
<td>X2 Frame Managers w/ 4 x1GbE (SGMII) &amp; 1 10GbE (XAUI)</td>
<td>X2 Frame Managers w/ 4 x1GbE (SGMII) &amp; 1 10GbE (XAUI)</td>
<td>5x GbE</td>
<td>4x GbE, 1 10GbE</td>
</tr>
<tr>
<td><strong>PCI-Exp</strong></td>
<td>X4 gen 2.0</td>
<td>X4 gen 2.0</td>
<td>X3 gen 2.0</td>
<td>X3 gen 2.0</td>
<td>X3 gen 2.0</td>
<td>X3 gen 2.0</td>
</tr>
<tr>
<td><strong>sRIO</strong></td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td><strong>USB2.0</strong></td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td><strong>SerDes</strong></td>
<td>18 lanes @ 5GHz</td>
<td>18 lanes @ 5GHz</td>
<td>18 lanes @ 5GHz</td>
<td>18 lanes @ 5GHz</td>
<td>10 lanes @ 5GHz</td>
<td>12 lanes @ 5GHz</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>DDR2/3 to 1.3GHz</td>
<td>DDR2/3 to 1.3GHz</td>
<td>DDR2/3 to 1.3GHz</td>
<td>DDR2/3 to 1.3GHz</td>
<td>DDR2/3 to 1.067GHz</td>
<td>DDR2/3 to 1.3GHz</td>
</tr>
<tr>
<td><strong>Other interfaces</strong></td>
<td>SPI, 2xI2C, DUART, CoreNet SATA</td>
<td>SPI, 2xI2C, DUART, CoreNet SATA</td>
<td>SPI, 4x I2C, 4x UART, CoreNet</td>
<td>SPI, 4x I2C, 4x UART, CoreNet</td>
<td>SPI, 2xI2C, 4x UART, CoreNet, SATA</td>
<td>SPI, 2xI2C, 4x UART, CoreNet, SATA</td>
</tr>
<tr>
<td><strong>Accelerators</strong></td>
<td>Datapath: SEC 4.0, PME</td>
<td>Datapath: SEC 4.0, PME</td>
<td>Datapath: SEC 4.0, 10Gb/s IP forwarding, PME</td>
<td>Datapath: SEC 4.0, 10Gb/s IP forwarding, PME</td>
<td>Datapath: SEC 4.0, 5Gb/s IP forwarding, PME</td>
<td>Datapath: SEC 4.0, 5Gb/s IP forwarding, PME</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>1295 pin package</td>
<td>1295 pin package</td>
<td>1295 FCPBGA</td>
<td>1295 FCPBGA</td>
<td>783 pin package</td>
<td>1295 FCPBGA (pin compatible P4040)</td>
</tr>
</tbody>
</table>

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Multi-processing Use Cases

PowerQUICC III: MPC8548 & MPC8572

QorIQ™ 45nm Families

PowerQUICC III Comparison to QorIQ™ Platforms
  • Software considerations
  • Power supply voltages
  • Frequency & clock ratios

Migration Scenarios

Altivec Re-introduction

Single Board Computing

RTOS/OS Strategy

Back Up: QorIQ™ P1000 and P2000 Block Descriptions
## Power Architecture® Processor Roadmap

| High Performance within Embedded Power Budget of 30W – 64-bit Cores | QorIQ – P5
|---|---|
| e600 +Soc | Increase FP Perf Next Gen process Security plus AltiVec
| QorIQ – P4
| High Performance within Embedded Power Budget of 30W | P4080
| P4040 | Next Gen Core Increase FP Perf Security plus AltiVec
| Performance at Reasonable Power 15 W | qorIQ – P3
| P3041 | Increase FP Perf Next Gen process Security plus AltiVec
| Value Priced for Power/Performance Applications 10W | PowerQUICC III
| QorIQ – P2040
| P2020/P2011 | Trust Arch More cores AltiVec
| PowerQUICC II Pro
| PowerQUICC II | PowerQUICC I
| QorIQ – P1023/1017
| P1020/P1011
| P1021/P1012
| P1022/P1013 | Multi-core Next Gen Process Trust Arch

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AltiVec Technology on the e5500 Core

► Moving the AltiVec technology to the QorIQ processor family
  • Aligns with the hardware accelerator strategy – offload processing to dedicated functions/applications
  • Utilizing the QorIQ platform power management architecture to manage power of all functions on the device

► The initial core will be e5500 + AltiVec
  • 64-bit core with next-generation Floating Point Unit (increase over e500mc)
  • AltiVec 128-bit SIMD unit which operates independent of Scalar Integer and Floating Point Units
  • Improved functionality
    - Vector Absolute Difference function – single cycle function which previously was taking multiple lines of code
    - Improved Load and Store instructions – which resolve the cumbersome alignment issues and improves performance
    - Gated clocks to minimize dynamic power

► Freescale software enablement support of internally-developed and externally-supplied libraries
AltiVec’s Vector Execution Unit

- Concurrent with Power Architecture integer and floating-point units
- Enhanced separate, dedicated vector registers
- No penalty for mixing integer, floating point and AltiVec operations
Software Enablement for AltiVec Technology

► Freescale-developed libraries and compiler development
  • Application-specific Algorithms Libraries
  • GCC AltiVec improvements for the Open Source community

► Freescale investments and technical support to OEMs and Open Standards (VSIPL)
  • Multicore capable
  • Improving market access of libraries
  • Engineering support and technology to Real Time OS (RTOS) vendors
  • Technical support for library development to OEM’s and industry standards (VSIPL)

► Online User community
Agenda

► Multi-processing Use Cases

► PowerQUICC III: MPC8548 & MPC8572

► QorIQ™ 45nm Families

► PowerQUICC III Comparison to QorIQ™ Platforms
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  • Frequency & clock ratios

► Migration Scenarios

► Altivec Re-introduction

► Single Board Computing

► RTOS/OS Strategy

► Back Up: QorIQ™ P1000 and P2000 Block Descriptions
### Single Board Computer Partners

*Subset of a comprehensive partner ecosystem*

<table>
<thead>
<tr>
<th></th>
<th>COM Express</th>
<th>ATCA Blades</th>
<th>AMC</th>
<th>Compact PCI</th>
<th>PMC’s</th>
<th>ATX, uATX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freescale (dev sys)</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>Curtiss Wright</td>
<td></td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td>KONTRON</td>
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<td></td>
</tr>
<tr>
<td>Emerson Network Power</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td></td>
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<tr>
<td>EuroTech</td>
<td></td>
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<tr>
<td>GE Intelligent Platforms</td>
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<td>Interphase</td>
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<tr>
<td>Mercury</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
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<tr>
<td>RadiSys</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Embedded Planet</td>
<td>✔</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>
Easing the Make vs. Buy Decision with Emerson

► Emerson and Freescale have collaborated to develop a series of production-ready COM Express modules based on Freescale’s QorIQ processors

► Freescale will offer development system that utilize COM Express modules from Emerson
  • $1499/Kit available beginning in November, 2010
  • P4080COME-DS-PB
  • P2020COME-DS-PB
  • P1022COME-DS-PB

P2020COMX
Carrier Blade Supports the Complete QorIQ Family

QorIQ Carrier Blade

- SD/MMC
- Dual CAN
- Five PCIe x4 Connectors
  - 4 lanes of PCIe 2.0/1.0
  - SGMII
  - SRIO
  - XAUI
- 2 PCIe x1
  - Sideband connectors for PCIe x4
  - 1 PCIe x1 for TDM riser
- 8 USB 2.0
- 4 SATA II
- Tamper Detect
- 1 Dual and 1 single GMII
- RJ-11 Phone
- COMe Modules
  - Basic
  - Compact
- 1 DVI-I (digital or analog)
- 2 TFT Display
- 2 Dual DB-9 RS-232 for UART
- 1 dual RMII (100/10MHz), 1 Dual and 1 single GMII (1GHz) RJ-45
- Stereo Audio
- 1 PCIe x1 for TDM riser
- 8 USB 2.0
- 4 SATA II

Other Features:

- Standard barrel ATX power supply
- Capable to support RJ-485 (PROFIBUS)
- Touch screen capable
- OS support from Mentor Graphics, QNX, Green Hills, Wind River
COMX-Pxxx Module Attributes

- Plugs onto custom carrier to provide embedded PC functionality
- CPU soldered down and sometimes memory too
- All connections including custom I/O are via the carrier card
- Inherently Rugged, Pin & Socket Connection
- Off the shelf software
## Emerson COMX-Pxxx – Product at a Glance

<table>
<thead>
<tr>
<th>Part Number</th>
<th>COMX-P4080</th>
<th>COMX-P2020</th>
<th>COMX-P1022</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Form Factor</strong></td>
<td>COM Express Basic</td>
<td>COM Express Compact</td>
<td>COM Express Compact</td>
</tr>
<tr>
<td></td>
<td>(125 X 95mm)</td>
<td>(95 X 95mm)</td>
<td>(95 X 95mm)</td>
</tr>
<tr>
<td><strong>Processor</strong></td>
<td>P4080 - 1.5GHz</td>
<td>P2020 - 1.2 GHz</td>
<td>P1022 - 1.0GHz</td>
</tr>
<tr>
<td><strong>Number of Cores</strong></td>
<td>8</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>Up to 4GB DDR3 ECC SO-UDIMM</td>
<td>Up to 2GB DDR3 ECC SO-UDIMM</td>
<td>Up to 2GB DDR3 ECC SO-UDIMM</td>
</tr>
<tr>
<td><strong>SDIO</strong></td>
<td>MicroSD Slot included on Module</td>
<td>MicroSD Slot included on Module</td>
<td>MicroSD Slot included on Module</td>
</tr>
<tr>
<td><strong>Ethenet</strong></td>
<td>1 x 1GE with integrated PHY Up to 1x10GE XAUI and up to 4 x SGMII ports available via SERDES links</td>
<td>3 x 1GE with integrated PHY</td>
<td>2 x 1GE with integrated PHY</td>
</tr>
<tr>
<td><strong>USB 2.0</strong></td>
<td>4 with integrated PHY</td>
<td>4 with integrated PHY</td>
<td>4 with integrated PHY</td>
</tr>
<tr>
<td><strong>UART</strong></td>
<td>2, with flow control</td>
<td>2, with flow control</td>
<td>2, with flow control</td>
</tr>
<tr>
<td><strong>SPI</strong></td>
<td>1, with 4 chip selects</td>
<td>1, with 4 chip selects</td>
<td>1, with 4 chip selects</td>
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<tr>
<td><strong>GPIO</strong></td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td><strong>I2C</strong></td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td><strong>PCle/Rapid IO</strong></td>
<td>Up to 2x4 SRIOv2 ports and up to 2x4 PCIev 2 ports available via SERDES links</td>
<td>x2 PCIe + x1 PCIe</td>
<td>x2 PCIe + dual x1 PCIe</td>
</tr>
<tr>
<td><strong>Graphics</strong></td>
<td>-</td>
<td>VGA/LVDS</td>
<td>VGA/LVDS</td>
</tr>
<tr>
<td><strong>SATA 2.0</strong></td>
<td>-</td>
<td>-</td>
<td>2</td>
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<tr>
<td><strong>IEEE 1588</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>COM Module Availability</strong></td>
<td>December, 2010</td>
<td>November, 2010</td>
<td>January, 2011</td>
</tr>
<tr>
<td><strong>Power of module</strong></td>
<td>30W typical</td>
<td>12W typical</td>
<td>10W typical</td>
</tr>
<tr>
<td><strong>Freescale Development System</strong></td>
<td>P4080COME-DS-PB</td>
<td>P2020COME-DS-PB</td>
<td>P1022COME-DS-PB</td>
</tr>
<tr>
<td><strong>Dev System Availability</strong></td>
<td>December, 2010</td>
<td>November, 2010</td>
<td>January, 2011</td>
</tr>
</tbody>
</table>
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► Multi-processing Use Cases

► PowerQUICC III: MPC8548 & MPC8572

► QorIQ™ 45nm Families

► PowerQUICC III Comparison to QorIQ™ Platforms
  • Software considerations
  • Power supply voltages
  • Frequency & clock ratios

► Migration Scenarios

► Altivec Re-introduction

► Single Board Computing

► RTOS/OS Strategy

► Back Up: QorIQ™ P1000 and P2000 Block Descriptions
What are the most important factors in choosing a processor?

- Software development tools available
- The chip's performance
- The chip's cost
- Available middleware, drivers, existing code
- The operating system it supports
- HW development tools available
- The on-chip I/O or peripherals
- The chip's power consumption
- Chip family's future growth path
- Familiarity w/ architecture/chip family
- The supplier's reputation
- The processor's debug support

2010 (N = 1,497)
2009 (N = 1,521)
2008 (N = 1,056)
2007 (N = 932)
Linux Growing in Embedded Systems

- Yes (Net)
  - 2010: 57%
  - 2009: 48%
  - 2008: 52%
  - 2007: 48%

- Yes, using it now
  - 2010: 28%
  - 2009: 23%
  - 2008: 21%
  - 2007: 23%

- Yes, likely to use it in next 6 months (soon)
  - 2010: 7%
  - 2009: 6%
  - 2008: 5%
  - 2007: 6%

- Yes, likely to use in next 12 months
  - 2010: 22%
  - 2009: 21%
  - 2008: 20%
  - 2007: 25%

- No, not interested in using it
  - 2010: 43%
  - 2009: 49%
  - 2008: 52%
  - 2007: 48%
Hardware Multi Core Implementations

### Single Core with Hardware Accelerators
- CPU
- Shared Bus
- Bridge
- Shared Bus
- I/O
- I/O
- Accel

- Sequential Operations that cannot be multi-threaded
- Hardware acceleration provides more power/performance efficiency than software

### Homogeneous Multi/Many Core

#### With or Without accelerators

- CPU
- CPU
- CPU
- CPU
- Accel
- I/O
- I/O
- Accel

- Easier Programming Environment
- Easier Migration of Legacy Code
- Lack of specialized hardware for differing tasks

### Heterogeneous Multi/Many Core

- CPU
- GPU
- DSP
- CPU
- Accel
- I/O
- I/O
- FPU

- Specialized hardware for different tasks
- Most power/performance efficient
- Software complexity and Portability

**Increasing Software Complexity**

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Freescale has signed new strategic partnerships with Enea, Green Hills and Mentor Graphics for Freescale’s QorIQ, PowerQUICC and StarCore portfolios.

These deep partnerships call for unprecedented levels of collaboration across the entire silicon lifecycle:
- IP sharing
- Joint investments in technology and product roadmaps
- Go-to-market partnership

Establishes extremely comprehensive enablement support for QorIQ, PowerQUICC and StarCore devices.

Plans call for adding more strategic partners over time.
A better approach

► Freescale is building from a strong foundation of in-house software more than a decade in the making

► Freescale is embracing and expanding proven embedded ecosystem models by adding and nurturing a select number of strategic partners offering unique capabilities

► Freescale is taking a hybrid approach that preserves customer choice, fosters innovation and encourages “cross-pollination” while nurturing select, preferred partnerships that enable comprehensive solutions

• 1999: Metrowerks
• 2002: AMC, Lineo
• 2005: Seaway Networks
• 2008: Intoto
• 2009: MQX Runtime Platform
• Processor Expert - UNIS
Alliance Specifics for Linux Partnership

► Alliance Objectives & Customer Benefits

• Faster availability of Commercial Linux support for Freescale processors
• Seamless migration for customers looking to move from Roll-Your-Own-Linux (RYOL) to Commercial Linux from Mentor
• Highly integrated Linux solutions with specific optimizations for Freescale’s device

► How we will achieve it…

1. Freescale will continue to develop and make available to customers and the community the Linux kernel and basic packages as before
2. Mentor will add to the base from Freescale with their Commercial Linux Offerings
   • Hardening
   • Professional Tools Support (EDGE toolset) including their leading debugger technology
   • Additional Customizations/Packages for specific vertical markets
   • Warranty, Indemnity, Liability, Support & Maintenance
   • Services and Support
3. Mentor and Freescale will partner to develop Linux solutions
   • Distribution is based on SystemBuilder (OpenEmbedded Open Source Framework)
   • LTIB based distribution is expected to be phased-out over time in favor of SystemBuilder
   • Facilitate joint/faster development of basic and advanced Linux software support for Freescale’s devices
NSD Software Strategy

► Continue investment in **silicon optimized IP** across all of our products and platforms

- Own / Control silicon optimized Software IP across all of our hardware devices and platforms
  - Multi-core, PPC, DSP, Accelerator
- Stand alone base tools and run-time Technologies
- Built around standard platforms
- Available throughout the ecosystem

► **Partner for Vertical Solutions**

- Complete solutions in select application spaces – VortiQa Security Apps
- Leverage Partners (ENEA, Mentor Graphics, Green Hills) elsewhere
  - Pro-active technology roadmap and IP alignment
  - Significant IP sharing and reuse
  - Joint go-to-market strategy
Power Architecture® Technology: QorIQ Platform

**Size, Weight, Power and Performance**
- Answering the demands of the market

**QorIQ – A balanced Architecture for performance and power**
- High performance multicore processing
- Tri-level Memory subsystem
- High Speed IO – PCI Express, Rapid IO
- Hardware Acceleration
  - Security and Networking
- CoreNet - Non-blocking Fabric
- Scalable Signal Processing

**QorIQ – Scalable Performance**
- 600 MHz to 2.2 GHz/core
- 4 to 30 Watts
- Single ISA across family

**Tools and OS**
- CodeWarrior
- Broad OS support
  - GreenHills
  - ENEA
  - Mentor
  - QNX
  - Wind River

**Control & Signal Processing**

**Trusted Architecture**
- User controlled line of trust

**Secure Boot**
- Drive Linux® enhancements
- Drive multicore support
- Drive open virtualization technologies
- Drive open firmware, x86 emulation, HAL

**Threat Protection**
- From Loss of Functionality
- From Loss of Data
- From Loss of Uniqueness

**Strong Partitioning**

**Tamper Detection**

**Single Board Computing**
- Curtiss Wright
- Emerson
- Eurotech
- GE Intelligent Platforms
- Mercury Computing
Thank you!
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QorIQ™ P1000 and P2000 Block Descriptions

- IP Lineage
- E500 V2 Processor Core
- L2 Cache Controller
- Enhanced Triple Speed Ethernet Controller
- IEEE1588
- PCI Express and Serial Radio I/O
- Interface Muxing
- USB, SD/MMC Controllers
- SPI Controller
- SEC Engine
- Enhanced Local Bus
- Memory and DMA Controllers
- Programmable Interrupt Controllers
- Run time power management
- Clock Control/Low Power States
## P2020 IP Module Lineage

### Platform IP Block | Source
---|---
e500 CPU Core | Reuse from 8572
L2 Cache | Reuse from 8536
DDR Memory Controller | Reuse from 8572
e500 Coherency Module | Reuse from 8572
Interrupt Controller | Reuse from 8572
Trace Buffer | Reuse from 8572
Performance Monitor | Reuse from 8572
Local Bus | Reuse from 8572
Boot Sequencer | Reuse from 8572
eTSEC | Reuse from 8536
DMA | Reuse from 8572
I2C | Reuse from 8572

### Peripheral IP Block | Source
---|---
DUART | Reuse from 8572
JTAG/COP | Reuse from 8572
Serial RapidIO | Reuse from 8572
PCI Express | Reuse from 8572
SerDes | Reuse from 8572
Security | Reuse from 8572
SGMII | Reuse from 8536
Power Management | Reuse from 8572
USB | Reuse from 8536
SPI | Reuse from 8536
SD/MMC | Reuse from 8536

* From MPC8540

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## High-end PQ3 Differences

<table>
<thead>
<tr>
<th>Platform IP</th>
<th>8548</th>
<th>8572</th>
<th>P2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>e500 CPU core</td>
<td>Single up to 1.5 GHz</td>
<td>Dual up to 1.5GHz</td>
<td>Dual up to 1.2GHz</td>
</tr>
<tr>
<td>L2 Cache</td>
<td>512KB</td>
<td>1MB w/ per way cache allocation to a given CPU core</td>
<td>512KB w/ per way cache allocation to a given CPU core</td>
</tr>
<tr>
<td>DDR Memory Controller</td>
<td>1x 64b DDR1/2 to 533MHz</td>
<td>2x 64b DDR2/3 with Asynchronous Clocking to Platform to 800MHz</td>
<td>1x 64b DDR2/3 with Asynchronous Clocking to Platform to 800MHz</td>
</tr>
<tr>
<td>e500 Coherency Module</td>
<td>Reused</td>
<td>Reused</td>
<td>Reused</td>
</tr>
<tr>
<td>Interrupt Controller</td>
<td>Programmable Interrupt Controller</td>
<td>Multi-processor Programmable Interrupt Controller</td>
<td>Multi-processor Programmable Interrupt Controller</td>
</tr>
<tr>
<td>Performance Monitor</td>
<td>Reused</td>
<td>Reused</td>
<td>Reused</td>
</tr>
<tr>
<td>Trace Buffer</td>
<td>Reused</td>
<td>Reused</td>
<td>Reused</td>
</tr>
<tr>
<td>Local Bus</td>
<td>32b muxed addr/data</td>
<td>32b Enhanced to include NAND Flash Support</td>
<td>16b Enhanced to include NAND Flash Support</td>
</tr>
<tr>
<td>eTSEC</td>
<td>4</td>
<td>4 (Includes SGMII support)</td>
<td>3 (Includes SGMII support)</td>
</tr>
<tr>
<td>PCI-Express</td>
<td>1x8/x4/x2/x1</td>
<td>Reuse: 1x8 or 2x4 or 1x4 and 2x2</td>
<td>Reuse: 1x4 or 2x2 or 1x2 and 2x1</td>
</tr>
<tr>
<td>SHIO</td>
<td>1x4/x1</td>
<td>Reuse</td>
<td>1x4 or dual x1</td>
</tr>
<tr>
<td>DMA</td>
<td>1x4ch</td>
<td>2x4ch (separate 4K space per processor)</td>
<td>2x4ch (separate 4K space per processor)</td>
</tr>
<tr>
<td>Security</td>
<td></td>
<td>RSA key size increased to 4096 bits, SHA-supports 385/512, AES GCM, OFB, and CMAC Support</td>
<td>Upgraded with SNOW</td>
</tr>
<tr>
<td>Table Look up Unit</td>
<td>N/A</td>
<td>2, 1/processor</td>
<td>N/A</td>
</tr>
<tr>
<td>Pattern Matching Engine</td>
<td>N/A</td>
<td>RegEx + Deflate (Decompression)</td>
<td>N/A</td>
</tr>
<tr>
<td>DUART</td>
<td></td>
<td>Reused</td>
<td>Reused</td>
</tr>
<tr>
<td>Dual I2C</td>
<td></td>
<td>Reused</td>
<td>Reused</td>
</tr>
<tr>
<td>Package</td>
<td>783 FCPBGA</td>
<td>1023 FCPBGA</td>
<td>689 TePBGAII</td>
</tr>
<tr>
<td>SPI</td>
<td>N/A</td>
<td>N/A</td>
<td>Serial boot flash</td>
</tr>
<tr>
<td>SD/MMC</td>
<td>N/A</td>
<td>N/A</td>
<td>Integrated controller supports booting from card</td>
</tr>
<tr>
<td>USB Controller</td>
<td>N/A</td>
<td>N/A</td>
<td>ULPI dual role interface</td>
</tr>
<tr>
<td>Power Management</td>
<td>Core sleep, doze, nap, block power down</td>
<td>Reused</td>
<td>Reused</td>
</tr>
</tbody>
</table>

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e500v2 Core Architecture

- Up to 1.2GHz
- L1: 32KB, 8-way set associative, Parity
- L2: Front Side: 8-way set associative, ECC
- Cache line locking supported
- MESI cache coherence
- Peak IPC 2 Instructions plus 1 branch
- Out of Order Execution
- Multiple Book E APUs
- 16 TLB SuperPages
- 512-entry 4K Pages
- 36-bit Physical Address
Shared 512kB unified frontside L2 cache w/8-way associativity (Each way: 64KB)

Assignment Granularity:
- One, two, four, or all eight “ways” of the cache can be assigned as the following:
  - SRAM
  - Stash-Only
  - CPU0 L2 Only
  - CPU1 L2 Only
  - Both CPU0 & CPU1 L2

Stash-Only regions can now be defined
- Prevents stash data from polluting processor data and vice-versa
- One, two or four “ways” of the cache can be dedicated as stash-only

Stash Allocate Disable mode added
- Allows update of all resident cache lines without allocation of new lines
Enhanced Triple Speed Ethernet Controller

- Optimizes CPU performance on TCP/IP
  - TCP/IP checksum offload Rx + Tx
  - IPv6 support in H/W
- QoS support for 16 H/W queues (8 Rx + 8 Tx)
  - Customizable per-packet filing/filtering
  - 802.1p, IP TOS, Diffserv classification
  - Support for weighted fair queueing
  - TCP/UDP port-based flows
  - Assist firewall through IP/TCP/UDP reject
  - Ethernet preamble sorting and insertion
- FIFO I/F to ASICs + (R)GMII/(R)MII/(R)TBI
  - 8/16-bits @ OC-48 rates (155MHz)
- Layer 2 features
  - VLAN insertion and deletion per frame
  - 16 exact-match MAC addresses
  - Lossless Flow Control
- Code compatible with PQ3 e/TSEC controllers

<table>
<thead>
<tr>
<th>eTSEC1</th>
<th>eTSEC2</th>
<th>eTSEC3</th>
</tr>
</thead>
<tbody>
<tr>
<td>GMII/TBI/MII/8b FIFO</td>
<td>GMII/TBI/MII/8b FIFO</td>
<td>SGMII</td>
</tr>
<tr>
<td>RGMII/RTBI/RMII/8b FIFO</td>
<td>RGMII/RTBI/RMII/8b FIFO/SGMII</td>
<td>SGMII</td>
</tr>
<tr>
<td>16b FIFO</td>
<td>SGMII</td>
<td>SGMII</td>
</tr>
<tr>
<td>RGMII/RTBI/RMII</td>
<td>RGMII/RTBI/RMII/SGMII</td>
<td>RGMII/RTBI/RMII/SGMII</td>
</tr>
</tbody>
</table>
IEEE-1588 – Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems

- The standard defines a Precision Time Protocol (PTP) designed to synchronize real-time clocks in a distributed system
- Intended for local area networks using multicast communications (including Ethernet)
- IEEE-1588 was designed to work within a building or factory
  - Intended typically for industrial automation and test and measurement systems (e.g. synchronized printing presses)
- Targeted accuracy of microsecond to sub-microsecond
- Version 1 approved September 2002 and published November 2002
- Version 2 approved March 2008 and published August 2008
- Available from the IEEE-1588 web site (http://ieee1588.nist.gov)
PCI Express

- Three PCI Express controllers
- PCI Express 1.0a compatible
- Supports x1, x2, and x4 link widths @ 2.5 Gbaud, 2.0Gb/s
  - Auto-detection of number of connected lanes
- Selectable as root complex or endpoint at initialization
- 32 and 64b addressing into PCI Express address space
- Root complex inbound support for MSI and INTx
- Endpoint support for outbound MSI
- Reads/writes carried across ports, but not a switch
- 256 byte maximum payload size
- One virtual channel
- Strong and relaxed ordering rules
- 8 non-posted, 6 posted transactions
- 3 inbound + 1 configuration window
  - Translates upper 52b of PCI addr to upper 24b of local addr
  - Window sizes of 4kB to 64GB
  - Settings: read/write type, prefetchable, and target
  - 1MB Config window maps to CCSR region
- 4 outbound + 1 default window
  - Translates upper 24b of local addr to upper 52b of PCI addr
  - Select I/O or memory for reads and writes
  - Window sizes of 4kB to 64GB
Serial RapidIO for Fabric Connectivity

- Dual SRIO controllers for redundancy and greater connectivity
- Compliant to SRIO Interconnect Spec, Rev 1.2
- In-the-box interconnect
  - Chip-to-chip, board-to-board, backplane
  - Greater efficiency than box-to-box protocols
  - Physical layer defined for backplane interconnection
    - ~80–100 cm + 2 connectors (serial)
  - Both memory-mapped and packet-based transactions
- Point-to-point packetized architecture
  - Low overhead
  - Variable packet size
  - Maximum 256 byte PDU
  - SAR support for 4K-byte messages
  - Hardware error recovery
- Implementation
  - 1x or 4x serial, 1.25, 2.5, and 3.125GBaud
  - Read/write bridged between PCI Express port
- Message Unit
  - Two outbound and two inbound message controllers
  - One outbound and one inbound doorbell controllers
P20xx Interface Muxing

- **PCle combinations**
  - x4/x2/x1
  - x2/x1 + x2/x1
  - x2/x1 + x1 + x1

- **SRIO combinations**
  - x4/x1
  - x4/x1 + x1

- **SGMII combinations**
  - x2/x1 PCIe + SGMII + SGMII
  - x1 PCIe + x1 PCIe + SGMII + SGMII
  - x1 SRIO* + x1 SRIO* + SGMII + SGMII
  - x1 PCIe + x1 SRIO* + SGMII + SGMII

  *Note: SRIO runs at 2.5GHz in this configuration*
Hi-Speed USB Controller

- Complies with USB specification rev 2.0
  - High Speed (HS) = 480 Mbit/s
  - Full Speed (FS) = 12 Mbit/s
  - Low Speed (LS) = 1.5 Mbit/s
- EHCI Compliant
- Hi-Speed, Full-speed, and Low-speed
- USB dual role controller
  - Device Controller
    - Six programmable USB bi-directional endpoints
  - Host Controller
    - USB root hub with one downstream facing port
    - EHCI compatible
- Supports external USB PHYs
  - ULPI (UTMI+ Low Pin Interface)
  - Full Speed Serial
► Works with SD Memory, MMC, MMCplus, up to 52MHz
► Supports SD 1-bit/4-bit cards,
  • SD Memory Card Specification version 2.0, support High Capacity SD Memory Card
  • SD Host Controller Std Spec, Ver 2.0
► Supports MMC 1-bit/4-/8-bit cards
  • Compatible with the MMC System Specification version 4.0
► Supports Single Block, Multi Block read and write
► Supports Auto CMD12 for multi-block transfer
► Host can initiate non-data transfer command while data transfer is in progress
► Supports SDIO Read Wait and Suspend/Resume operations
► Additional Features:
  • Supports write protection switch for write operations
  • Supports synchronous abort and asynchronous abort
  • Supports pause during the data transfer at block gap
- Four-signal interface (SPIMOSI, SPIMISO, SPICLK, and SPISEL)
- Full- and half-duplex operation
- eSPI master and RapidS full clock cycle operation support
- 32 byte TX and 32 byte RX Buffers
- 16 and 24 bit Addressing
- Supports a range from 4-bit to 16-bit data characters
- Supports back-to-back character transmission and reception
- Supports single master SPI mode
- Independent programmable baud rate generator
- Programmable clock phase and polarity
- 4 Chip Selects
- Local loopback for testing
Security Engine – SEC 3.1

- Public Key Execution Unit supports:
  - RSA and Diffie-Hellman (to 4096b)
  - Elliptic curve cryptography (1023b)
  - Supports Run Time Equalization

- DES Execution Unit
  - DES, 3DES (2K, 3K)
  - ECB, CBC, OFB modes

- AES Execution Unit
  - Key lengths of 128, 192, and 256b
  - ECB, CBC, CTR, CCM, GCM, CMAC, OFB, CFB, and XTS

- Message Digest Execution Unit
  - SHA-1 160-bit digest
  - SHA-2 256-bit digest
  - SHA-384/512
  - MD5 128-bit digest
  - HMAC with all algorithms

- ARC Four Execution Unit
  - Compatible with RC4 algorithm

- Kasumi Execution Unit (KEU)
  - F8, F9 as required for 3GPP
  - A5/3 for GSM and EDGE
  - GEA-3 for GPRS

- Snow 3G Execution Unit (STEU)
  - Implements Snow 3GPP

- CRC Execution Unit
  - CRC32, CRC32C

- XOR acceleration

- Random Number Generator

- Multi-OS friendly
Enhanced Local Bus Controller (eLBC)

► Multiplexed 32-bit address and 16b data operating to 150MHz
► Eight chip selects support eight external slaves
► Variable memory block sizes (32 KBytes to 4 GBytes)
► Odd/even parity checking
► Atomic operations
► Write protection capability
► Parity byte-select

► General-purpose chip-select machine (GPCM)
  • Compatible with SRAM, EPROM, FEPROM, and peripherals
  • Global (boot) chip-select available at system reset
  • Boot chip-select support for 8- and 16-bit devices
  • Minimum 3-clock access to external devices
  • Two byte-write-enable signals (LWE[0:1])
  • Output enable signal (LOE)
  • External access termination signal (LGTA)

► Three user-programmable machines (UPMs)
  • Can be programmed to support to ZBT and NoBL SRAMs, NAND and NOR Flash, & Compact Flash
  • Programmable-array-based machine controls external signal timing with a granularity of up to one-quarter of an external bus clock period
  • User-specified control-signal patterns can be initiated by software
  • Support for 8- and 16-bit devices
NAND Flash Control Machine (FCM)

- Support for small page (512 data bytes + 16 spare bytes) and large page (2,048 data bytes + 64 spare bytes) parallel NAND flash SLC E²PROM devices
- Support for hardware-based ECC checking and generation
- Global (boot) chip-select available at system reset, with 4 Kbytes boot block buffer for execute-in-place boot loading
- Boot chip-select support for 8-bit devices
- Dual 2-Kbyte/eight 512-byte buffers allow simultaneous data transfer during flash reads and programming
- Interrupt-driven block transfer for reads and writes
- Support for user-programmable command and data transfer sequences of up to eight steps
- Support for proprietary flash interfaces through generic command and address registers
- Block write locking to ensure system security and integrity
- Support for checking/verifying ECC for NAND flash boot blocks
Memory Controller

- DDR2 and DDR3
- 64-bit (72 bits with ECC)
  - 32-bit (40 bit with ECC) also
- 4 chip selects
- Support for up to 4Gb devices, x8, x16, x32 configurations
- Up to 4GB DIMMs per bank
- Up to 16GB
- Supports self-refresh mode
- Battery backup
- Initialization bypass
- Chip-select interleaving
- Automatic DRAM initialization
- Error injection
4ch DMA Controller (x2)

- Each controller in separate 4k memory space to facilitate making it a private resource per core
- 4 channels and all accessible by local and remote masters
- Supports direct, simple chaining, advanced chaining and stride mode
- Support for unaligned transfers
- Support for transfers to and from any local memory or I/O port
- Interrupt on completed segment, link, list and error
- Selectable hardware enforce coherence (snoop/no-snoop)
- Programmable bandwidth control between channels
- Support 256B sub-block transfer for RapidIO & PCI-Express
- Ethernet descriptor mode to transfer data using Ethernet descriptors
DMA Controller Modes of Operation

- **Direct Mode**
  - DMA channel registers initialization by the host (internal or external)
  - Transfer triggered by Software or External Control Signal

- **Chaining Mode:**
  - DMA channel transfer programmed via link descriptor segments in memory
  - Transfer trig by Software or External Control Signal
  - Transfer of a number of segments
Programmable Interrupt Controller

- 12 external IRQ pins
  - Minimum 12 EXTIRQs.
- 43 internal sources (PCIe, L2, eTSEC, etc)
- Multi-core capability
  - Per core interrupt routing
  - Dedicated core interrupts
  - Intercore communication
    - Messages
    - Interrupts
  - Register duplication
  - Multicast delivery for interprocessor and timer interrupts
- Prioritization
  - 16 levels
  - Fully nested
- Modes
  - Pass through and Mixed
- Eight global timers
  - Cascade to create 127-bit timer
  - Can be clocked with divided internal clock or external RTC
- OpenPIC compliant
Normal Interrupt Processing Mechanism

MPIC notifies CPU of new INT by asserting int signal

CPU acknowledges by reading IACK register
- CPU gets INT vector
- INT removed from IPR to ISR

CPU updates CTPR register

End of interrupt routine, EOI instruction, context restored, INT removed from ISR
Runtime Power Management

► Dynamic power management
  • Withholds clocks to e500’s unused execution units, MMUs, caches, and other blocks without performance impact

► Programmable power mode
  • Programmable transition (per core) between e500 modes: full power, doze, nap, and sleep
  • Three external pins track power mode of cores
  • POWMGTCR puts device into sleep or doze

► Memory Controller
  • Dynamic power management
    • Doesn’t clock DRAM when no transactions
  • Sleep/doze mode. DRAM put into self-refresh mode, controller goes into sleep mode

► I/O power management
  • eTSEC’s Magic Packet support: specially defined Ethernet packet received on eTSEC wakes chip from sleep
  • PCI Express power states: D0 – D3, L0 – L3
Configuration Power Management

- Multiplier flexibility to optimize core, internal bus, and DDR performance and power
- Disable unused blocks through DEVDISR register
  - e500 (each individually)
  - PCI Express (all three individually)
  - SRIO (both together)
  - Local bus
  - Security block
  - USB
  - eSDHC
  - SPI
  - DMAs (both individually)
  - eTSECs (each individually)
  - DDR controller
  - I2C (both together)
  - DUART
  - Timers (both sets individually)
## e500 Clock Control Architecture and Low Power States

<table>
<thead>
<tr>
<th>Processor Clocks</th>
<th>Snoops Responded To?</th>
<th>Interrupts Responded To?</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>On</td>
<td>Yes</td>
<td>Yes</td>
<td>Dynamic Power Management (DPM) may be enabled</td>
</tr>
<tr>
<td>Off except time base</td>
<td>No</td>
<td>Yes</td>
<td>Flush data cache before entering</td>
</tr>
<tr>
<td>Off</td>
<td>No</td>
<td>Yes</td>
<td>I/O clocks also turned off except interrupt controller and (optionally) eTSEC</td>
</tr>
</tbody>
</table>
QorIQ™ P2000 DDR2/DDR3 Memory Controller
Customers are expecting DDR3 support on their new product offerings, especially as the price cross-over point has already occurred.

The first device with DDR3 support was 8572.

The first development system with DDR3 was the P2020.

As such, more and more FSL products are supporting DDR3 moving forward.

In this session we will look at key distinctions between DDR3 vs. DDR1 & DDR2, with key emphasis placed on elements that are important to hardware / board design engineers.
DDR3 – Same players

- Supported by all major memory vendors

![Micron](image1.png)  ![ELPIDA](image2.png)  ![Samsung](image3.png)  ![Hynix](image4.png)  ![Infineon](image5.png)  ![Qimonda](image6.png)  ![Nanya](image7.png)
Cross-over has occurred

<table>
<thead>
<tr>
<th></th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td>14%</td>
<td>3%</td>
<td>2%</td>
<td>1%</td>
</tr>
<tr>
<td>DDR2</td>
<td>83%</td>
<td>78%</td>
<td>64%</td>
<td>33%</td>
</tr>
<tr>
<td>DDR3</td>
<td>3%</td>
<td>19%</td>
<td>34%</td>
<td>60%</td>
</tr>
</tbody>
</table>

Source: Micron Marketing
## DDR SDRAM Highlights and Comparison

<table>
<thead>
<tr>
<th>Feature/Category</th>
<th>DDR1</th>
<th>DDR2</th>
<th>DDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>TSOP</td>
<td>BGA only</td>
<td>BGA only</td>
</tr>
<tr>
<td>Densities</td>
<td>128Mb - 1Gb</td>
<td>256Mb - 4Gb</td>
<td>512Mb - 8Gb</td>
</tr>
<tr>
<td>Voltage</td>
<td>2.5V Core</td>
<td>1.8V Core</td>
<td>1.5V Core</td>
</tr>
<tr>
<td></td>
<td>2.5V I/O</td>
<td>1.8V I/O</td>
<td>1.5V I/O</td>
</tr>
<tr>
<td>I/O Signaling</td>
<td>SSTL_2</td>
<td>SSTL_18</td>
<td>SSTL_15</td>
</tr>
<tr>
<td>Internal Memory Banks</td>
<td>4</td>
<td>4 to 8</td>
<td>8</td>
</tr>
<tr>
<td>Data Rate</td>
<td>200–400 Mbps</td>
<td>400–800 Mbps</td>
<td>800–1600 Mbps</td>
</tr>
<tr>
<td>Termination</td>
<td>Motherboard termination to $V_{TT}$ for all signals</td>
<td>On-die termination for data group. $V_{TT}$ termination for address, command, and control</td>
<td>On-die termination for data group. $V_{TT}$ termination for address, command, and control</td>
</tr>
<tr>
<td>Data Strobes</td>
<td>Single Ended</td>
<td>Differential or single</td>
<td>Differential</td>
</tr>
</tbody>
</table>
### DDR SDRAM Highlights and Comparison (cont.)

<table>
<thead>
<tr>
<th>Feature/Category</th>
<th>DDR1</th>
<th>DDR2</th>
<th>DDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Burst Length</td>
<td>BL= 2, 4, 8 (2-bit prefetch)</td>
<td>BL= 4, 8 (4-bit prefetch)</td>
<td>BL= 8 (Burst chop 4) (8-bit prefetch)</td>
</tr>
<tr>
<td>CL/tRCD/tRP</td>
<td>15 ns each</td>
<td>15 ns each</td>
<td>12 ns each</td>
</tr>
<tr>
<td>Master Reset</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>ODT (On-die termination)</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Driver Calibration</td>
<td>No</td>
<td>Off-Chip (OCD)</td>
<td>On-Chip with ZQ pin (ZQ cal)</td>
</tr>
<tr>
<td>Write Leveling</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Typical Freescale DDR2/3 Controller Highlights

► Interface speed
  • DDR2 - up to 800 MHz
  • DDR3 - up to 1600 MHz today

► Support Interface width
  • 64/72-bit data bus – high end product
  • 32/40-bit data bus – low end products
  • 16/24-bit data bus – low end products

► Discrete, unbuffered, and registered DIMM support
  • Memory device densities from 64Mb – through 8Gb
  • Up to four chip selects supported
  • Support for x8/x16 DDR devices – x4 devices are not supported

► Full ECC (Error Correction Code) support
  • Single error correction/detection, double error detection
  • Error injection for software development

► Self refresh support
Typical Freescale DDR2/3 Controller Highlights (cont’d)

► Read-Modify-Write support for Atomic Inc, Dec, Set, Clear, and sub-double word writes
► All timing parameters are under SW control
► Automatic Data Initialization (easy ECC support)
► Differential or Single-ended data strobes
  • Differential option only available for DDR2 memories
  • DDR3 only implements differential DQS signals
► Dedicated Open Row Table for each sub-bank
  • Up to 32 simultaneous open rows with 4 chip selects
► Up to six diff clock pairs
  • Eliminates the need for any external clock PLLs
► ODT support (both internally and externally), on-chip ZQ driver calibration
► SSTL-1.8, and SSTL-1.5 compatible IOs
Freescale DDR3 controller additions

- Freescale New Features Supported for DDR3
- New DRAM initialization sequence supported
  - Accommodates new DDR3 mode register functions
- ZQ Calibration
  - Enable and timing parameters reside in DDR_ZQ_CNTL register
- Write Leveling
  - Enable and timing parameters reside in DDR_WRLVL_CNTL register
- Read Adjust
  - Automatic read adjust per byte lane
- Address Parity
  - Supports address parity for registered DIMMS
- Dynamic ODT
  - Supports Dynamic ODT (Programmable assertion of ODT pin)
- Burst Chop
  - Supports Burst Chop to 4 beats
Key DDR3 Memory Improvements and Additions

- Lower signaling standard
- Reduced power
- Improved device pinout
- Fly-by architecture
- Write Leveling
- Dynamic ODT for improved Write signaling
- Driver calibration
- Device Reset
- DIMM address mirroring
DDR3 Signaling – Example SSTL-1.5

Transmitter

Receiver

V_{DDQ} (1.5V nominal)

V_{OH} (MIN)

V_{OL} (MAX)

V_{SSQ}

V_{IHAC}

V_{IHDC}

V_{REF} + AC Noise

V_{REF} + DC Error

V_{REF} - DC Error

V_{REF} - AC Noise

V_{ILAC}

0.925V

0.850V

0.765V

0.750V

0.650V

0.575V

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Lower Power

► Supply voltage reduced from 1.8V to 1.5V
  • ~ 30% power reduction (Micron claim)
  • ~ 25% is JEDEC’s official claim
    ▪ Compared to DDR2 at same frequency bin

► Lower I/O buffer power
  • 34 ohm driver vs. 18 ohm driver at memory device

► Improved bandwidth per Watt
Improved Pinout

► Improved power delivery
  • More power and ground balls

► Improved signal quality
  • Better power & ground distribution
  • And better signal referencing

► Fully populated ball grid
  • Stronger reliability

► Improved pin placement
  • Less pin skew
  • Tighter timing leaving chip
Introduction of “Fly-by” architecture

- Address, command, control & clocks
- Improved signal integrity…enabling higher speeds
- On module termination
Fly By Routing Improved SI

**DDR2 Matched tree routing**

![Graph for DDR2 Matched tree routing]

**DDR3 Fly by routing**

![Graph for DDR3 Fly by routing]
Fly By Skew Across All receivers

This illustrates the skew created by DDR3 fly by routing
The need for write-leveling….

- **tDQSS requirement:**
  - DQS/DQS# rising edge to CK/CK# rising edge
  - Clock to Strobe should be within a certain range for proper write operation to DDR3 SDRAMs

- **tDQSS spec:** +/- 0.25*tck
Write-Leveling… How it works
Read Adjustment

- Automatic CAS to preamble calibration
- Data strobe to data skew adjustment

Instead of JEDEC’s MPR method, Freescale controllers use a proprietary method of read adjust method which will work with DDR2 and DDR3. This provides comparable performance to JEDEC’s DDR3 MPR method.
Example of termination scheme in application

<table>
<thead>
<tr>
<th>Transaction</th>
<th>Slot 1</th>
<th>Slot 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write to Slot 1</td>
<td>RTT_WR = 120 Ω</td>
<td>RTT Nom = 20 Ω</td>
</tr>
<tr>
<td>Write to Slot 2</td>
<td>RTT Nom = 20 Ω</td>
<td>RTT_WR = 120 Ω</td>
</tr>
</tbody>
</table>

Significant improvement of write signal integrity with dynamic ODT
New DDR3 Pins

- Introduction of an asynchronous RESET# pin
  - Prevent Illegal commands and/or unwanted states
    - Cold reset
    - Warm reset
  - Known initialization
    - Resets all state information
    - No power-down required
    - Destructive to data contents
VREF broken into separate banks (..at the DDR3 memories)

- VREFCA
  - Used for the command / address signals
  - Decoupled to VDD plane
- VREFDQ
  - Used for the data signals
  - Decoupled to VDD plane

Key premise – Noise reduction and coupling between the groups

At the DDR3 controller the same source driving VREFDQ to the memories would drive the controller VREF pin.
NEW DDR3 pins – ZQ Calibration Pin

The RZQ resistor is connected between the DDR3 memory and ground:
- Value = 240 Ohm +/- 1%
- Permits driver and ODT calibration over process, voltage, and temperatures

Easier and more accepted than DDR2’s (optional) OCD method.

Our controllers support both ZQ calibration commands:
- ZQCL – used during initialization (..takes longer)
- ZQCS – used during normal operation (…periodic and takes less time)

Table 9-26. DDR_ZQ_CNTL Field Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ZQ_EN</td>
<td>ZQ Calibration Enable. This bit determines if ZQ calibrating will be used. This bit should only be set if DDR3 memory is used (DDR_SDRAM_CFG[SDRAM_TYPE] = 3'b111). 0 ZQ Calibration will not be used. 1 ZQ Calibration will be used. A ZQCL command will be issued by the DDR controller after POR and anytime the DDR controller is exiting self refresh. A ZQCS command will be issued every 32 refresh sequences to account for VT variations.</td>
</tr>
</tbody>
</table>
Our Freescale controller also does driver calibration
  • Occurs automatically during initialization when MEM_EN is set

MDIC precision resistors are used at our controller
  • Value = 40 Ohms 1% tolerance
DIMM Mirroring…

The DDR3 IP fully supports address mirroring

Non-Mirrored

Mirrored

<table>
<thead>
<tr>
<th>Edge Connector Signal</th>
<th>SDRAM Pin, Standard</th>
<th>SDRAM Pin, Mirrored</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>A0</td>
<td>A0</td>
</tr>
<tr>
<td>A1</td>
<td>A1</td>
<td>A1</td>
</tr>
<tr>
<td>A2</td>
<td>A2</td>
<td>A2</td>
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<tr>
<td>A3</td>
<td>A3</td>
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<tr>
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<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>A15</td>
<td>A15</td>
<td>A15</td>
</tr>
<tr>
<td>BA0</td>
<td>BA0</td>
<td>BA1</td>
</tr>
<tr>
<td>BA1</td>
<td>BA1</td>
<td>BA0</td>
</tr>
<tr>
<td>BA2</td>
<td>BA2</td>
<td>BA2</td>
</tr>
</tbody>
</table>
NEW DDR3 pins – TDQS/TDQS#

TDQS/TDQS# New pin on x8 DDR3 devices
- Not present on x4 or x16 devices
- Allows combinations of x4/x8 devices in the same system.

We don’t support TDQS/TDQS#
- We do not support x4 devices… so this function is not supported

Combinations of different width devices (x8 and x16) in the same system is not supported
#### DDR3 Initialization Flow

1. **Power-up**
2. **DDR Reset**
   - Chip selects enabled and Asserted at least 200us
   - DDR3’s Conduct Precharge
3. **DDR CTRL INIT**
   - DDR clocks begin
   - Stable CLKS
   - CKE = HIGH
   - MEM_EN = 1
4. **Controller Started**
5. **DRAMs Initialized**
6. **ZQ Calibration**
7. **Write Leveling**
8. **Read Adjust**
9. **Init Complete**
10. **Mode Register Commands Issued**
11. **ZQCL Issued (512 clocks)**
   - Also DLL lock time is occurring
12. **Automatically handled**
   - By the controller
13. **Automatic CAS-to-Preamble**
   - (aka Read Leveling)….
   - Plus Data-to-Strobe adjustment
14. **Ready for User accesses**

---

Need at least 500us from reset deassertion to the controller being enabled.

Timed loop may be needed.
DDR2 Initialization Flow

1. **Power-up**
   - Chip selects enabled and DDR clocks begin
   - CKE = HIGH

2. **DRAMs Initialized**
   - Mode Registers Programmed
   - Issued by controller

3. **Wait t_DLL**
   - t_DLL = 512 clocks

4. **Init Complete**
   - Ready for User accesses

5. **Controller Started**
   - MEM_EN = 1

6. **Precharge All**
   - Issued by controller
Burst Length

- Burst Length control (BC4/8 on the fly)
  - 8-bit pre-fetch is standard for DDR3 memories
  - Thus, burst length of 8 is default

- DDR3’s also support ‘pseudo BL4’ using burst chip
-byte lane routing example
120 Ohm / Half Driver / 1 DIMM

Good margins across all data beats

Required
Tsu = 95 ps
Th = 170 ps

8572’s interface pushed up to 1066Mhz

<table>
<thead>
<tr>
<th>Measured Setup (Average)</th>
<th>646 ps</th>
<th>443 ps</th>
<th>440 ps</th>
<th>452 ps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured Hold (Average)</td>
<td>427 ps</td>
<td>405 ps</td>
<td>432 ps</td>
<td>850 ps</td>
</tr>
</tbody>
</table>