Qorivva MCUs - The Scalable 32-bit Platform for Automotive Solutions

AMF-AUT-T1056

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Product Manager
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Trends Driving Performance
### Trends

#### Power
- Need lower power to balance throughput and package constraints
- OEM adopting HEV & EV to meet average fleet fuel economy
- Multi-core architecture & e-Motor control to achieve lower power
- Increasing vehicle content driving request for lower Idd/MCU

#### Performance
- 3-5x performance increase to support auto-coding & signal filtering
- Vehicle electrification driving higher MCU performance demand
- On-chip DSP to meet tighter emission regulations
- DigRF SIPI & Aurora for high speed inter-processor comm & debug

#### Global Support
- Emerging markets & environmental concern = engine downsizing
- Shifting development to BRIC to lower costs
- S/W code re-use, autocoding & scalability = faster development

#### Safety & Security
- Enable ASIL-C or ASIL-D Functional Safety (ISO26262) adoption
- Interest in tamper detection & encryption to deter code tampering
Performance

• Industry’s highest performance powertrain MCU (800 DMIPS)
  - Targeting >1400 DMIPS on 55nm
• Qorivva e200z4 / z7 cores enhanced to run at 200MHz / 300MHz
• On-chip DSP, SIPI and faster debug capabilities
• Reaction channels for precise current control (peak & hold injector)
Power

- 55nm designs optimized to reduce leakage and clock-gating
- Multicore designs allow lower power per MHz
- Higher integration to reduce system level power
- Optimize HEV/EV designs using;
  - FlexPWM
  - eTPU/GTM
  - Resolver
Global Support

• Enablement to support emerging markets
  - Software code examples, engine reference designs and motor control libraries to speed development
  - eTPU function selector to autocode difficult engine parameters
• On-chip hardware to support tighter emission regulations
• Expertise to support engine downsizing
  - shift from 8-cylinders to 4/6-cylinders with turbochargers
Safety and Security

• ISO26262 (Functional Safety)
  – Qorivva supports ASIL-C and ASIL-D applications
    ▪ Lockstep core and end to end ECC on all 55nm products
• Flash Reprogramming Detection and Prevention
  – Tamper detection and encryption options on all 55nm products
  – ECC, HSM, SB256 (secure boot 256-bit encryption)
Freescale Microcontrollers and NVM Technologies

More than 25 years of Automotive Microcontroller Leadership

<table>
<thead>
<tr>
<th>Year</th>
<th>Transistors</th>
<th>CPU Type</th>
<th>Flash Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>1982</td>
<td>20,000</td>
<td>8-bit</td>
<td></td>
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<tr>
<td>1990</td>
<td>200,000</td>
<td>32-bit</td>
<td></td>
</tr>
<tr>
<td>1998</td>
<td>7,000,000</td>
<td>32-bit RISC</td>
<td>1.0MB</td>
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<tr>
<td>2000</td>
<td>14,000,000</td>
<td>32-bit RISC</td>
<td>2.0MByte</td>
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<tr>
<td>2003</td>
<td>34,000,000</td>
<td>MCU/DSP/IO</td>
<td>250MHz, 6MByte</td>
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<tr>
<td>2008</td>
<td>65,000,000</td>
<td>Dual Cores</td>
<td>264MHz, up to 8MByte</td>
</tr>
<tr>
<td>2011</td>
<td>&gt;100,000,000</td>
<td>Multi Cores</td>
<td>&gt;300MHz, up to 16MByte</td>
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<tr>
<td>2014</td>
<td>&gt;200,000,000</td>
<td>Multi Cores</td>
<td></td>
</tr>
</tbody>
</table>

Value proposition
- System performance benefits
- Power performance gains
- Flexibility in customization
- Reduced part counts

Stringent Product Specs
- Wide Temp Range: -40°C to 165°C
- Low Power: standby and active
- Wide Supply Range: Core + 3.3V+ 5V
- High Performance: 20ns access
- High Reliability: zero defect (no returns)
- Tight process controls and periodic audits
Enablement and Functional Safety
The Four Pillars

Safety process
- Integrating functional safety into product development process
- Select products defined and designed from the ground up to comply with the standards

Safety hardware
- Built-in safety functions (self-testing, monitoring and hardware-based redundancy) in Freescale microcontrollers (MCUs), power management ICs and sensors
- Additional system-level safety functionality from Freescale analog solutions (checking MCU timing, voltages and error management)

Safety software
- A comprehensive set of automotive functional safety software, including AUTOSAR OS and associated microcontroller abstraction layer (MCAL) drivers, as well as core self-test capabilities
- Partnerships with leading third-party software providers for additional safety software solutions

Safety support
- From customer-specific training and system design reviews to extensive safety documentation and technical support
High Level Functional Safety (ISO26262) Concept

- Redundant, delayed lock step computational shell
- Data bus pathways with error detection
  - Ensures the integrity of software execution
- Clock Integrity Check
  - Clock monitor circuits on internal clock divider outputs
- Power Supply Integrity Check
  - Low and High Voltage Detectors on internal power supplies
    - Includes supplies to Cores, Flash, ADCs, Oscillator, and I/O
- Detection of latent faults will be handled by:
  - automatic MBIST (Memory Built-in Self Testing)
  - software enabled LBIST (Logic Built-in Self Testing)
- Fault collection and reporting handled by FCCU
  - Configured to generate a range of output signals on fault detection
- Replication of sensor measurements
- Loop back monitoring of actuation signals
- Memory protection modules
  - MPU
Methods for Achieving Diagnostic Coverage

• To achieve diagnostic coverage during application various different methods are available depending on SOC architecture:
  - Pure SW based Self-Test
  - SW based self-test supported by additional testing to increase coverage
  - LBIST (Logic)
  - MBIST (Memory for SRAMs)
  - Peripheral BIST for analog parts
Enablement

- **Software:**
  - AUTOSAR MCAL & OS 4.0 for multicore and ISO26262 support
  - Enhanced multi-core compiler/debugger support
  - Motor control and advanced timer libraries
- **Reference Designs:** Motor control and engine management
- **Hardware:** $100 EVBs (TRAK kits) and calibration tools
- **Calibration:** Support for VertiCal & eCal
Qorivva Comprehensive Ecosystem

Power Architecture® Technology
• The leading architecture for automotive 32-bit processors

Development Tools
• Best-in-class compiler support for Power Architecture
• Multi-core debuggers from Freescale and development partners
• Online development support includes (appnotes, training and code examples)

Run-time Software
• AUTOSAR MCAL driver
• AUTOSAR RTOS, single core (v3.x) and multicore (v4.0)

AutoSAR Partners
• KPIT Cummins – On demand delivery
• Merce – On demand delivery
• Electrobit – All MCAL & OS
• Vector – All MCAL & OS
• ETAS – On demand delivery
• MentorGraphics – On demand delivery

Consortium & Standards
• Founding member of FlexRay™ and LIN consortia
• Premium member of AUTOSAR™
• PSI5 Consortium

Regional Auto Labs & Support
• Systems lab support around the globe (Munich, Detroit, Tokyo, Seoul, Shanghai, Delhi)
• Software customization services direct from Freescale
Roadmaps
Advanced Architectures: Powertrain

**Multicore Processing**
(enhances throughput)

**Lockstep Core**
(safety)

**I/O Processor**
(offloads main cores)

**Crossbar**
(reduces delays in multicore memory access)

**DSP Functionality**

**Local I-RAM / D-RAM**
(instruction RAM, data RAM) to maximize throughput

**Embedded Flash / RAM**

**Crossbar Processing**
(reduces delays in multicore memory access)

**COMPUTATIONAL SHELL**

- 300 MHz Cores
- 200 MHz Crossbar

- Power™ e200Z7
- FPU
- VLE
- 16k I-Cache
- 4k D-Cache
- MPU

- SWT
- STM
- INTC
- MCM
- I-RAM 32k
- D-RAM 64k

- Power™ e200Z7
- FPU
- VLE
- 16k I-Cache
- 4k D-Cache
- MPU

- SWT
- STM
- INTC
- MCM
- I-RAM 32k
- D-RAM 64k

**PERIPHERALS CONTROL SHELL**

- 200 MHz Core
- 100 MHz Crossbar - 50 MHz Periphery

- Power™ e200Z4
- SWT
- STM
- INTC
- MCM
- I-RAM 32k
- D-RAM 32k

- Power™ e200Z4
- SWT
- STM
- INTC
- MCM
- I-RAM 32k
- D-RAM 32k

- eDMA
- SIPI/DigRF
- Ethernet
- 2x FlexRay
- Hardware Security Module

- Bridge A
- Bridge B

- Periph
- Periph
- Periph
- Periph

- eTPU
- FlexPWM
- GTM

- High-Speed A/D Converters
- Reaction Channels
- Decimation Filters

**Reaction Channels**

**Decimation Filters**
eTPU

- **Key Market Characteristics**
  - Maintained for legacy customers
  - Large eTPU code base, mature toolset

- **Key Technical Characteristics**
  - Upgrading design process for ASIL C/D
  - Lockstep and safety designs
  - Improved reaction channels for current control
  - Decimation filters
GTM Introduction

- **Key Market Characteristics**
  - Defined and developed by Bosch
  - Continental is close follower
  - Developed for “standard” timer from multiple sources

- **Key Technical Characteristics**
  - Multicore architectures
  - Data flow driven design concept
  - Configurable dedicated hardware sub-modules
  - Central routing unit managing all internal data movement between sub-modules.
  - Internal programmable RISC-like cores
  - Qual Q1 2014

- **Drawbacks**
  - Reliance on Bosch by Freescale and non-Bosch Tier 1s
  - Weakness for motor control

MPC5746M McKinley
4M Flash, 320k SRAM
2CC + 1LS 200MHz, 1IO 200MHz
FlexRay & Ethernet, GTM

Core Legend
CC = Computational Core
IO = I/O Processor
LS = Lockstep Core
Powertrain MCU Roadmap

Applications

High-end
>6 Cylinder

Mid-range
6 Cylinder Transmission HEV / EV

Low-end <= 4 Cylinder

90 nm

MPC567xR
2 x 180MHz
6M, eTPU2

MPC567xF
264MHz
3M – 4M, eTPU2

MPC564xA
150MHz
2M – 4M, eTPU2

MPC564xL
120MHz
1M, FlexPWM

MPC563xM
80MHz
768K – 1.5M, eTPU2

S12 (X)
50MHz
16 bit, 128K -1M, X-Gate

55 nm

MPC5746M
2 x CC & 1xLS @ 200MHz,
1 x IOP @ 200MHz
4MB, GTM, ∑∆ADC

Powertrain

1st Si

Proposal
Planning
Execution
Production

Qorivva™

Single Core
Dual Core
Multi Core

CC – Computation core
IOP – I/O processor
LS – Lockstep core

< 2012 | 2013 | 2014 | 2015

High-end
>6 Cylinder

Mid-range
6 Cylinder Transmission HEV / EV

Low-end <= 4 Cylinder

< 2012
Jun12
MPC5676R (Cobra90) Block Diagram

- **Modes & Memory**
  - 2 x Computational cores @ 180MHz
    - Cores include VLE, SPE1.1, FPU
    - 16kB i-cache & 16kB data-cache w/ coherency
  - Up to 6MB Flash RWW w/ ECC
  - Up to 461kB total SRAM
    - 384kB on chip static RAM w/ECC (up to 48KB standby)
    - 45kB eTPU RAM, 32kB data cache

- **I/O & System**
  - 64ch Quad RSD ADC (12bit res.w/ 670ns conversions)
    - On-chip temperature sensor and VGA (x1,x2,x4)
    - 12 x Decimation Filters w/ hardware knock integrators
  - 3 x 32ch eTPU2 & 32ch eMIOS timer (128ch total)
  - 2 x 64ch eDMA support (128ch total)
  - 4 x FlexCAN & dual channel Flexray communication ports
    - 64 message buffers on FlexCAN
  - Serial – 3 x eSCI and 5 x DSPI w/ Microsecond bus support
  - 1 x CRC unit – w/ 3 independent channels, 4 x protected port outputs, MPU and MMU
  - FMPLL – plus IRC for fast start up

- **Packaging**
  - 416 PBGA and 516 PBGA
  - 552CSP for VertiCal calibration

- **Key Electrical Data**
  - -40 to +125°C (ambient), Single 5V power supply option
MPC5746M McKinley 4M Block Diagram

- **Key Functional Characteristics**
  - Two independent 200 MHz Power Architecture z4 computational cores
    - Single 200 MHz Power Architecture z4 core in delayed lockstep for ASIL-D safety
  - Single I/O 200 MHz Power Architecture z4 core
  - eDMA controller – 64 channels
  - 4M Flash with ECC
  - 320k total SRAM with ECC
    - 128k of system RAM (incl. 64k standby on 292 PBGA package)
    - 192k of tightly coupled data RAM
  - 6 ΣΔ & 8 SAR converters – 60 channels on 292 MAPBGA, 48 channels on 176 LQFP
  - Ethernet (MII/RMII)
  - DSPi – 7 channels (2 supporting μSec ch.)
  - LINFlex - 5 channels (2 supporting μSec ch.)
  - MCAN-FD/TTCAN – 3x modules/1x module
  - GTM – 120 timer channels

- **Key Electrical Characteristics**
  - -40 to +125 °C (ambient)
  - 165 °C junction for KGD
  - 1.26V Vdd, 5.0V I/O, 5V ADC

- **Package**
  - 176 LQFP / EP, 292 PBGA
  - eCal emulation device for each package

- **Enablement**
  - Software: AutoSAR drivers
  - Tools
    - Debugger: Green Hills, Lauterbach and PLS
    - Multicore compiler: HighTec, GCC, Wind River, GHS
  - Simulation tools

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**Core**
- Dual up to 180 MHz PowerTM ISA e200 zen4 core (Z420)
- 32 bit Reg File, 64 bit BIU with E2E ECC
- 64kB RAM of D-LMEM with MPU for fast context switch + local data
- 8KB 2-way I-cache / 4KB 2-way D-Cache
- 1x Scalar FPU (compiler supported) per core
- Safety enhanced Cores – VLE only
- No Signal processing unit extension + NO MMU
- Delayed Lock Step configuration only

**Memory**
- 2.5 MBytes NVM with ECC (with add. Safety measure for address)
- 64kB EEE (Data Flash) available incl. ECC
- Up to 384 Kbyte global system SRAM with ECC (Addr + Data)

**I/O**
- 3 x FlexCAN (64+2x32 message buffers)
- 1 x FlexRay (Dual Channel 64 msg. buffers)
- 2 x LINFlex (Uart/Lin protocol driver)
- 4 x DSPI (4 cs each)
- 2x FlexPWM (2x 12ch for 2 independent Motors Controlled)
- 3 x eTimer modules (18 channel total)
- 4 x SAR ADC – 1MS/s target 5V input capable
- 2 x Cross-triggering unit for motor control automatism
- 2x SENT

**System**
- Interprocessor I/F SIPI (~ approx 300Mbaud)
- Safe DMA
- Fault Collection unit, WDG, T-sens, & CRC computing unit
- Nexus debug interface – Aurora
- Dual-PLL (Peripheral + System Core)
- 3.3 V Single supply: internal regulator with external power stage or External supply
- 3.3 V I/Os (ADC 5 V capable)
- 144 LQFP / 257 MAPBGA 0.8 mm pitch
- Tj = 150°C . Extended Temperature at 165°C Option (separate P/N)
# Panther Family

<table>
<thead>
<tr>
<th></th>
<th>Panther</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Flash</strong></td>
<td>1M</td>
</tr>
<tr>
<td></td>
<td>1.5M</td>
</tr>
<tr>
<td></td>
<td>2M</td>
</tr>
<tr>
<td></td>
<td>2.5M</td>
</tr>
<tr>
<td><strong>Core/Platform</strong></td>
<td>2 x z4, 180MHz</td>
</tr>
<tr>
<td><strong>SRAM</strong></td>
<td>128K</td>
</tr>
<tr>
<td></td>
<td>192K</td>
</tr>
<tr>
<td></td>
<td>256K</td>
</tr>
<tr>
<td></td>
<td>384K</td>
</tr>
<tr>
<td><strong>ASIL</strong></td>
<td>ASIL D</td>
</tr>
<tr>
<td><strong>I/O</strong></td>
<td>SENT, ADC, FlexCAN, FlexRay, LinFlex, DSPI, FlexPWM etc shared throughout the family</td>
</tr>
<tr>
<td><strong>System</strong></td>
<td>Dual PLL, safe DMA, FCU, T-sens, etc shared throughout the family</td>
</tr>
<tr>
<td><strong>Other IP</strong></td>
<td>SIPI, Nexus debug interface - Aurora</td>
</tr>
<tr>
<td><strong>Tj</strong></td>
<td>165 °C</td>
</tr>
<tr>
<td><strong>Packages</strong></td>
<td>144 LQFP or 257 MAPBGA</td>
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FSL 32-bit Body Legacy and Next Gen Drivers

- Freescale is a Leader in the 32-bit body MCU space
  - First targeted body product launch was the dual core MPC5510 family nearly 5 years go.
  - Bolero product family has a large customer install base and is widely adopted for a range of BCM/Gateway applications.
  - Currently developing 3rd generation of BCM/Gateway products

- Moving forward, customers are looking for next gen products that provide additional functionality and cost reduction.
  - Advanced communication requirements
  - Higher performance and increased memory
  - Improved power consumption
  - Support of Functional Safety
  - Competitive Tier 1 market driving need for reduced component costs
32-bit Next Gen High End Body MCU Roadmap

- **FSL Calypso family of MCUs offers:**
  - **Advanced Communication Peripherals** – Ethernet AVB support, USB, SDHC, FlexRay, MOST, higher quantity of LINs, CANs, CAN FD support, etc
  - **Improved Performance** - multicore MCUs options, increased MHz
  - **Large Flash and RAM** to support increased message handling/code requirements
  - **New Low Power Unit** with improved functionality in low power modes
  - **Support of Functional Safety** – ISO26262 process, targeting ASIL-B
  - **Enhanced Hardware Security Module**
  - **Family Concept** – Scalable HW and SW approach within Calypso family and migration path from the widely used Bolero family
  - **Availability** – 55nm products in design, Bolero 90nm can be used for early development today.
32-bit Body Electronics MCU Roadmap

**Fado/Bolero 90nm Products**

- **MPC5668G/E**
  - z6+z0, 116MHz,
  - Up to 2M Flash, 598k RAM
  - Flex, Ether, MLB, CAN, LIN

- **MPC5668E**
  - z6+z0, 116MHz,
  - Up to 2M Flash, 598k RAM
  - Flex, Ether, MLB, CAN, LIN

- **MPC5607/6/5/B**
  - z6, 64MHz,
  - Up to 1.5M Flash, 96k RAM
  - CAN, LIN

**55 nm Next Gen Products**

- **MPC5646/5/4C**
  - z4+z0, 120MHz,
  - Up to 3M Flash, 256k RAM,
  - Flex, Ether, Security,
  - CAN, LIN

- **MPC5646/5/4B**
  - z4, 120MHz,
  - Up to 3M Flash, 192k RAM,
  - Flex, Security,
  - CAN, LIN

- **MPC5604/3/2/B/C**
  - z0, 64MHz,
  - Up to 512k Flash, 48k RAM
  - CAN, LIN

- **MPC5602/1D**
  - z0, 48MHz,
  - Up to 256k Flash, 16k RAM
  - CAN, LIN

**Integrated Gateways**

- **MPC5748/7/6G**
  - z4+z4+z2, 160MHz,
  - 3M-6M Flash,
  - Flex, Ether, Security,
  - MLB, USB, CAN, LIN

**Past**

- 2012
- 2013
- 2014
- 2015
- 2016

**Production**

- Proposal
- Planning
- Execution
- Production

First Sample Date (left edge)
Product Qualification (right edge)
**MPC5748G - High End Gateway/BCM Solution**

**Applications:**
- High end Gateway and Body Modules

**Key Characteristics:**
- 2x e200z4 + 1x z2 cores, FPU on z4 cores
- 160 MHz max for z4s and 80 MHz on z2
- HSM Security Module option supports both SHE and EVITA low/medium standard
- Media Local Bus supports MOST communication
- 2 x USB 2.0 (1 OTG and 1 Host module) support interfacing to 3G modem and infotainment domain
- Ethernet 10/100 Mbps RMII, MII, +1588, AVB
- SDHC provides standard SDIO interface
- Low Power Unit provides reduced CAN, LIN, SPI, ADC functionality in low power mode
- Designed to ISO26262 process for use in ASIL B
- -40 to +125C (ambient)
- 3.0V to 5.5V

**Packages:**
- 176 LQFP, 256 BGA, 324 BGA

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**Diagram Notes:**
* Mixture of internal and external channels
MPC5646C vs MPC5748G

- Dual core
- Security module (CSE)
- Communications peripherals

- Reuse of Power Arch Technology, Crossbar and some basic modules
- New and Improved – Security, communication peripherals, low power functionality, functional safety
- Pin out very similar to Bolero MPC5646C – only 3 pin difference
• Green: Protected by HW
• Red: Protected by redundant/diverse use by SW
  - (HW replication but not checkers)
• Blue: Other measures necessary/not safety relevant
Core Replication Detail

- TCMs not replicated
- Checker core with 1 clock delay
- No bus access from checker core
- ECC end point replicated
  - No ECC miscorrection problems
- Checker core has reduced debugging functionality
  - Reduces CCF potential