Layerscape - New Embedded Family Solution
EUF-NET-T1280

Haim Cohen
Agenda

- Introducing the QorIQ LS1 Family
- Target Markets and Applications
- QorIQ LS1 Processors-Block diagrams
- QorIQ LS1 Use Case Examples
- Deliverables Schedule and Enablement Plan
- Summary
Introducing the QorIQ LS1 Family
Highest Level of Integration Under 3 W

Leveraging over 20 years of networking expertise, the ARM®-based QorIQ LS1 family is optimized to offer high efficiency, leading integration and a broad array of high-speed interconnects for power-constrained applications.
Market Trends

Networks strained by use of smarter, bandwidth-hungry devices need:

- Multicore platforms performing more intelligently and securely
- Virtualized systems for scalability and speed of deployment
- Low-power, low-cost, easy-to-use equipment – without sacrificing performance

Time to market pressures require abstraction of system-level complexity

- Increased need for high-level languages
- Application level/full-suite software solutions have become table stakes

Standardization and openness of hardware, software and tools
Comprehensive Portfolio Based on ARM Technology

Kinetis Microcontrollers
Design Potential. Realized

Industry’s most scalable ultra-low-power, mixed-signal MCU solutions based on the ARM® Cortex™-M and Cortex™-M0+ architectures.

Vybrid Controller Solutions
Rich Apps in Real Time.

Real-time, highly integrated solutions with best-in-class 2D graphics to enable your system to control, interface, connect, secure and scale.

i.MX Application Processors
Your Interface to the World.

Industry’s most versatile solutions for multimedia and display applications, with multicore scalability and market-leading power, performance & integration.

QorIQ Processors built on Layerscape Architecture
Accelerating the Network’s IQ

Industry’s first software-aware, core-agnostic networking system architecture for the smarter, more capable networks of tomorrow – end to end.

Automotive

Freescale has the industry’s broadest range of solutions built on ARM® technology for automotive, industrial, consumer and networking applications.

Find your ideal solution at the price, performance and power level you desire, and leverage the extensive software and tool bundles available to speed and ease your design process.
Cortex A7 Delivers Extreme Power Efficiency

- **Power efficient microarchitecture**
  - In-order 8-stage, partial dual-issue
  - Integrated L2, improved memory system
  - 0.35 Specint2K/MHz, 1.86DMIPS/MHz

- **Architecture aligned with Cortex A-15**
  - Hardware enhanced OS virtualization
  - AMBA4 ACE system coherency
  - 1 TB physical memory addressable

- **Available Now**

### 28 HPM Process Targets

<table>
<thead>
<tr>
<th></th>
<th>Desired Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (worst/OD)</td>
<td>850 MHz/1.0 GHz</td>
</tr>
<tr>
<td>Power (P_dyn)</td>
<td>0.080 mw/MHz</td>
</tr>
<tr>
<td>Power (P_static)</td>
<td>30.7mW</td>
</tr>
<tr>
<td>Area (MP2 + L2)</td>
<td>1.86 mm²</td>
</tr>
</tbody>
</table>

* Power is per core, Dhrystone, Pdyn TT/85C, 28HPM Dual-core w/256KB L2, each core with 32K x 32K L1, NEON, FPU, Frequency at SSG, 9T, Vnom-10%, Vcore at 0.9V (worst)

Compelling performance at <100 mW
LS1 Family Differentiated Features

- **Performance starts with the core**
  - Dual ARM Cortex-A7 cores delivering over 6,000 CoreMark® of performance at **under 3W (typical)** for improved performance without increased power utilization
  - **Best in class** 1.7 CoreMark / mW ratio

- **Broadest range of peripheral and I/O features in its class**
  - Only product in its class to offer **ECC protection** for both L1/L2 caches, meeting networking requirements for **high reliability**
  - **Virtualization support** enables partitioning of CPU resources on low-power parts for increased system productivity
  - **First in its class** to offer support for DDR4 memory ensuring continued **performance efficiency**
  - Only communications processor to combine **LCD controller, USB 3.0 with integrated PHY, SD/MMC and SATA3 on a single SoC** to enable lower system-level costs
  - **QUICC Engine** provides **proven support** for protocols required in industrial, building and factory automation applications

LS102x Target Applications

- Management processor
- Multi-service IOT gateways
- 802.11ac AP routers
- Carrier line cards
- Printing & Imaging
- Networked attached storage
- Industrial Automation & control
- M2M
- Robotics
Target Markets and Applications

Enterprise Networking
- High-speed interfaces
- Security engine
- ECC-protected caches
- Virtualization

Industrial Automation and Control
- Industrial interfaces
- LCD for HMI support
- Industrial protocol support

IoT Gateways
- High-speed interfaces
- Multi-protocol support
- High-bandwidth LAN/WAN support

The LS1 processors extend Freescale’s market leadership in communications processors and enables new categories of applications under 3 W.

$1.9B SAM in 2015

Industrial Automation and Control
- Industrial Automation
- IoT Gateways
- Surveillance
- Energy Gateway
- Multi-Protocol Gateway
- Service Provider Res Gateway
- Carrier Line Cards
- Fixed Switches
- Security Appliance
- NAS

Other 15%

Enterprise Networking 35%

Source: IDC and IMS Research, World Market for Internet connected Devices, August, 2012
Scalable LS102xA Family of ARM Cortex-A7 Processors

LS102xA Family: All feature Dual Cortex A7 Cores

Networking
- Up to 1 GHz, 2.6W Typ.
- Enterprise & Consumer Networking
- Enterprise WLAN AP’s
- Gateways
- Security Appliances

Industrial & Printing
- Up to 1 GHz, 2.8W Typ.
- Adds LCDC and CAN
- Printing
- Factory Automation
- Building Automation
- Defense & Aero
- M2M

Entry Consumer & Industrial
- Up to 600 MHz, 2W Typ.
- For demanding low-power designs

Pin & Software Compatible
QorIQ LS1021A

- Dual ARM Cortex-A7 cores up to 1.0 GHz
  - ECC protected L1/L2 caches
  - DDR3L/4 up to 1.6 GHz
- Over 5,000 Coremark at under 3.7W (TDP(thermal design power) power)
- Industry best Coremark / mW ratio
- Outstanding security and IP forwarding
- High integration reduces BOM costs for targeted applications:
  - Industrial gateways
  - Industrial Automation
  - Printing & Imaging
  - HMI
  - M2M, Smart “X”

Key Architectural Features:
- ARM AMBA4 MPCore™ Virtualization
- DDR3L/4 32-bit with ECC support
- 3-port GigE with IEEE 1588
- 2x PCI Express Gen2
- Multi-protocol 4-Lane SerDes
- PCIe-2, SATA3, SGMII
- QUICC Engine – HDLC/TDM/ProfiBUS
- EnergyStar support with fast wakeup
- 2Gbps IP forwarding

Key System Integration Features:
- Low-cost NAND/NOR flash systems
- Low-cost DRAM systems
- USB3 SuperSpeed
- Audio networking and motor control
- QorIQ Trust Architecture and ARM TrustZone support
- Alignment with Kinetis/Vybrid portfolio

Package & Board:
- Package: 525-pin, 19x19mm, 0.8mm ball pitch
- Power: ~2.8W @1.0 GHz Typical
- Temp: -40C (TA) to 105C (Tj)
- Boards: Tower low-cost board
  Freescale Linux BSPs
QorIQ LS1020A

- Dual ARM Cortex-A7 cores up to 1.0 GHz
  - ECC protected L1/L2 caches
  - DDR3L/4 up to 1.6 GHz
- Over 5,000 Coremark at under 3.6W (TDP power)
- Industry best Coremark / mW ratio
- Outstanding security and IP forwarding
- High integration reduces BOM costs for targeted applications:
  - 802.11ac AP Routers
  - Line cards
  - Multi-service gateways
  - M2M, Smart “X”

Key Architectural Features:
- ARM AMBA4 MPCore™ Virtualization
- DDR3L/4 32-bit with ECC support
- 3-port GigE with IEEE 1588
- 2x PCI Express Gen2
- Multi-protocol 4-Lane SerDes
- PCIe-2, SATA3, SGMII
- QUICC Engine – HDLC/TDM
- EnergyStar support with fast wakeup
- 2 Gbps IP /1Gbps IPSec forwarding

Key System Integration Features:
- Low-cost NAND/NOR flash systems
- Low-cost DRAM systems
- USB3.0 Super Speed (5GT/s)
- SATA III (6GT/s)
- Audio networking
- QorIQ Trust Architecture and ARM TrustZone support
- Alignment with Kinetis/Vybrid portfolio

Package & Board:
- Package: 525-pin, 19x19 mm, 0.8 mm ball pitch
- Power: ~2.6W @1.0 GHz Typical
- Temp: -40C (TA) to 105C (Tj)
- Boards: Tower low-cost board
- Freescale Linux BSPs
QorIQ LS1022A

- Dual ARM Cortex-A7 cores up to 600 MHz
  - Coherent 512 KB L2 cache
  - DDR3L up to 1 GHz
- Over 3,000 Coremarks at under 3W (TDP power)
- Outstanding Coremark / mW ratio: 1.1 Coremarks / mW
- Excellent IP forwarding
- Lowest power-to-performance ratio in class, ideal for targeted applications:
  - Environmental control
  - Industrial controllers
  - M2M, Smart “X”

**Key Architectural Features:**
- ARM AMBA4 MPCore™ Virtualization
- DDR3L 16-bit with ECC support
- 2-port GigE with IEEE 1588
- 1x PCI Express Gen2
- 4x CAN ports for industrial applications
- EnergyStar support with fast wakeup
- 2Gbps IP forwarding

**Key System Integration Features:**
- Low-cost NAND/NOR flash systems
- Low-cost DRAM systems
- USB2.0
- QorIQ Trust Architecture and ARM TrustZone support
- Alignment with Kinetis/Vybrid portfolio

**Package & Board:**
- Package: 525-pin, 19x19 mm, 0.8 mm ball pitch
- Power: ~2W @ 600 MHz Typical
- Temp: -40C (TA) to 105C (Tj)
- Boards: Tower low-cost board
- Freescale Linux BSPs
LS102xA Core IP
LS102x Family CPU Core Complex and L2 Cache

• Dual ARM Cortex-A7 cores configured as:
  - Up to 1.0 GHz operation
    ▪ Limited to 600 MHz on LS1022
  - 32KB I-cache and 32 KB D-cache per core with ECC protection
  - 512 KB shared L2 cache with ECC protection
  - FPU and NEON VFPv4 (Floating Point Unit) supported
  - CoreSight (on-chip debug and real-time trace) ETM (Embedded Trace Macrocell) supported for debug trace
LS102x Family DDR Memory Controller

- 32-bit Data + 4-bit ECC
  - 16-bit Data + 2-bit ECC, 8-bit Data + 1-bit ECC
  - Only 16-bit Data supported on LS1022
- Operation from 1.0 GHz to 1.6 GHz
- DDR3L (1.35V) and DDR4 (1.25V) supported
  - Only DDR3L supported on LS1022
- 4 chip selects supported
• LS102x supports two different DMA Controllers:
  - Peripheral DMA
    - As used on i.MX and Vybrid
    - Used for relatively low-speed offload of data movement to/from low-speed peripherals (DSPI, LPUART, SAI, ASRC, FlexCAN)
  - QDMA
    - Optimized for high bandwidth to/from DDR and/or PCIe
Power Management: Deep Sleep

• LS102x supports P1022-style Deep Sleep
  – Wake on: RGMII Ethernet, or Timer, or GPIO etc.

• <150mW total SoC power (including IO)
  – Enabling < 0.5W AC system design solutions

• Supports core Dynamic Frequency Scaling (DFS)
  – Same as supported on QorIQ P3/P4/P5 products
Networking & High Speed IO
LS102x PCI Express 2.0 Controller and SERDES

- 2 PCI Express Controllers can support x1/x2/x4 operation
  - For dual PCIe, maximum of 2-lane operation can be supported
  - Only single lane SERDES supported on LS1022
- MSI supported (but not MSI-X)
- USB 3.0 Phy integrates its own dedicated SERDES

### LS102x SERDES Protocol combinations

<table>
<thead>
<tr>
<th>Protocol Options</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCIe x4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>PCIe x2</td>
<td>PCIe x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>PCIe x1</td>
<td>SATA x1</td>
<td>PCIe x2</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PCIe x1</td>
<td>SGMII 1</td>
<td>PCIe x1</td>
<td>SGMII 2</td>
</tr>
<tr>
<td>5</td>
<td>PCIe x1</td>
<td>SATA x1</td>
<td>SGMII 1</td>
<td>SGMII 2</td>
</tr>
<tr>
<td>6</td>
<td>PCIe x2</td>
<td>SATA x1</td>
<td>SGMII 1</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>PCIe x1</td>
<td>PCIe x1</td>
<td>SATA x1</td>
<td>SGMII 1</td>
</tr>
</tbody>
</table>
SATA and USB

- **SATA**
  - Enhanced from previous generation QorIQ products
  - One SATA Gen1/2/3 controller (up to 6.0 GBAud)

- **USB**
  - 1 USB 3.0/2.0 Host/Device/OTG controller with integrated PHY
    - (Up to 5.0GBaud)
  - Additional USB 2.0 Host/Device/OTG controller with ULPI interface to external PHY
    - (Up to 480Mbps)
Code compatible with QorIQ P1 eTSEC

Support for weighted round robin and strict priority queueing

TCP/IP checksum offload for RX and TX

IPv6 and Magic Packet support

RMII Interface Support added

SGMII Interface Support

IEEE1588 Hardware Support

Additional hashing logic to aid in packet distribution

QoS support for 8 Rx and 8 Tx H/W queues, with queues individually assigned to any core

Programmable IP header alignment

Customizable per-packet rejection

Customizable per-packet filtering/filing to 64 logical receive queues. Examples: 802.1p, IP TOS, Diffserv classification, TCP/UDP ports, etc.

Layer 2 features:
- VLAN insertion and deletion per frame
- 16 exact-match MAC addresses
- Increased hash table address matching

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- VLAN insertion and deletion per frame
- 16 exact-match MAC addresses
- Increased hash table address matching
VeTSEC Benefits

- Programmable Protocol classification (5-tuple) for protocols such as IPv4, IPv6 and TCP/UDP
- Offload Checksum operations to accelerate TCP/IP stack performance
- Bandwidth Scheduling - Modified Weighted Round Robin (MWRR) to manage bandwidth allocation for multiple transmit queues
- Programmable quality of service rules per Ethernet port to support differentiated services
- Programmable firewall strategies based on high-level protocol identification
- Virtualization of Interrupts - Interrupts can be steered to any CPU core reducing software overhead and improving performance
- Advanced Hashing logic - Enables load balancing of traffic across CPU cores for improved performance
- Queues can be individually assigned to any CPU core – reduces software and CPU overhead for improved performance.
LS1020/21 QUICC Engine Feature Overview

Protocols and Interfaces
- HDLC/Transparent (bit rate up to 70 Mbps)
- HDLC BUS (bit rate up to 10 Mbps)
- Asynchronous HDLC (bit rate up to 2 Mbps)
- UART
- BISYNC (bit rate up to 2 Mbps)
- Two TDM interfaces supporting 64 multichannels, each running at 64 Kbps

Time Slot Assigner and 2 TDM Interfaces
- Independent Rx and Tx routing RAM with 512 routing entries each
- Time slot assigner with bit or byte resolution
<table>
<thead>
<tr>
<th>Feature</th>
<th>LS1021</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>1280 x 1024 @ 72 Hz</td>
<td>For single plane</td>
</tr>
<tr>
<td></td>
<td>1280 x 768 @ 72 Hz</td>
<td>Up to 2 planes (WXGA)</td>
</tr>
<tr>
<td></td>
<td>1024 x 768 @ 72 Hz</td>
<td>Up to 3 planes</td>
</tr>
<tr>
<td></td>
<td>1024 x 768 @ 60 Hz</td>
<td>Up to 4 planes</td>
</tr>
<tr>
<td>Blending</td>
<td>4-Planes</td>
<td></td>
</tr>
<tr>
<td></td>
<td>α-blend / chroma key</td>
<td></td>
</tr>
<tr>
<td>Input Planes</td>
<td>Sub-Plane selection from 16-layers</td>
<td>DCU blends selected pixels from 16-layers of images based on priority. Only displayed layers’ pixels contribute to input BW.</td>
</tr>
<tr>
<td></td>
<td>Pixel format per layer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Tile Texturing</td>
<td></td>
</tr>
<tr>
<td>Input Plane BW</td>
<td>TBD (higher than P1022)</td>
<td>Limited by internal memory bandwidth assuming fully populated blend planes</td>
</tr>
<tr>
<td>Pixel Formats</td>
<td>32-bit RGB</td>
<td>Transparency α-component used to mix foreground/background colors (gradient). Luminance values add to pixel components below the luminance blend plane (intensity).</td>
</tr>
<tr>
<td></td>
<td>8+8-bit pallete</td>
<td></td>
</tr>
<tr>
<td></td>
<td>YCrCb</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transparency</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Luminance</td>
<td></td>
</tr>
<tr>
<td>Cursor</td>
<td>256xH (8K-pixel)</td>
<td>A blend plane can be used for enhanced cursor support</td>
</tr>
<tr>
<td></td>
<td>1-bit pixel, blinking</td>
<td></td>
</tr>
<tr>
<td>Post-Processing</td>
<td>Gamma Correction</td>
<td>DCU supports dithering to improve color depth and pixel tagging to check tagged input pixels are displayed in blended output</td>
</tr>
<tr>
<td></td>
<td>Component Dithering</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Safety Pixel Tagging</td>
<td></td>
</tr>
<tr>
<td>Display Interface</td>
<td>24-bit RGB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(12-bit DDR pin interface)</td>
<td></td>
</tr>
</tbody>
</table>
Display Controller (DCU)

- Static objects
  - Any memory
- Dynamic objects
  - RAM

DCU
- 16 obj

- Color conv pre blend, RLE exp, 32bpp
- Animate, Alpha, Pos, Obj ...
- Blend Color key, 4 planes
- Dithering Gammar correction CRC check

- Pipelined operation up to 150 MHz pixel clock
- Memory size optimized
- Per obj. any frame rate
LS102x Trust, Virtualization and Security
LS102x Security Architecture Overview (p1/3)

TrustZone
- As per Vybrid and i.MX6
- Hardware compliant to ARM Trusted Base System Architecture (TBSA v1.0)
- Enablement of this will be from customers or ecosystem, not Freescale
- Trusted execution environment for security-critical SW
  - Secure & Normal Worlds (processor modes)
  - Complemented by custom hardware firewalls

QorIQ Trust Architecture Secure Boot
- As per QorIQ P3/P4/P5 Products
- Security library embedded in tamper-proof on-chip ROM
- Authenticated boot: protect against unauthorized SW
  - Verify SW signature during boot
  - RSA-1024/2048 keys anchored to OTP fingerprint (SHA-256)
- Encrypted boot to protect software confidentiality
  - Decrypt SW during boot
  - AES-128/256 keys protected by HW master key (AES-256)
- Run every time SoC is reset
- Image Version Control (on-chip OTP-based)
HW Cryptographic Accelerators
- **Support for wireline protocols, plus Wi-Fi and WiMax,**
  - Not supported: Kasumi, Snow, ZUC, ARC4
  - Symmetric: AES, DES, 3DES, ARC4
  - Hash & HMAC: MD5, SHA-1, SHA-224, SHA-256
  - Hardware random number generator (SP800-90)
  - Export control support

Secure Storage
- Programmable TrustZone protected region within On-chip RAM
- Off-chip storage protected by HW master key (AES-256)

Secure Real-Time Clock
- On-chip, separately-powered real-time clock (1.0V)

HW Firewalls
- Control access from CPU & DMA peripherals to
  - on-chip peripherals
  - on-chip memory
  - off-chip memory
- Integrated with TrustZone
Secure Debug
- Secure Debug Challenge/Response as per QorIQ P3/P4/P5 products

Physical Tamper Detection
- Tamper input signal available for:
  - Cover seal
  - Clock, voltage, temperature detectors
  - Active tamper detection
- Hardware and software tamper response
LS1021 Security Engine Overview

(1) Public Key Hardware Accelerator (PKHA)
- RSA and Diffie-Hellman (to 4096b)
- Elliptic curve cryptography (1024b)
- Supports Run Time Equalization

(1) Random Number Generator (RNG)
- NIST Certified
- RNG supports key generation algorithm

(1) Message Digest Hardware Accelerators (MDHA)
- SHA-1, SHA-2 256,384,512-bit digests
- MD5 128-bit digest
- HMAC with all algorithms

(1) Advanced Encryption Standard Accelerators (AESA)
- Key lengths of 128-, 192-, and 256-bit
- ECB, CBC, CTR, CCM, GCM, CMAC, OFB, CFB, and XTS

(1) Data Encryption Standard Accelerators (DESA)
- DES, 3DES (2K, 3K)
- ECB, CBC, OFB modes

(1) CRC Unit
- CRC32, CRC32C, 802.16e OFDMA CRC

IPsec throughput performance:
- 64B: 0.5 Gbps
- 390B: 1.6 Gbps
- 1456B: 2.1 Gbps
Virtualization Support by S-MMU

• System-MMU for 2nd stage translation of Intermediate Physical Address (IPA) to Physical Address (PA) addresses

• Analogous concept to PAMU (Peripheral Access Mgmt Unit) on QorIQ P3/P4/P5

• Benefits of using System MMU’s for virtualizations are:
  - Full HW Virtualization support (a.k.a. “IO Virtualization”)
  - Better performance than SW virtualization (“Para-Virtualization”)
  - Simpler (thus faster) porting of the Virtualized (“guest”) OS
  - Support for >4GB address space, for 32-bit bus masters

• S-MMU features:
  - Up to 64 TLB entries in TLB cache
  - Address translation in HW, for best performance
  - TLB size configurable, to best suite each master needs
I2C and UART

• I2C
  – 3 instances of I2C as per Kinetis K-series and Vybird F-series
  – Adds DMA offload support compared to previous QorIQ products

• UART
  – 4 instances of 16550-compatible UARTs as per QorIQ P-series
    ▪ 2x 4-wire or 4x 2-wire interfaces
  – 6 instances of high-speed “Industrial” UARTs as per Kinetis L-series
    ▪ Supports RS485 (9-bit multi-drop)
    ▪ Supports up to 3.6 Mbps data rate
    ▪ Supports DMA offload
LS1 Family Use Case Examples
Features Supported

- LCD Touch Display
- Dual 802.11n or ad for LAN
- USB3.0 for storage or Zwave
- SPI for HomePlug Green PHY
- LPUART for ZigBee
- SATA for storage
- SD card for configuration or optional storage
- QSPI for fast serial Flash as alternative
- FPGA/ASIC Fast parallel interface (low latency)
- Console Port
Mobile Wireless Router Application

Features Supported

Connectivity
- Ethernet (GbE) 2x
- 2x PCIe Gen 2 for 802.11n or ad for LAN
- USB 3.0 for 4G/LTE WAN

Local Storage
- SATA 3

Display
- LCD Touch Display (optional)
- LEDs

Debug, Memory
- Console Port
- LCD
- DDR3L/4
- QSPI for fast serial Flash as alternative
- FPGA/ASIC Fast parallel interface (low latency)
MFP (Multifunction printer) Printer Application

- **Connectivity**
  - Ethernet (GigE)
  - USB 3.0 (1 or 2)
  - 802.11 ac/ad Dual band [PCle + I2C + USB]
  - SD

- **Debug**
  - Console port/Ethernet

- **Display**
  - LCD Touch screen
  - ADC

- **Print Engine**
  - FPGA/ASIC
  - Sensors SPI and/or I2C

- **Storage** - SATA
- **FAX** - UART(4-wire)
**Features Supported**

- Console Port
- NOR Parallel Flash (File system and reliability)
- Support for at least 2 Protocols
- At least 2 ports for each protocol interface (redundancy and chaining)
- SPI and I2C for Sensor, EEPROM, display, I/O expansion ......
- FPGA/ASIC Fast parallel interface (Latency is critical)
- Support two protocols at any time
- SD card for storage and configuration
- USB for storage, Control and other protocol support
Industrial Slave Application Example

Features Supported

- Console Port
- NOR Parallel Flash (File system and reliability)
- At least 1 port for each protocol interface but this is high end solution then 2 ports are preferred (redundancy and chaining)
- SPI and I2C for Sensor, EEPROM, display, I/O expansion ......
- FPGA/ASIC Fast parallel interface (Latency is critical)
- SD card for storage and configuration
- USB
PLC Controller Use Case Example

Features Supported

- Console Port
- NOR Parallel Flash (File system and reliability)
- Support for at least 2 Protocols
- At least 2 ports for each protocol interface (redundancy and chaining)
- SPI and I2C for Sensor, EEPROM, display, I/O expansion ......
- FPGA/ASIC Fast parallel interface (Latency is critical)
- Support two protocols at any time
- SD card for storage and configuration
- USB for storage, Control and other protocol support
Features Supported

- Console Port
- NOR Parallel Flash (File system and reliability)
- At least 1 port for each protocol interface but this is high end solution then 2 ports are preferred (redundancy and chaining)
- SPI and I2C for Sensor, EEPROM, display, I/O expansion ..... 
- FPGA/ASIC Fast parallel interface (Latency is critical)
- SD card for storage and configuration
- USB
Deliverables Schedule
(Subject to change)
LS1021A Freescale Deliverables Schedule (subject to change)

Silicon
- Rev1.0 Tapeout
- Rev1.0 Alpha Samples
- Rev1.0 Gen. Avail Samples
- Rev1.1 Tapeout
- Rev1.1 Eng Samples
- Prod. Qual

Software
- QDS BSP Freescale
- Freescale SDK 1.6

Boards
- Alpha QDS Boards
- Proto TWR Boards
- Rev1.0 TWR Boards
- Rev1.1 TWR Boards

Timeline:
- 2013
- Oct, Nov, Dec
- 2014
- Jan
- Q1, Q2, Q3, Q4
- 2015
- Q1, Q2

Freescale "alpha QDS boards" and "proto TWR boards" are used throughout the timeline.
## Current Deliverables

<table>
<thead>
<tr>
<th>LS102xA Family</th>
<th>Version</th>
<th>Availability</th>
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<tr>
<td>SEC Reference Manual</td>
<td>Rev. A</td>
<td>Available now</td>
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<tr>
<td>LS1021A Hardware Spec</td>
<td>Rev. C</td>
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<tr>
<td>LS1021A Product Brief</td>
<td>Rev. A</td>
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- All now available on Extranet folder – QorIQ LS1021A
## LS102x Family Part Numbers

<table>
<thead>
<tr>
<th>Device</th>
<th>Part Number</th>
<th>TEMP</th>
<th>Security</th>
<th>CPU / DDR / QE</th>
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### CPU & DDR

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### Package

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### Prefixes

- Pre-Qual: P
- Qual: (blank)
- Special: S

### Part Numbering Scheme

- **P** = Power
- **L** = LS102x
- **S** = 1
- **1**
- **02**
- **3**
- **A** = ARM
- **X**
- **N**
- **7**
- **P**
- **Z**
- **Z**

- **Qual Status**
  - P = Sampling
  - Blank = Qual

- **# of Cores** (virtual)

- **Generation**
  - S = 1
  - V = 2
  - X = 3

- **Performance Level** (LS1, LS2, LS3)
- **Unique Identifier**
  - *Actively managed

- **Core Type**
  - (P = Power, A = ARM)

- **DDR Speed**

- **Temp**

- **Encryp**
  - (E, N)

- **PKG**

- **Rev**

- **Freq Of core**
LS1021 Enablement Plan
EcoMAP: QorIQ Layerscape Series

<table>
<thead>
<tr>
<th>ARM DS-5</th>
<th>CodeWarrior</th>
<th>Crank Software</th>
<th>Green Hills</th>
<th>Mentor Embedded</th>
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LS1 Software - Board Support Package (BSP)

Early engineering release for QDS board will be available April 1, 2014

Functionality Supported:

- **U-Boot**
  - ARM A7 Core initialization in u-boot
  - DDR (static setting)
  - RCW, Serdes
  - UART
  - FlexTimer in u-boot (2-signals output)
  - PCIe RC, Ethernet(e1000)
  - NOR boot
  - I2C and EEPROM
  - DDR (SPD)
  - SD
  - VeTSEC
  - IFC NAND & NOR (Flash programming)
  - USB 2.0
  - NAND boot
  - SD boot
  - ESBC
  - SATA3
  - DSPI driver

- **Linux**
  - ARM A7 Core initialization in kernel
  - DUART in kernel
  - RAMDISK
  - LPUART
  - I2C controller & I2C EEPROMs
  - WDOG
  - eSDHC (SD)
  - DSPI in kernel
  - eDMA & DMAMUX (Same as in Faraday)
  - QE (UART)
  - Power Management (TMU)
  - PCIe (RC mode)
  - eSDHC (SDIO, SDXC)
  - VeTSEC
  - IFC NAND & NOR
  - USB 2.0 (Host, Gadget mode, OTG)
  - GPIO
  - SATA3.0
  - CAAM
  - FlexCAN

Early engineering release for QDS board will be available April 1, 2014.
Proposed CW-ARM Products for LS1021A

**CW Suite Pro Edition**
- $5500 ($4995/perpetual + $500 probe)
- Trace & Performance Analysis
- CW tools for other processors

**CW-ARM LS1 Edition**
- $1200 ($700 + $500 probe)
- CW-TAP JTAG Probe
- Optional LSCS-lite +$300

**CW-ARM Tower Edition**
- $200 (stops working after 1/2 year)
- Bound to Tower CMSIS-DAP
- on-board JTAG (slow)
- Includes Linux GDB App
LS102x Enablement Boards

QDS Board

• Internal Use, for validation and de-bug support

Tower-based Eval Platform

• Rapid prototyping for Industrial Market:
  • Modular design supports a range of connectivity options
  • Accelerate design & time to market

• Cost-effective, open source development platform
  • Designed to simplify product evaluation
Tower boards now feature OpenSDA debug based on Kinetis-L MCU

- Full size SD slot to support SDIO expansion
- 2\textsuperscript{nd} USB and RS232 serial debug to TWR-SER board

Leverage the MPC830x-TLCD touchscreen display module

Region not covered by mezzanine board

Surface mount lugs for PCIe cards

Dual mPCIe connectors for .11 Wi-Fi cards

Surface mount lugs for PCIe cards

2\textsuperscript{nd} USB and serial header

Vertical SATA connector

mDP to eDP conversion cable
**TWR-LS1021A Kitting Plan**

- **TWR-LS1021A-KIT:**
  - TWR-LS1021A
  - TWR-SER +
  - TWR-ELEV boards

- **TWR-IND-IO**
  - Will be kitted for industrial protocol support
Summary

QorIQ processors continue to drive networking innovation, now bringing over 20 years of networking expertise to ARM processing.

The scalable LS1 family has been optimized for low-power, small-form-factor networking and industrial applications, offering the highest level of integration under 3 W.

Freescale is the first to take the highly-efficient ARM® Cortex®-A7 core into the networking market, delivering enterprise reliability and exceptional performance-per-watt.

Powerful combination of Freescale and ARM ecosystems for best-in-class customer support.

Samples of LS1020A, LS1021A, LS1022A expected to be available Q1 2014.
QorIQ LS1 Backup slides
QorIQ LS1021 Pinout
Low-speed Interfaces

• Audio
  - 4 instances of SAI for I2S support (similar to Vybrid F-series)
• I2C
  - 3 instances of I2C (similar to Kinetis K-series and Vybrid F-series)
• SPI
  - 2 instances of regular SPI (similar to Vybrid F-series)
• Timers and PWM
  - 8 instances of Flextimer (similar to Kinetis K-series and Vybrid F-series)
  - 2 instances of Watchdog timer (similar to i.MX6-series and Vybrid F-series)
  - 2 instances of ARM Generic Timer (one per Cortex-A7)
• UART
  - 2 instances of 16550-compatible UARTs (similar to QorIQ P-series)
  - 6 instances of high-speed “Industrial” UARTs (similar to Kinetis L-series)
• USB
  - 1 USB 2.0 Host/Device/OTG controller with integrated PHY
Low-speed Interfaces (cont.)

- Additional Audio IP (all as per Vybrid F-series)
  - 1 instance of S/PDIF
  - 1 instance of ASRC
- CAN
  - 4 instances of FlexCAN as per Kinetis K-series and Vybrid F-series
- Ethernet
  - 3 VeTSEC controllers supporting 2x1G+1x100Mbit interfaces, with IEEE1588 support as per QorIQ P1020
- QuadSPI
  - 1 instance of QuadSPI as per Vybrid F-series
- QE
  - 2 UCC QUICC Engine featuring a subset of QorIQ P1021 QUICC Engine
- SATA
  - One SATA Gen1/2/3 controller (up to 6.0GBaud)
- SD/MMC
  - 1 controller supporting SD 2.0, SD 3.0, SDIO 2.0 and eMMC 4.5
- SEC
  - Support for IPSec, SSL/TLS, WiFi, WiMax hardware offload.
- USB
  - USB 3.0 operation of the USB 2.0 controller/PHY from previous slide.
  - Additional USB 2.0 controller with ULPI interface to external PHY
LS102x Customer Pinout

- **GVDD**: 89 pins DDR
- **BVDD**: 48 pins external Flash
  - 28-bit address/16-bit data NOR Flash, or
  - 16-bit parallel NAND + 3x 2-channel PWMs,
  - 16-bit parallel NAND + QuadSPI, or
  - 8-bit parallel NAND + QuadSPI + extra regular SPI, or
  - 8-bit parallel NAND
    (with 3rd I2C also available in several of the above options)
- **DVDD**: 8 pins UART
  - 2x 4-wire UART, or
  - 4x 2-wire UART, or
  - 1x 2-wire UART + regular SPI
- **EVDD/DVDD**: 10 pins SD/MMC
  - 8-bit eMMC (no CD or WP)
  - 4-bit SD/MMC/eMMC + 2nd I2C
  - 3 additional UARTs + 2nd I2C

**GPIO is muxed over Most LVCMOS pins**

- **GVDD** = 1.2/1.35V
- **BVDD** = 1.8/3.3V
- **DVDD** = 1.8/3.3V
- **EVDD** = 1.8/3.3V
- **LVDD** = 1.8/2.5/3.3V
- **OVDD** = 1.8V

- **DVDD**: 2 pins I2C
- **OVDD**: 7 pins Interrupts
- **OVDD**: 7 pins Debug
- **OVDD**: 5 pins JTAG
- **OVDD**: 13 pins clock, resets, system control, etc.
LS102x Customer Pinout (cont.)

- **LVDD: 2 pins Ethernet Management**
- **LVDD: 13 pins “EC1”**
  - RGMII, or
  - 2 CAN interfaces, or
  - 8-channel PWM, or
  - 2 I2S Tx/Rx interfaces, or
  - Combinations of the above
- **LVDD: 13 pins “EC2”**
  - RGMII, or
  - 2 additional CAN interfaces, or
  - 8-channel PWM, or
  - USB 2.0 ULPI, or
  - Combinations of the above
- **LVDD: 13 pins “EC3”**
  - RGMII, or
  - IEEE15888, or
  - 8-channel PWM, or
  - I2S with 6 Rx or Tx data lanes and shared frame syncs/clocking
  - Combinations of the above
- **DVDD: 14 pins “QE”**
  - 2 QE UCC engines for HDLC/TDM or PROFIBUS, or
  - 2 I2S Tx/Rx interfaces, or
  - SPDIF, or
  - 8-channel PWM, or
  - LCD Controller Dual Data Rate interface (also eliminates one UART)
QorIQ LS1021 Pinout
Low-speed Interfaces

- **Audio**
  - 4 instances of SAI for I2S support (similar to Vybrid F-series)
- **I2C**
  - 3 instances of I2C (similar to Kinetis K-series and Vybrid F-series)
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  - 2 instances of ARM Generic Timer (one per Cortex-A7)
- **UART**
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  - 6 instances of high-speed “Industrial” UARTs (similar to Kinetis L-series)
- **USB**
  - 1 USB 2.0 Host/Device/OTG controller with integrated PHY
Low-speed Interfaces (cont.)

- Additional Audio IP (all as per Vyrid F-series)
  - 1 instance of S/PDIF
  - 1 instance of ASRC
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  - 1 instance of QuadSPI as per Vyrid F-series
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  - 2 UCC QUICC Engine featuring a subset of QorIQ P1021 QUICC Engine
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  - 16-bit parallel NAND + QuadSPI, or
  - 8-bit parallel NAND + QuadSPI + extra regular SPI, or
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    (with 3rd I2C also available in several of the above options)
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  - 4-bit SD/MMC/eMMC + 2nd I2C
  - 3 additional UARTs + 2nd I2C

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- **DVDD**: 1.8/3.3V
- **EVDD**: 1.8/3.3V
- **LVDD**: 1.8/2.5/3.3V
- **OVDD**: 1.8V

- **DVDD**: 2 pins I2C
- **OVDD**: 7 pins Interrupts
- **OVDD**: 7 pins Debug
- **OVDD**: 5 pins JTAG
- **OVDD**: 13 pins clock, resets, system control, etc.
LS102x Customer Pinout (cont.)

- **LVDD: 2 pins Ethernet Management**
  - **LVDD: 13 pins “EC1”**
    - RGMII, or
    - 2 CAN interfaces, or
    - 8-channel PWM, or
    - 2 I2S Tx/Rx interfaces, or
    - Combinations of the above
- **LVDD: 13 pins “EC2”**
  - RGMII, or
  - 2 additional CAN interfaces, or
  - 8-channel PWM, or
  - USB 2.0 ULPI, or
  - Combinations of the above
- **LVDD: 13 pins “EC3”**
  - RGMII, or
  - IEEE15888, or
  - 8-channel PWM, or
  - I2S with 6 Rx or Tx data lanes and shared frame syncs/clocking
  - Combinations of the above
- **DVDD: 14 pins “QE”**
  - 2 QE UCC engines for HDLC/TDM or PROFIBUS, or
  - 2 I2S Tx/Rx interfaces, or
  - SPDIF, or
  - 8-channel PWM, or
  - LCD Controller Dual Data Rate interface (also eliminates one UART)