Storage Area Network Solutions Based on QorIQ Processors

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Avinash Naidu | Manager, Embedded Software & Systems, Digital Networking Group
Kwok Wu | Head of Embedded Software & Systems, Digital Networking Group

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Agenda

Overview
- Storage Architecture
- Freescale QorIQ Processor Families
- QorIQ Storage Product Mapping

QorIQ Devices for Storage

Benchmarking and Performance Results
- iSCSI - RAID5 (IOMeter) on T4240

T4240 iSCSI Demo
Networks Must Get Smarter, Fast!

The exponential demands of the network infrastructure require a networking architecture designed with software in mind:

- Flexible hardware approach
- Extreme programming flexibility
- Real-time, ‘soft’ control over the network

- SELF HEALING AND RESILIENCE
- Content Delivery Functionality
- EFFECTIVE USE OF “Big Data”

- Trusted Systems
- Software-Defined Networks: On-the-Fly Service Updates, Changes
- Distributed Intelligence
- Service Differentiation Through Quality of Service Tuning
- Security, Advanced Cryptography

- Better Manageability
- MONETIZATION OF SERVICES
- Energy Management
- Truel Systems

Energy Management

The exponential demands of the network infrastructure require a networking architecture designed with software in mind:

- Flexible hardware approach
- Extreme programming flexibility
- Real-time, ‘soft’ control over the network
Realities of the New Virtualized Network

With the Evolving Physics of Networking Implementations …

Next-Generation Networks Must Balance Changing Deployment Paradigms

1. Deployment, configuration, management agility
2. Vendor neutral interoperability
3. Open Standards based

1. Power limitations dominate architectural decisions
2. IO scaling MUCH faster than CPU integration
3. Multicore scaling has reached limits (HW, SW)
QorIQ LS2 Family

Key Features

SDN/NFV Switching

Data Center

Wireless Access

Unprecedented performance and ease of use for smarter, more capable networks

High performance cores with leading interconnect and memory bandwidth
- 8x ARM Cortex-A57 cores, 2.0GHz, 4MB L2 cache, w Neon SIMD
- 1MB L3 platform cache w/ECC
- 2x 64b DDR4 up to 2.4GT/s

A high performance datapath designed with software developers in mind
- 20Gbps Packet processing performance (crypto acceleration, Pattern Match/RegEx, Data Compression)
- New datapath hardware and abstracted acceleration that is called via standard Linux objects
- Management complex provides all init/setup/teardown tasks

Leading network I/O integration
- 8x1/10GbE + 8x1G, MACSec on up to 4x 1/10GbE
- Integrated L2 switching capability for significant cost savings
- 4 PCIe Gen3 controllers, 1 with SR-IOV support
- 2 x SATA 3.0, 2 x USB 3.0 with PHY
LS2085A Smart NIC Reference Designs

- PCIe cards providing enhanced L3/L4+ functionality
  - IPSEC
  - Katsumi
  - TCP offload
  - Compression/decompression
  - Security (SSL/IPsec, SRTP),
  - SDN
  - Software switch
  - SR-IOV I/O virtualization

<table>
<thead>
<tr>
<th></th>
<th>T2080</th>
<th>LS2085A</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Cores</td>
<td>4 (8 threads)</td>
<td>8 A57s</td>
</tr>
<tr>
<td>Frequency</td>
<td>1.2 to 1.8GHz</td>
<td>Up to 2.0GHz</td>
</tr>
<tr>
<td>Worst Case Power</td>
<td>15W-28W</td>
<td>30W TYP</td>
</tr>
<tr>
<td>64 bit DDR cntr</td>
<td>1 DDR3</td>
<td>2 DDR4</td>
</tr>
<tr>
<td>10G Enet I/Fs</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>IPv4fwd</td>
<td>24Gbps</td>
<td>80Gbps</td>
</tr>
<tr>
<td>IPSec</td>
<td>10Gbps</td>
<td>20Gbps</td>
</tr>
<tr>
<td>Data Compression</td>
<td>17.5Gbps</td>
<td>17.5Gbps</td>
</tr>
<tr>
<td>Pattern Matching</td>
<td>10Gbps</td>
<td>10Gbps</td>
</tr>
<tr>
<td>SR-IOV</td>
<td>128 VF</td>
<td>128 VF</td>
</tr>
</tbody>
</table>
Enterprise Class Storage

• Built in for multiple generations – setting the state of the art
• Multicore SoCs with built in acceleration
  – Networking – 40GbE
  – Data Center Bridging
    ▪ Dupe and DeDupe
    ▪ Data address encryption
    ▪ In Line Encryption
  – Pattern Matching Engine
  – Compression

Powerful integrated SoC solutions
## QorIQ T4 Series Key Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>High perf/watt</strong></td>
<td>• 188k CoreMark in 55W = 3.4 CM/W</td>
</tr>
<tr>
<td></td>
<td>• Compare to Intel E5-2650: 146k CM in 95W = 1.5 CW/W;</td>
</tr>
<tr>
<td></td>
<td>• Or: Intel E5-2687W: 200k MC in 150W = 1.3 CM/W</td>
</tr>
<tr>
<td></td>
<td>• T4 is more than 2x better than E5</td>
</tr>
<tr>
<td></td>
<td>• 2x perf/watt compared to P4080, FSL’s previous flagship</td>
</tr>
<tr>
<td><strong>Highly integrated</strong></td>
<td><strong>SOC</strong></td>
</tr>
<tr>
<td></td>
<td>Integration of 4x 10GE interfaces, local bus, Interlaken, SRIO mean that few chips (takes at least four chips with Intel) and higher performance density</td>
</tr>
<tr>
<td><strong>Sophisticated PCIe</strong></td>
<td><strong>capability</strong></td>
</tr>
<tr>
<td></td>
<td>• SR-IOV for showing VMs a virtual NIC, 128 VF (Virtual Functions)</td>
</tr>
<tr>
<td></td>
<td>• Four ports with ability to be root complex or endpoint for flexible configurations</td>
</tr>
<tr>
<td><strong>Advanced Ethernet</strong></td>
<td>• Data Center Bridging for lossless Ethernet and QoS</td>
</tr>
<tr>
<td></td>
<td>• 10GBase-KR for backplane connections</td>
</tr>
<tr>
<td><strong>Secure Boot</strong></td>
<td>Prevents code theft, system hacking, and reverse engineering</td>
</tr>
<tr>
<td><strong>Altivec</strong></td>
<td>On-board SIMD engine – sonar/radar and imaging</td>
</tr>
<tr>
<td><strong>Power Management</strong></td>
<td>• Thread, core, and cluster deep sleep modes</td>
</tr>
<tr>
<td></td>
<td>• Automatic deep sleep of unused resources</td>
</tr>
<tr>
<td><strong>Advanced</strong></td>
<td><strong>virtualization</strong></td>
</tr>
<tr>
<td></td>
<td>• Hypervisor privilege level enables safe guest OS at high performance</td>
</tr>
<tr>
<td></td>
<td>• IOMMU ensures memory accesses are restricted to correct area</td>
</tr>
<tr>
<td></td>
<td>• Virtualization of I/O blocks</td>
</tr>
<tr>
<td><strong>Hardware offload</strong></td>
<td>• Packet handling to 50Gb/s</td>
</tr>
<tr>
<td></td>
<td>• Security engine to 40Gb/s</td>
</tr>
<tr>
<td></td>
<td>• Data compression and decompression to 20Gb/s</td>
</tr>
<tr>
<td></td>
<td>• Pattern matching to 10Gb/s</td>
</tr>
<tr>
<td><strong>3x Scalability</strong></td>
<td>• 1-, 2-, and 3- cluster solution is 3x performance range over T4080 – T4240</td>
</tr>
<tr>
<td></td>
<td>• Enables customer to develop multiple SKUs from on PCB</td>
</tr>
</tbody>
</table>
## QorIQ T4 Series Target Applications

<table>
<thead>
<tr>
<th>Application</th>
<th>Key Features</th>
</tr>
</thead>
</table>
| **Storage**          | • High performance networking  
                        | • Single-chip SOC solution                                                   |
| **Wireless Infrastructure** | • Power architecture for legacy code migration  
                                | • High performance density  
                                | • Kasumi at 20Gb/s  
                                | • Dual x4 SRIO at 5GHz for DSP and backplane                                  |
| **Micro server**     | • High perf/watt  
                        | • Integration leads to higher processing per rack unit  
                        | • Ethernet integration eliminates the NIC  
                        | • Data Center Bridging for rack-to-rack cabling  
                        | • 10Gbase-KR for backplane                                                   |
| iNIC or PCIe offload | • SR-IOV for support of 128 VMs  
                        | • Compression and decompression to 20Gb/s for ADC                           |
| **Mil/Aero**         | • Altivec for legacy code support, > 6x the Altivec performance of 8641D.    |
| **UTM**              | • 40Gb/s IPSEC  
                        | • Deep Packet Inspection offload to 10Gb/s                                  |
| **Data Plane**       | • 48Gb/s 64B packet handling  
                        | • Interlaken Lookaside for TCAM connectivity                                 |
QorIQ T4 Family: Introducing T4080

Now with Value, Mid, and High tier offerings

3x CPU Performance Scaling in One Package

Scalability – Now the T4 family has a one-, two-, and three-cluster solutions. Choose the best fit for the performance requirement.

Pin Compatibility – All T4 family members are pin compatible. Enables customers to develop multiple SKUs from a single PCB

Accelerator Centric – T4080 performance is weighted towards efficient accelerators (security, DPI, data compression), enabling better performance per watt per dollar.

Upgrade from T2080 - choose T4080 for dual memory controllers, more I/O flexibility, higher performance security or Ethernet support, or Interlaken.

Migrate from P4080 - Same 8-thread, 2-FMan programming model, but higher frequency, upgraded I/O, accelerators, packet handling, and DDR controllers, and lower cost.
## Industry’s Most Scalable Processor Portfolio

<table>
<thead>
<tr>
<th></th>
<th>T2080</th>
<th>T4080</th>
<th>T4160</th>
<th>T4240</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU (64b)</td>
<td>e6500</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td># of CPU cores, threads</td>
<td>4, 8 threads</td>
<td>8, 16 threads</td>
<td>12, 24 threads</td>
<td></td>
</tr>
<tr>
<td>Max frequency</td>
<td>1.8GHz</td>
<td>1.67GHz</td>
<td>1.8GHz</td>
<td></td>
</tr>
<tr>
<td>L2 Cache per core</td>
<td>512KB</td>
<td>512KB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Platform Cache</td>
<td>512KB</td>
<td>1MB</td>
<td>1.5MB</td>
<td></td>
</tr>
<tr>
<td>DRAM Interface</td>
<td>1x DDR 64b 3/3L</td>
<td>2x DDR 64b 3/3L</td>
<td>3x DDR 64b 3/3L</td>
<td></td>
</tr>
<tr>
<td>IPFwding perf (small pkt)</td>
<td>24Gbps</td>
<td>24Gbps</td>
<td>36Gpbs</td>
<td>48Gbps</td>
</tr>
<tr>
<td>IPSec perf (large pkt)</td>
<td>14Gbps</td>
<td>32Gpbs</td>
<td>32Gbps</td>
<td></td>
</tr>
<tr>
<td>Max # Ethernet</td>
<td>4x 1/10GbE + 4x 1GbE</td>
<td>2x 1/10 GbE + 14x 1GbE</td>
<td>4x 1/10GbE + 12x 1GbE</td>
<td></td>
</tr>
<tr>
<td>Other High Speed Serial</td>
<td>4x PCIe: Gen 2.0/3.0</td>
<td>4x PCIe: Gen 2.0/3.0</td>
<td>4x PCIe: Gen 2.0/3.0</td>
<td></td>
</tr>
<tr>
<td>Power (typ 65C) at Fmin</td>
<td>11W-1.2GHz</td>
<td>19W-1.5GHz</td>
<td>25W-1.5GHz</td>
<td>30W-1.5GHz</td>
</tr>
<tr>
<td>Pin Compatibility</td>
<td>25x25 mm 896p FCBGA</td>
<td></td>
<td></td>
<td>42.5x42.5mm 1932-pin FCBGA</td>
</tr>
</tbody>
</table>
## T4080 Upgrades Relative to T2080

- Both have the same one cluster, same CPU capability, and same L2, but:

<table>
<thead>
<tr>
<th>Feature</th>
<th>T2080</th>
<th>T4080</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR Contrlr</td>
<td>One</td>
<td>Two</td>
<td>2x the bandwidth, and lower latency due to interleaving</td>
</tr>
<tr>
<td>Corenet Platform Cache</td>
<td>512kB</td>
<td>1MB</td>
<td>Lower latency access for DPAA, higher throughput</td>
</tr>
<tr>
<td>IPSec, 1442B pkt</td>
<td>14Gbps</td>
<td>32Gbps</td>
<td>Higher perf SEC block in T4</td>
</tr>
<tr>
<td>FMan</td>
<td>One</td>
<td>Two</td>
<td>Each Fman has 38Mpps packet handling capability</td>
</tr>
<tr>
<td>SerDes lanes</td>
<td>16</td>
<td>24</td>
<td>More I/O flexibility</td>
</tr>
<tr>
<td>Interlaken LA-1</td>
<td>No</td>
<td>Yes</td>
<td>Supports TCAM for high-perf classification</td>
</tr>
<tr>
<td>Pin compatible devices</td>
<td>T10x0 (T2081)</td>
<td>T4160, T4240</td>
<td>T2081 is pin compatible to lower cost devices, T4080 is pin compatible to higher performance devices</td>
</tr>
</tbody>
</table>
Digital Networking Product Family Progression

- **QorIQ Layerscape**
  - **NEW**
  - Software Driven Core-agnostic

- **QorIQ Qonverge**
  - 2-14 Heterogeneous cores
  - Protocol acceleration

- **QorIQ T-Series**
  - Multi-thread 1-24 cores, 64-bit, Altivec

- **QorIQ P-series**
  - 1-8 cores, packet acceleration, security & pattern matching, hardware-assisted hypervisor

- **PowerQUICC**
  - Industry’s leading Communications Processor

**Platform in Execution**
- 4 family members / 2013
- 6 family members 2013
- 25 family members
- 75 family members

**External Use** | 13
**QorIQ T4240**

**Block Diagram**

Industry’s highest CoreMark score for an embedded SOC

- **Performance-per-watt leadership**
  - 12 dual threaded e6500 cores, 64b
  - 1.8GHz
  - Altivec
  - Inverted cache hierarchy

- **Advanced Power Management**
  - Thermal Management Unit
  - Drowsy power modes

- **Improved Dataplane**
  - 40Gb/s Pkt handling with 64B packets
  - 4x 10GE ports incl XFI/10GBase-KR
  - Datacenter Bridging, Interlaken, HiGig

- **Upgraded Acceleration**
  - Crypto upgraded to 40Gb/s
  - Data Compression Engine to 20Gb/s
  - Pattern matching to 10Gb/s
Layerscape Trust Architecture

Layerscape Trust Arch Dedicated IP
Layerscape Datapath IP with Trust Arch extensions
TrustZone IP
Hardware view of Layerscape
Concept: LS2060A Block Diagram

General Purpose Processing Layer
- 6 x ARM A57 CPUs, 64b, 2.0GHz
  - 2MB L2 cache
- HW L1 & L2 Prefetch Engines
- Neon SIMD in all CPUs
- 4MB L3 platform cache w/ECC
- 2x64b DDR4 up to 2.4GT/s

Accelerated Packet Processing Layer
- 10Gbps SEC- crypto acceleration
- 10Gbps Pattern Match/RegEx
- 10Gbps Data Compression Engine

Express Packet IO Layer
- Supports1x8, 4x4, 4x2, 6x1 PCIe Gen3 controllers
- SR-IOV support, Root Complex
- PCIe Interworking to LSDPAA via PEXMan
- 2 x SATA 3.0, 2 x USB 3.0 with PHY
- Network IO
- Wire Rate IO Processor:
  - 8x1/10GbE + 8x1G
  - XAUI/XFI/KR and SGMII
  - MACSec on up to 4x 1/10GbE

Datapath Acceleration
- SEC- crypto acceleration
- DCE - Data Compression Engine
- PME – Pattern Matching Engine
Concept: LS3280A Block Diagram

![Diagram showing LS3280A block diagram with various components like ARM A57, ARM A57, SEC, DCE, PME, L2 Switching, AIOP, SEC, DCE, Pattern Matching Engine, and so on.]

**Datapath Acceleration**
- SEC - crypto acceleration
- DCE - Data Compression Engine
- PME - Pattern Matching Engine
- L2 Switching
- AIOP - Advanced IO Processing

**General Purpose Processor Layer**
- 12 x ARM A57 CPUs, 64b, 2.0GHz
  - 2MB L2 cache/2 CPU cluster
- 16 x ARM A53 CPUs, 64b, 1.2GHz
  - 1MB L2 cache/4 CPU cluster
- HW L1 & L2 Prefetch Engines
- Neon SIMD in all CPUs
- Memory & Cache Coherent Interconnect
  - Platform/L3 Cache up to 8MB w/ECC
  - 4x DDR4 Controllers up to 2.4GT/s
  - Up to 1TB addressability

**Accelerated Packet Processing Layer**
- 80Gbps AIOP
- 80Gbps SEC- crypto acceleration
- 40Gbps Pattern Match/RegEx
- 40Gbps Data Compression Engine

**Enhanced Packet Processing Layer**
- Supports 6 PCIe Gen3 controllers
- SR-IOV support, Root Complex
- PCIe Interworking to LSDPAA via PEXMan
- 2 x SATA 3.0, 2 x USB 3.0 with PHY
- Network IO
- Wire Rate IO Processor:
  - 4x40 or 16x10GbE
  - XAUI/XFI/KR and SGMII
  - MACSec
Storage Architecture Overview

Network Attached Storage (NAS)

SAN
- Ethernet Switch
- iSCSI Storage
- FibreChannel over Ethernet (FCoE) Storage
- FibreChannel Storage (FC)

FibreChannel Switch

CONVERGED NETWORK ADAPTERS (CNA)

Storage Appliance

Network Interface Card (iNIC)

10G

10G

10G

10G

10G

10G

Direct Attached Storage (DAS)
Via Serial Attached SCSI (SAS)
High Performance Computing Environments
10 processors one hop away

10 x 24 = 240 Vcores

RapidIO switching
Bandwidth = 500 Gbps

Zero CPU overhead for Ethernet packet forwarding

Scalable thru backplane switches

Processor to Processor Ethernet forwarding latency ~ µSeconds

Lower power and Lower cost than Ethernet switching

Sub-microsecond chip to chip latency!
**QorIQ Processing Platforms**

<table>
<thead>
<tr>
<th>Platform</th>
<th>Description</th>
<th>Applications</th>
</tr>
</thead>
</table>
| P5021, P5040, P5010, P5020 | High performance control plane processing  
- Up to 2.4 GHz  
- Large L2 caches | Service Provider Routers, Fabric Controller, Storage Networks |
| T4240, T4160, T4080, P4080, P4040, P3041 | Mixed control and data plane processing  
- Up to 1.8 GHz  
- Highly parallelized workloads  
- Data off-load acceleration | Metro Carrier Edge Router, Aerospace & Defense, Datacenter/Network Services |
| T1040, T2080, P101x(8), P102x(5), P2x(4) | Optimal performance to power ratio  
- Up to 1.6 GHz  
- Less than 10W  
- Broadest portfolio of power-efficient SoCs | Integrated Services Router, Network Attached Storage, Media Gateway |
Freescale SoC Storage/Gateway Solutions

Relative Performance

I/O & Features

P2041
1-4 cores, e500mc
To 1.5 GHz
~15W

Multi-Core High Performance NAS w/ 10GbE Controllers

P50X0
1-4 cores, e5500
To 2.2 GHz
22-35W

Multi-Core High Performance SAN & CNA w/ 10GbE & RAID5/6

T2xxx /T4xxx
8 - 24 threads, e6500
To 1.8 GHz
11 - 37W

Highest Performance
SAN, CAN w/ multiple 10GbE
Processors for Storage Area Networks (SAN)  
Converged Network Adaptors (CNA)

**Example QorIQ Processor Solution**

- **P5040**
  - Quad-core / Dual-core up to 2.2GHz
  - 512KB L2 per core, 2MB L3
  - Dual DDR3/3L 64-bit interfaces
  - Gen 2 PCI-Express – 4 controllers
  - 2 SATA 3Gbps
- **P5020**
  - Single-core pin-compatible option available (P5010).
  - Supports RAID5 / RAID6 parity engine:
    - Dual parity generation in single pass
    - Block sizes of 512B, 1KB, 2KB and 4KB

**Requirements for Management Processors**
- Similar requirements as switching platforms

**Requirements for Storage Data Path Processors**
- Multi-core at 1.5GHz or higher
- RAID 5/6 acceleration
- PCI-Express Gen2

**P5020 w/ HW Assisted RAID**

- Quad-core / Dual-core up to 2.2GHz
- 512KB L2 per core, 2MB L3
- Dual DDR3/3L 64-bit interfaces
- Gen 2 PCI-Express – 4 controllers
- 2 SATA 3Gbps
- Single-core pin-compatible option available (P5010).
- Supports RAID5 / RAID6 parity engine:
  - Dual parity generation in single pass
  - Block sizes of 512B, 1KB, 2KB and 4KB
Benchmarking and Performance Results
Storage Solutions Using T4240
T4240 as a Storage Controller in a 40Gb/s SAN

T4240
• Highest CoreMark/W
• 24 virtual cores
• 50Gb/s packet handling
• Hardware virtualization
• Advanced power management

• T4240 is iSCSI target
• T4240 implements RAID5 array, accelerator calculates parity
• Receives reads and writes from iSCSI initiator (server)
• T4240 reads/writes SCSI blocks to eight solid-state disks

Demo
T4240 as Storage Controller
40Gb/s bidirectional traffic at line rate

**iSCSI initiator**
HP Server w/ 10G NIC

**iSCSI target**
T4240

- T4240 builds RAID storage array
- T4240 runs SCSI over Ethernet (one XAUI used, three more available)
- T4240 receives read and write commands and write data from iSCSI initiator (server)
- Security accelerator calculates XOR for RAID5 parity
- T4 sends and receives SCSI block to HBA
- T4 sends read data to server
- Full line rate achieved

**Diagram:**
- PCIe x4 LSI HBA
- 8x OCD Vertex3 SSD Drives - 6 Gbps/Drive
- XAUI
- 10G Patch Cables
- Rd/wr cmd/data
- IOMeter measures read and write performance
- x4 Gen2 PCIe at line rate
- Block Storage I/O

**Legend:**
- T4240
- HP Server w/ 10G NIC
- PCIe x4 LSI HBA
- 8x OCD Vertex3 SSD Drives - 6 Gbps/Drive
- XAUI
- 10G Patch Cables
T4240 Storage Demo Configuration

Hardware:
- T4240QDS (1.67GHz/ 16000MT/s)
- LSI PCIe 2.0 SAS 9211-4i HBA
  - (four-port 6Gb/s SATA+SAS HBA)
- OCZ Vertex3 SATA III Solid State Drive (SSD) 6 Gb/s
- Intel E10G42BT X520-T2 10Gigabit NIC
- HP ProLiant G6 Tower Server

Software on T4240:
- iSCSI-SCST v2.2 Target
- LVM2
- Linux 3.0.51

Software on Server:
- Windows 7 Professional Edition (32bit)
- Iometer
- Microsoft iSCSI initiator
- Windows Disk Manager
- Iometer - Dynamo
- DU Meter – bandwidth monitor

8x OCD Vertex3 SSD Drives - 6 Gbps/Drive

10G Patch Cable

HP Server w/ 10G NIC

x4 Gen2 PCIe - at line rate

PCle x4 LSI HBA

PCle x4 LSI HBA
QorIQ T4240

- Industry’s highest CoreMark score for an embedded SOC
- Performance-per-watt leadership
  - 12 dual threaded e6500 cores, 64b
  - 1.8GHz
  - AltiVec
  - Inverted cache hierarchy
  - Virtualization
- Advanced Power Management
  - Thermal Management Unit
  - Drowsy power modes
- Improved Dataplane
  - 40Gb/s Pkt handling with 64B packets
  - 4x 10GE ports incl XFI/10GBase-KR
  - Datacenter Bridging, Interlaken, HiGig
- Upgraded Acceleration
  - Crypto upgraded to 40Gb/s
  - Data Compression Engine to 20Gb/s
  - Pattern matching to 10Gb/s

Data Path Acceleration Architecture
Networking – 40GbE
Data Center Bridging
Dupe and DeDupe
Data address encryption
In Line Encryption
Pattern Matching Engine
Compression
T4240 ISCSI – Storage Area Network (SAN) Implementation

• iSCSI: **Internet Small Computer System Interface**, an internet Protocol (IP)-based storage networking standard for linking data storage facilities, enabling location independent data storage and retrieval

• Can be used to transmit data over local area networks (LANs), wide area networks (WANs), or the Internet
T4240 iSCSI – Target & Initiator

• Typical System has iSCSI Target and Initiator

• T4240 SAN system uses the iSCSI-SCST Target implementation (SCST -SCSI target subsystem for Linux)

• Supported in kernel 3.0.6, mature target better performance
• Considering open-source Unified Target in Linux (LIO/TCM) as updated kernel versions become available on 5020

• iSCSI Initiator:
  – On Windows using the Microsoft iSCSI Initiator
  – On Linux Open iSCSI can be used
iSCSI SAN: Hardware & Software Configuration – iSCSI Target

- Reset Configuration Word (RCW) to support 2 PCIe X4 slots
- Ensure the Kernel configuration enables:
  - FMAN Resource allocation algorithm (turned ON)
  - RAID Engine is turned ON
  - Huge TLB Support
  - Jumbo frame support
- SW2 Setting: 10100001 (0=OFF, 1=ON) (0=OFF, 1=ON)
- XAUI Riser Card (10G)
- Two LSI PCIe 2.0 SAS 9211-4i HBA Cards support connecting four drives each
- Eight OCZ Vertex 3 SATA III Solid State Drive (SSD) 6 Gb/s
- One Cat 6e – 10G Patch Cable
T4240 iSCSI SAN: Hardware & Software Configuration –
iSCSI Initiator

- Intel Xeon E5620 2.40GHz 6GB or Better
- Intel E10G42BT X520-T2 10Gigabit NIC with Jumbo frames support – enabled
- Microsoft iSCSI Initiator
- Disk Management Tools
- DU Meter – Bandwidth manager
T4240 iSCSI SAN - Benchmarking

• Create RAID 5 array using the Linux ‘mdam’ utility
  – 8 drives are partitioned by 2
  – Tunable attributes:
    ▪ block size
    ▪ file size
    ▪ stride
    ▪ stripe-width
    ▪ read-ahead-cache

• Use EXT 4 file system
• SCST admin to create the iSCSI target as a virtual disk to be accessed in fileio mode
• Enable the 10G port on the P5020/40 now the iSCSI target is available to the initiator
T4240 iSCSI SAN - Benchmarking

• Connect the 10G ports on the P5020/40 & Win 7 Intel Initiator machine with a Cat 6e cable
• Ensure the latest driver for the Intel Server adapter is installed (May 2012)
• Launch the iSCSI initiator on the Win 7 machine
  − Detects the drives on the P5020/40 SAN as network drives
• Using the Disk Management tool format all the disks
• Launch the DU Meter (bandwidth measurement tool)
• Launch the Iometer tool
  − Set for 64Kb transfer size
  − Set Sequential Read & Writes access specifications
  − Set 10 workers for 2 minute test runs
T4240 Iometer SAN Read – 1226 MBps at Line Rate 10Gbps
T4240 Iometer SAN Write – 1226 MBps at Line Rate 10Gbps
T4240 (Rev 1) – 12 cores/12 threads
SAN throughput by Targets and by DDR memory

<table>
<thead>
<tr>
<th>T4240 (Rev 1)</th>
<th>12GB RAM</th>
<th>6GB RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>60%Read/40%WRITE</td>
<td>1220</td>
<td>1153</td>
</tr>
<tr>
<td>MBps</td>
<td>135,300</td>
<td>130,600</td>
</tr>
</tbody>
</table>

**MBps (12GB vs 6GB RAM)**

<table>
<thead>
<tr>
<th>T=8 (80%)</th>
<th>T=7 (78%)</th>
<th>T=6 (75%)</th>
<th>T=5 (68%)</th>
<th>T=4 (63%)</th>
<th>T=3 (53%)</th>
<th>T=2 (45%)</th>
<th>T=1 (20%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1220</td>
<td>1170</td>
<td>1120</td>
<td>960</td>
<td>930</td>
<td>810</td>
<td>600</td>
<td>400</td>
</tr>
</tbody>
</table>

**IOPs**

<table>
<thead>
<tr>
<th>T=8 (80%)</th>
<th>T=7 (78%)</th>
<th>T=6 (75%)</th>
<th>T=5 (68%)</th>
<th>T=4 (63%)</th>
<th>T=3 (53%)</th>
<th>T=2 (45%)</th>
<th>T=1 (20%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>135,300</td>
<td>130,600</td>
<td>120,000</td>
<td>110,000</td>
<td>102,000</td>
<td>93,000</td>
<td>81,000</td>
<td>60,000</td>
</tr>
</tbody>
</table>

**MBps by # Targets on T4240 (Rev 1)**

<table>
<thead>
<tr>
<th>Targets</th>
<th>MBps</th>
<th>CPU utilization (12 threads)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>1,220</td>
<td>80%</td>
</tr>
<tr>
<td>7</td>
<td>1,170</td>
<td>78%</td>
</tr>
<tr>
<td>6</td>
<td>1,120</td>
<td>75%</td>
</tr>
<tr>
<td>5</td>
<td>960</td>
<td>68%</td>
</tr>
<tr>
<td>4</td>
<td>930</td>
<td>63%</td>
</tr>
<tr>
<td>3</td>
<td>810</td>
<td>53%</td>
</tr>
<tr>
<td>2</td>
<td>600</td>
<td>45%</td>
</tr>
<tr>
<td>1</td>
<td>400</td>
<td>20%</td>
</tr>
</tbody>
</table>

**MBps Throughput by Targets**
**T4240 (Rev 1) – 6 cores/12 threads vs 12 cores/24 threads**

SAN throughput by Targets and by DDR memory

<table>
<thead>
<tr>
<th>MBps (8 Targets/16 workers)</th>
<th>Write</th>
<th>Read</th>
<th>60%Read/40%Write</th>
<th>CPU Util</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 cores/12 threads (CPU 88%)</td>
<td>800</td>
<td>1200</td>
<td>1040</td>
<td>88%</td>
</tr>
<tr>
<td>12 cores/12 threads (CPU 80%)</td>
<td>940</td>
<td>1212</td>
<td>1220</td>
<td>80%</td>
</tr>
<tr>
<td>12 cores/24 threads (CPU 67%)</td>
<td>1025</td>
<td>1212</td>
<td>1270</td>
<td>67%</td>
</tr>
</tbody>
</table>

![Graph showing performance comparison](chart.png)
T4240 (Rev 1) – CPU Frequency @1.67GHz vs @1.5GHz SAN throughput by Targets and by DDR memory

<table>
<thead>
<tr>
<th>MBps (8 Targets /16 workers)</th>
<th>Write</th>
<th>Read</th>
<th>60%Read/40%Write</th>
<th>CPU Util</th>
<th>Power Consump</th>
</tr>
</thead>
<tbody>
<tr>
<td>@1.5GHz 12 cores/24 threads (CPU 58%)</td>
<td>925</td>
<td>1210</td>
<td>1327</td>
<td>58%</td>
<td>33watts</td>
</tr>
<tr>
<td>@1.67GHz 12 cores/24 threads (CPU 56%)</td>
<td>1200</td>
<td>1490</td>
<td>1450</td>
<td>56%</td>
<td>35watts</td>
</tr>
</tbody>
</table>

![Graph showing SAN throughput by Targets and by DDR memory at 1.5GHz and 1.67GHz]

- 1.5GHz (CPU 58% 33watts)
- 1.67GHz (CPU 56% 35watts)
## T4240 (Rev 2) Performance

<table>
<thead>
<tr>
<th>Operation</th>
<th>Performance</th>
<th>CPU</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>READ</strong> 100% Sequential / 256 K</td>
<td>1345 MB/s</td>
<td>45%</td>
<td>26W</td>
</tr>
<tr>
<td><strong>Write</strong> 100% Sequential / 64 K</td>
<td>1072 MB/s</td>
<td>66%</td>
<td>28W</td>
</tr>
<tr>
<td><strong>60% READ 40% Write</strong> 100%</td>
<td>1178 MB/s</td>
<td>42%</td>
<td>27W</td>
</tr>
</tbody>
</table>
T4240 (Rev1, 1.67GHz, DDR3 1600) SAN Storage Controller

(Current System setup)

- T4240 builds RAID storage array
- T4240 runs SCSI over Ethernet (one XAUI used, three more available)
- Hardware offload for Ethernet packet handling
- T4240 receives read and write commands and write data from iSCSI initiator (server)
- Security accelerator calculates XOR for RAID5 parity
- T4 sends and receives SCSI block to HBA
- T4 sends read data to server
- Full line rate achieved

**iSCSI initiator**

HP Server w/ 10G NIC

1x 10G Rd/wr cmd/data

10G Patch Cables

**T4240 (6 cores/12 threads & 12 cores /24 threads)**

- **iSCSI target s**
  (ran with 1 to 8 targets)

1x 10G

10G Patch Cables

**PCIe x4 LSI HBA**

**PCIe x4 LSI HBA**

**8x OCD Vertex3 SSD Drives - 6 Gbps/Drive**

IOMeter measures read and write performance:
reports 1.2GB/s

**Block Storage I/O**

**iSCSI target s**

**PCIe x4 LSI HBA**
Networks Must Get Smarter, Fast!

The exponential demands of the network infrastructure require a networking architecture designed with software in mind:

- Flexible hardware approach
- Extreme programming flexibility
- Real-time, ‘soft’ control over the network
Digital Networking Software and Services

- **World-Class Technology**
  - Freescale Silicon - Used in Leading Products
  - Freescale Enablement – Innovative Investment
    - Device Drivers – Optimized and Portable
    - Linux – Commercial-grade, Available
    - Solutions References – Near-market Ready
    - CodeWarrior – Commercial Tools

- **World-Class Ecosystem**

- Complemented by **Commercial Capability**
  - Freescale Networking Software and Services
    - Commercial Software – VortiQa Applications
    - Commercial Services – Linux Support and Services
Agenda

Overview

• Storage Architecture
• Freescale QorIQ Processor Families
• QorIQ Storage Product Mapping

QorIQ Devices for Storage

Benchmarking and Performance Results

• NAS - RAID5 (Robocopy) on P1, P2
• iSCSI - RAID5 (IOMeter) on T4240

T4240 i.SCSI Demo
Introducing The
QorIQ LS2 Family

Breakthrough, software-defined approach to advance the world’s new virtualized networks

New, high-performance architecture built with ease-of-use in mind
Groundbreaking, flexible architecture that abstracts hardware complexity and enables customers to focus their resources on innovation at the application level

Optimized for software-defined networking applications
Balanced integration of CPU performance with network I/O and C-programmable datapath acceleration that is right-sized (power/performance/cost) to deliver advanced SoC technology for the SDN era

Extending the industry’s broadest portfolio of 64-bit multicore SoCs
Built on the ARM® Cortex®-A57 architecture with integrated L2 switch enabling interconnect and peripherals to provide a complete system-on-chip solution
QorIQ LS2 Family
Key Features

SDN/NFV
Switching

Data
Center

Wireless
Access

Unprecedented performance and ease of use for smarter, more capable networks

High performance cores with leading interconnect and memory bandwidth
- 8x ARM Cortex-A57 cores, 2.0GHz, 4MB L2 cache, w Neon SIMD
- 1MB L3 platform cache w/ECC
- 2x 64b DDR4 up to 2.4GT/s

A high performance datapath designed with software developers in mind
- New datapath hardware and abstracted acceleration that is called via standard Linux objects
- 40 Gbps Packet processing performance with 20Gbps acceleration (crypto, Pattern Match/RegEx, Data Compression)
- Management complex provides all init/setup/teardown tasks

Leading network I/O integration
- 8x1/10GbE + 8x1G, MACSec on up to 4x 1/10GbE
- Integrated L2 switching capability for cost savings
- 4 PCIe Gen3 controllers, 1 with SR-IOV support
- 2 x SATA 3.0, 2 x USB 3.0 with PHY
See the LS2 Family First in the Tech Lab!

4 new demos built on QorIQ LS2 processors:

- Performance Analysis Made Easy
- Leave the Packet Processing To Us
- Combining Ease of Use with Performance
- Tools for Every Step of Your Design