Memory Controller

Purpose:

- The memory controller consists of three types of interface generation. This module is a primer for in-depth looks at the different interfaces used in the PowerQUICC II processor.

Objectives:

- In completing this section, you will have a basic understanding of the three memory interfaces utilized by the memory controller: Standard chip select generation for SRAM, ROM and basic devices only requiring a chip select. An SDRAM controller specifically for providing the correct memory control signals, connections, and timing for SDRAM devices.

Contents:

- This module gives you a block diagram overview of the memory controller as well as the basic operation and finishes with an in depth look at the registers. Each of the interfaces are covered in subsequent sections.

Learning Time:

- There are 16 pages and 6 reference pages which will take approximately 27 minutes.

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Features

- The memory controller consists of three types of interface generation :
  - Standard chip select generation for SRAM, ROM etc..
  - SDRAM controller
  - User programmable machine for other types
- Both local and 60x Bus use the memory controller
- Multiple Parity options available

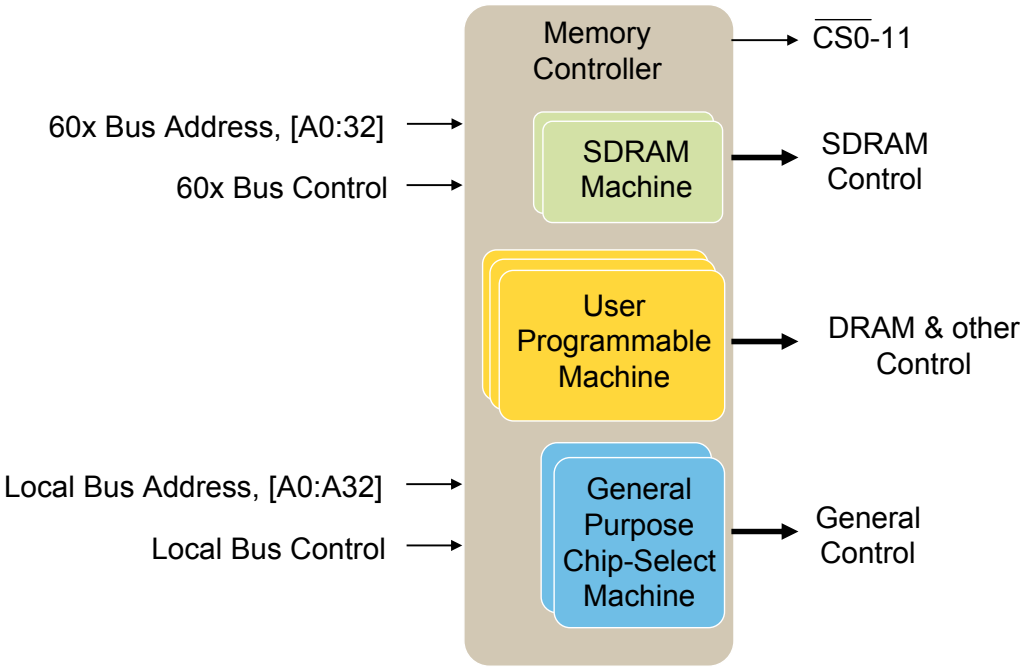
The memory controller consists of three types of interface generation:

Standard chip select generation for SRAM, ROM and basic devices only requiring a chip select. An SDRAM controller specifically for providing the correct memory control signals, connections, and timing for SDRAM devices.

And the User Programmable Machine for user defined control signals used for SDRAM and other types of memory. Both local and 60x bus use the memory controller and so there are separate controls for both. Multiple parity options available.

Block Diagram

- The memory controller handles a maximum of 12 memory banks shared between a general-purpose chip-select machine, three user-programmable machines, and an SDRAM machine.

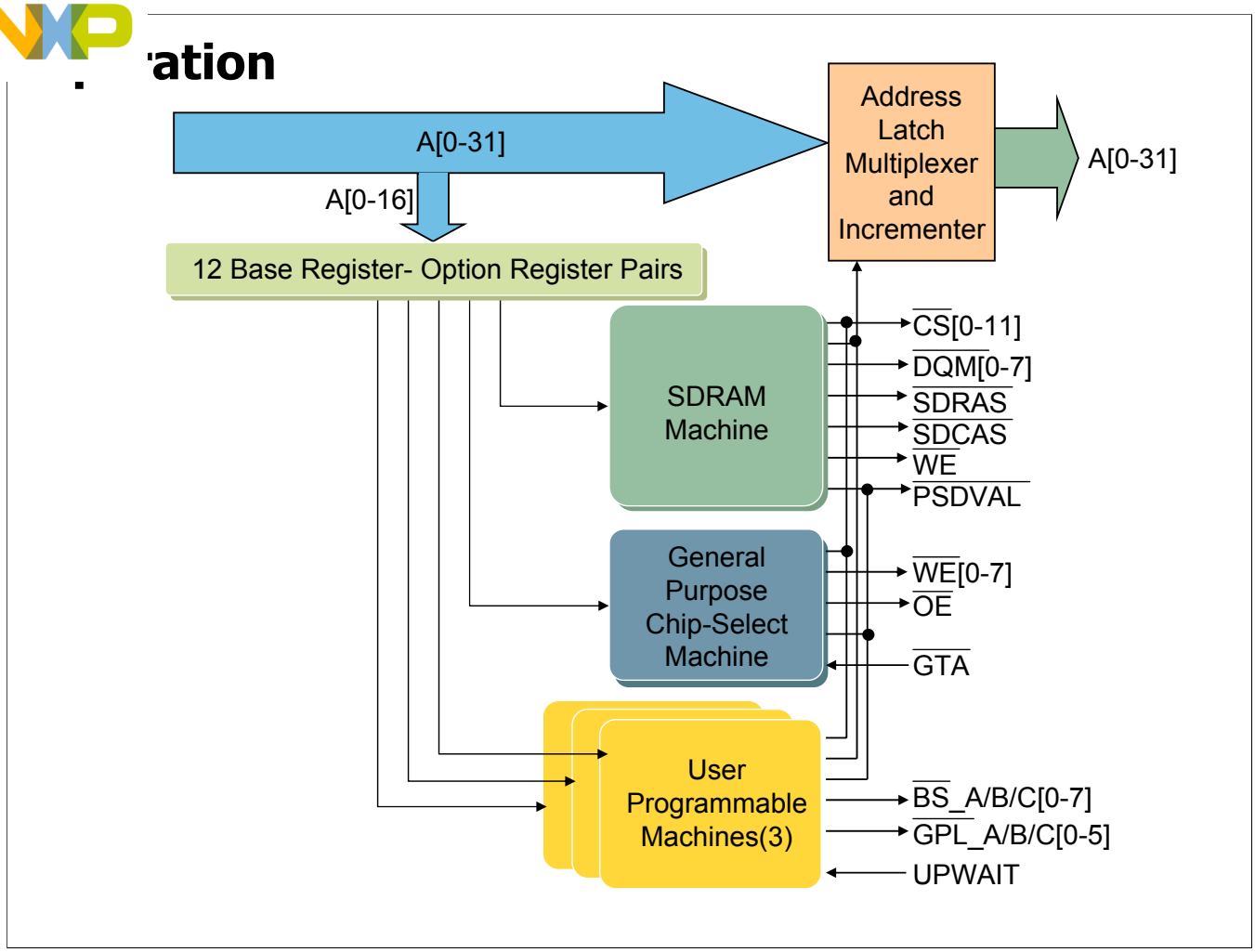


The memory controller handles a maximum of 12 memory banks shared between a general-purpose chip-select machine, three user-programmable machines, and an SDRAM machine. The bus activity generated by the internal CPU and peripherals does not, by itself, enable direct transfer of data between the external memory or peripherals, because the external devices require a transfer protocol different from either the 60x bus or local bus.

Unfortunately not all external devices require the same protocol, and so the memory controller provides the means to generate the required transfer signals. For the simpler requirements such as static RAM, ROM, simple peripherals, etc, the general purpose chip select machine will generate chip select signals within the range of addresses required.

The SDRAM controller will provide the necessary signals and address configuration required for the popular SDRAM memory devices. The user programmable machines allow the user to generate a programmable series of signals on several pins, providing the ability to control a variety of external memory or peripheral devices.

This mix of machines provides the ability to control most types of memory with up to five different types of device over twelve different memory banks, on two different busses.



This diagram shows the basic functions available for the memory controller. When an internal address is generated, the upper 17-bits of the address are used to define the memory block it relates to. This means that the minimum size of a block of memory is 32-kilobytes. There are 12 pairs of registers designated base and option register.

The upper address bits are compared with the value in the base registers in association with the bank size defined in the option registers. If there is a match with one of the pairs then the machine selected for that bank is used to control the data transfer. All machines control the chip select lines, and partial data valid signals.

The SDram machine controls data qualifier, row and column address strobes, and write enable. The general purpose chip select machine controls write enable, and output enable signals, and accepts a termination signal. Each user programmable machines control byte select and general purpose lines, and accepts a wait signal.

When a bank requires general-purpose chip-selects, the appropriate chip select is asserted with the relevant enable signals. When a bank requires to access SDRAM the SDRAM machine controls the transfer as defined by the machine set-up. When a bank requests the use of a UPM the control signals will be generated as programmed into the UPM control memory. Because there are three UPM‘s, then three different control variations are possible.

The SDRAM and UPMs all have refresh timers for regular memory refresh cycles. There are actually two SDRAM machines and two general purpose machines, but one of each is used for the 60x bus and the other for the local bus and only one of each machine is available for each bus. Each machine works independently.

Memory Control Pins (1 of 3)

Local or 60x Bus Accesses:

- $\overline{\text{CS}}$[0-11] - chip select pins
- $\overline{\text{PSDVAL}}$ - data valid pin
- BADDR[27-31] - burst address pins

60x Bus Mode Accesses Only:

- ALE - external address latch
- SDAMUX - external address mux control
- BNKSEL[0:2] - provides internal-bank-select to allow internal bank interleaving in 60x compatible mode.
- BCTL[0-1] - buffer control pins for the 60x data bus.

There are memory control pins for both the 60x bus and local bus, but since the 60x bus has more functionality then there are additional signals available for it. Both busses have chip select, partial data valid and burst address signals. The 60x bus additionally has an address latch, external address multiplex control, three bank selects for bank interleaving in 60x compatible mode and two data buffer control signals.

These are required, for multiple external bus masters are used. PSDVAL indicates that a data transfer beat completed successfully. Note that SDVAL must be asserted for each data beat a single beat and burst transaction. SDAMUX controls an SDRAM address multiplexer when the PowerQUICC II is in external master mode. ALE controls an external latch used for external masters. BCTL signals control data buffers. Their exact function is determined by the SIU module configuration register.

Memory Control Pins (2 of 3)

60x Bus Pin	Local Bus Pin	Description
PGTA	LGTA	GPCM transfer acknowledge pin
POE	LOE	GPCM output enable pin
PWE[0-7]	LWE[0-3]	GPCM write enable pins
PUPMWAIT	LUPWAIT	UPM wait pin
PGPL[0-5]	LGPL[0-5]	UPM general purpose pins
PBS[0-7]	LBS[0-3]	UPM byte select pins
PSDDQM[0-7]	LSDDQM[0-3]	SDRAM byte lane select pins
PSDA10	LSDA10	SDRAM control pin
PSDWE	LSDWE	SDRAM write enable pin
PSDCAS	LSDCAS	SDRAM CAS
PSDRAS	LSDRAS	SDRAM RAS
PSDAMUX	-	SDRAM address multiplexer
BNKSEL[0-2]	-	SDRAM Bank select
ALE	-	Address latch enable for external latch
BADDR[27-31]	-	Burst address for external master mode
BCTL[0-1]	-	Buffer control
-	LWR	Local write pin
PPBS	LPBS	Data parity chip byte select

This chart indicates the memory control signals available on both busses, showing their designation and description. As you can see, in most cases the same signals are available for both, but in the case of the local bus there are fewer write enable, byte select, and byte lane select signals because it only has a maximum of 32-bits on the data bus. The 60x bus can have up to 64-bits.

Memory Control Pins (3 of 3)

Direction	pin options
O	**CS[0-9]**
I/O	**CS[10] / BCTL1**
I/O	**CS[11]** / AP[0]
O	**POE / PSDRAS / PGPL2**
O	**LOE / LSDRAS / LGPL2**
O	**PWE[0-7] / PSDDQM[0-7] / PBS[0-7]**
O	**LWE[0-3] / LSDDQM[0-3] / LBS[0-3]**
I/O	**PGTA / PUPMWAIT / PGPL4 / PPBS**
I/O	**LGTA / LUPMWAIT / LGPL4 /LPBS**
O	**PSDA10 / PGPL0**
O	**LSDA10 / LGPL0**
O	**PSDWE / PGPL1**
O	**LSDWE / LGPL1**
O	**PSDCAS / PGPL3**
O	**LSDCAS / LGPL3**
O	**PSDAMUX / PGPL5**
O	**LGPL5**

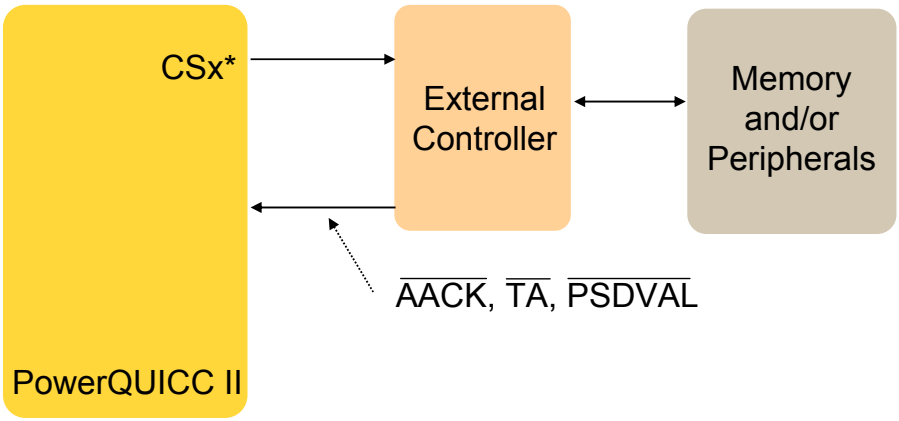
Direction	pin options
O	**BCTL0**
O	**ALE**
O	**BADDR[27-28]**
O	**BADDR29**/ CI / IRQ2
O	**BADDR30**/ WT / IRQ3
O	**BADDR31**/ CPU_BG / IRQ5
I/O	**BNKSEL**[0]/ AP[1] / MODCK1
I/O	**BNKSEL**[1]/ AP[2] / MODCK2
I/O	**BNKSEL**[2]/ AP[3] / MODCK3

This shows the pin availability, and the optional functions for sharing, as well as the signal direction for each. It must be remembered that in many cases pins are shared by different functions and so in those cases the necessary port control programming must be performed. Most of these pins are multi-purpose with the exception of the following.

Ten chip select pins are stand alone, as is the buffer control, address latch enable, and burst address 27 and eight. All of the rest are shared. However, the majority of the rest are shared by the memory controllers and since only one is active at any time, the pin takes on the relevant signal for the controller in use. Those are the ones shown in bold text. The others must be programmed as required by the SIU module configuration register.

Extended Memory Control

- EMEMC allows the memory controller to turnover control of accesses to an external memory controller. The Machine Select field of BRx is ignored.



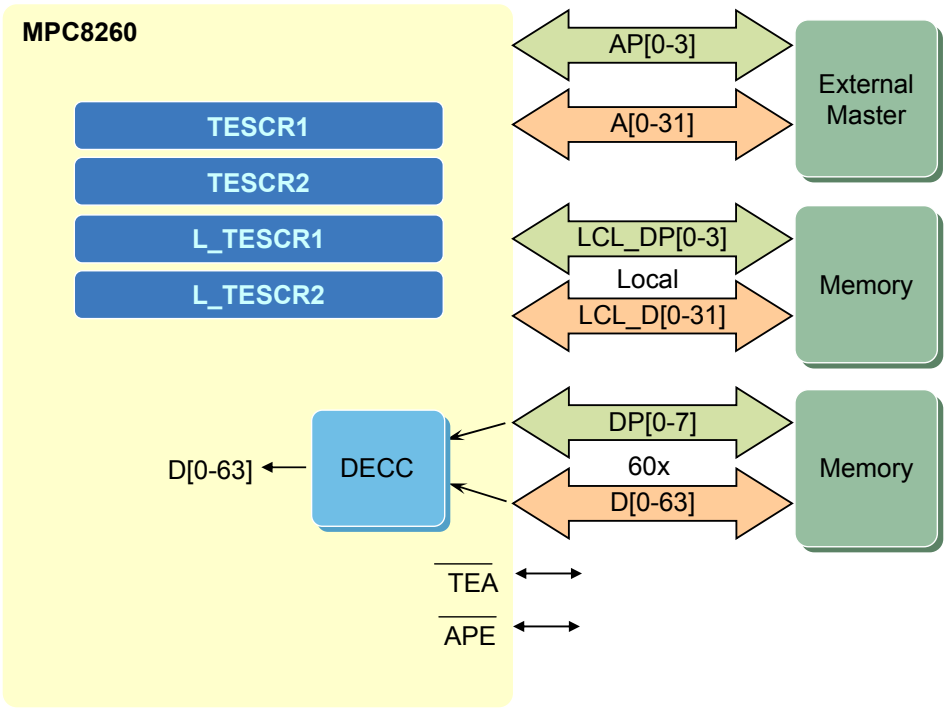
- Useful where multiple devices, such as MPC8260 family members, containing memory controller are used together.
- Available on 60x bus only.

There are situations where more than one device with a built in memory controller are used in a system. For instance there could be two or more PowerQUICC II devices used when more peripherals are required than provided by a single device. In that case, one of the device's memory controller can be used for memory control by all the processors.

This facility is only available for use with the 60x bus since the local bus cannot be used in multi-master mode. When any device connected to the bus performs a memory access the memory controller selected to handle the transaction recognizes the transfer request and provides all the necessary control signals to access the memory.

When the PowerQUICC II is using an external memory controller, the internal base and options register perform the bank recognition, but not the machine selection. The appropriate chip select signal is asserted and the external controller performs the machine selection and appropriate transfer signals. The external master provides the address acknowledge, transfer acknowledge, and partial data valid signals to terminate the cycles within the PowerQUICC II .

- The MPC8260 parity system is a combination of registers and pins as shown below.



The PowerQUICC II supports parity for the address bus, local bus and 60x bus. Parity checking is performed on a byte basis and for the address bus and local bus, there is support for four parity bit for each, due to each being 32-bit busses. The 60x bus is 64-bits and so eight parity pins are available for that.

Parity is supported using the transfer error status and control registers, and there are two for each bus. The 60x bus has support for data error checking and correction, which can detect all double bit errors. In this instance, any single bit error can be corrected as long as 64-bit transfers are used. For all data parity errors, except single bit corrected errors, the transfer error acknowledge and data parity error signals are asserted.

An address parity error results in the address parity error signal assertion. Notice that the signals are bi-directional since an external master could be in use. For more details of the TESCRs, click on the one of interest.

Parity Pins

I/O	**DP0** / NC / RSRV / EXT_BR2
I/O	**DP1 /** IRQ1 / EXT_BG2
I/O	**DP2 /** IRQ2 / TLBISYNC / EXT_DBG2
I/O	**DP3** / IRQ3 / CKSTP_OUT / EXT_BR3
I/O	**DP4** / IRQ4 / CORE_SRESET / EXT_BG3
I/O	**DP5** / IRQ5 / TBEN / EXT_DBG3
I/O	**DP6** / IRQ6 / CSE0
I/O	**DP7** / IRQ7 / CSE1
I/O	**AP[0]** / CS11
I/O	**AP[1]** / MODCK1 / TC[0]/BNKSEL[0]
I/O	**AP[2]** / MODCK2 / TC[1]/BNKSEL[1]
I/O	**AP[3]** / MODCK3 / TC[2] / BNKSEL[2]
I/O	**LCL_DP[0-3]** / C/BE[0-3]
O/P	**APE**

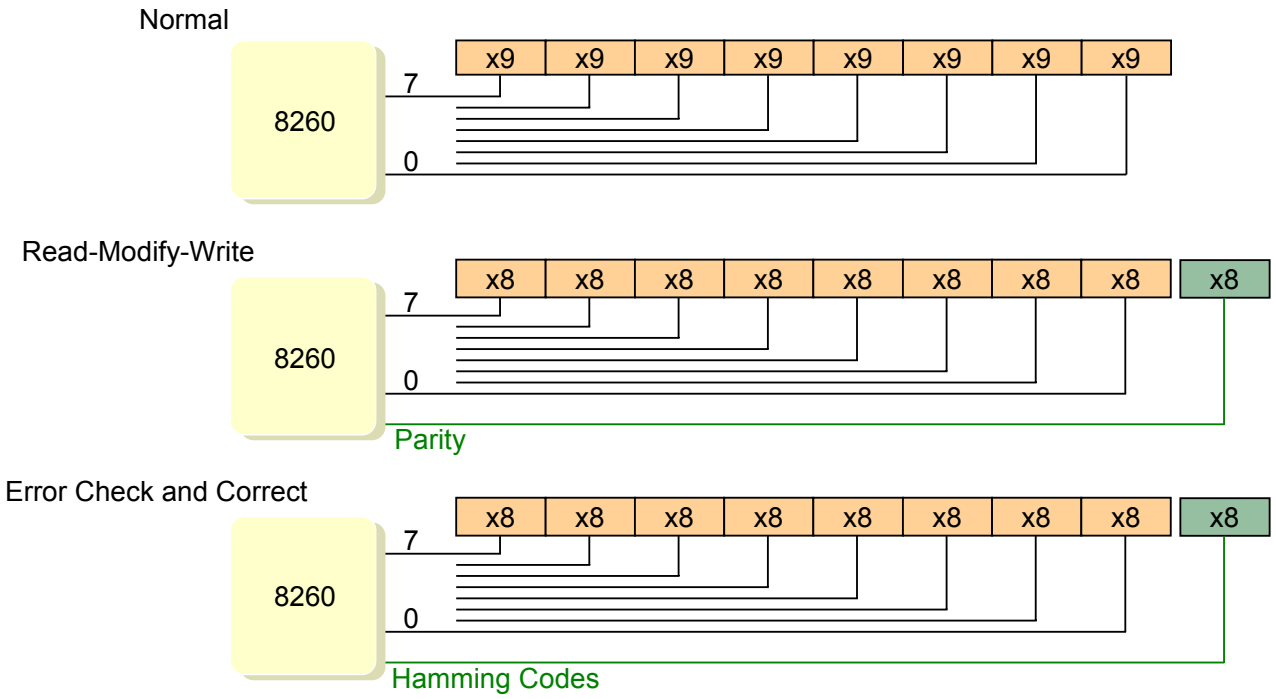
Register control	Pins functions
SIUMCR[DPPC] = 1	Data Parity and not alternate functions
SIUMCR[APPC] = 1	Address Parity and not alt. functions

This chart shows the parity pin options, and with the exception of the data parity error and address parity error pins all others use multi-function pins. In most cases, the pins can be either an input or output depending on the function it is used for. The majority of these pins can perform several functions and so there are two levels of control.

The SIU module configuration register defines if the pin performs a parity function or an alternative. When the pin is selected for an alternative, the port control defines which alternative it is used for.

Parity Options

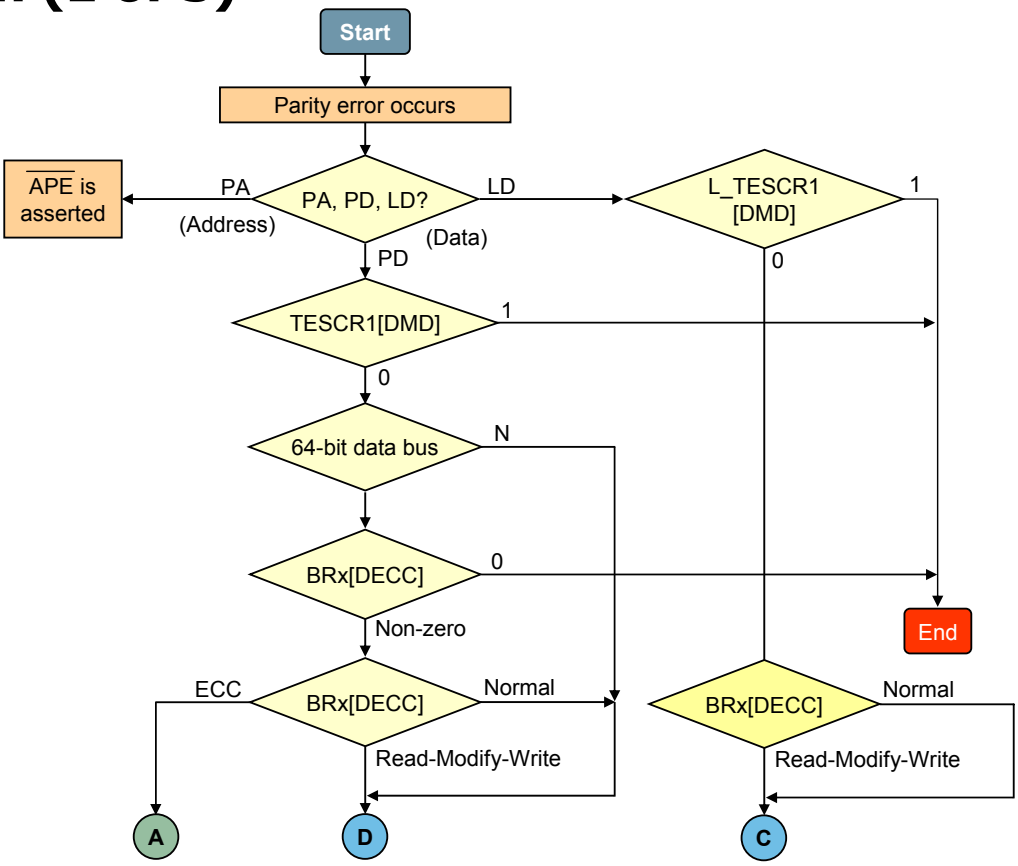
- 3 parity options are offered, Normal, Read-Modify-Write, and Error Check and Correction.
- An alternative is no parity.



There are three parity options available apart from not using parity checking. The normal method of parity checking is for each byte of memory having its own parity bit. This is simple to use, and any access has a directly related parity input. An alternative for a 64-bit data bus is to have a separate parity byte associated with the eight bytes of data.

This is complicated by the fact that only eight bit parity inputs are available and so they can only relate to eight byte accesses. This means that for smaller data transfers a complete sixty-four bit access must still be made. If error correction is required, then a similar approach is used, except that the byte that returned parity in the previous case returns a hamming code instead. Using this method, any two bit error can be detected and single bit errors can be corrected. The PowerQUICC II supports all of these options.

Operation (1 of 3)

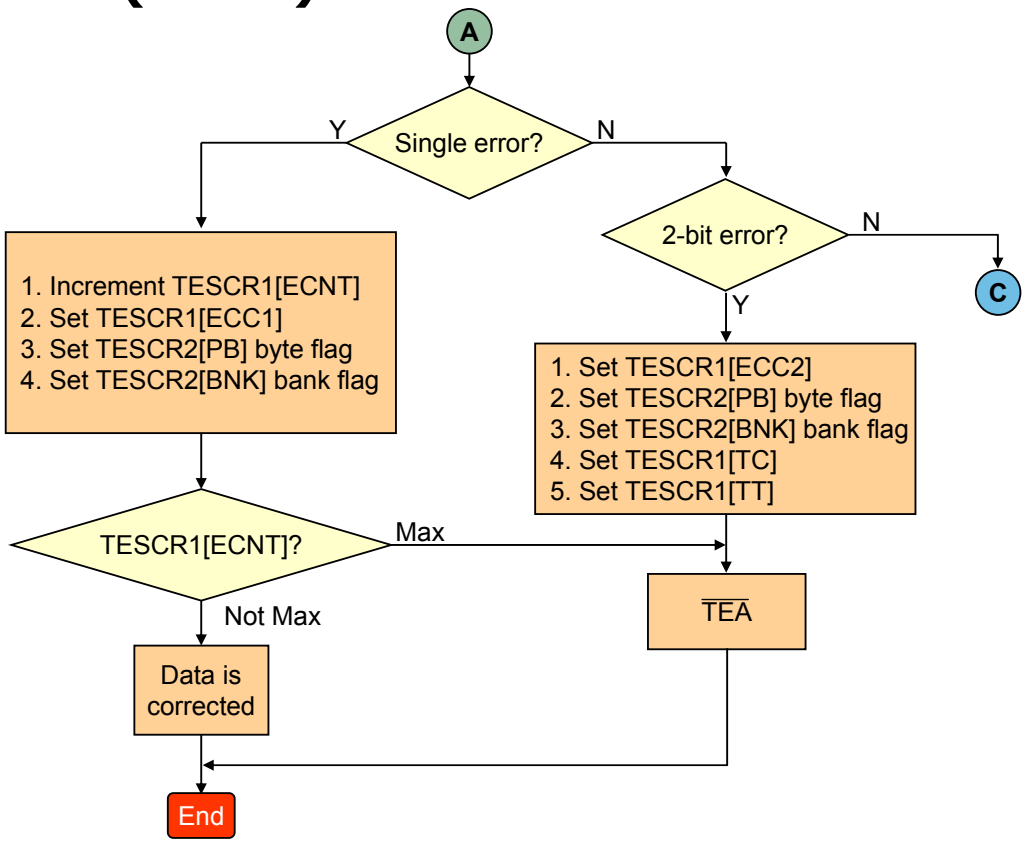


This flow chart indicates how the parity checking operates. When a parity error occurs, the first consideration is whether it's an address error or which data bus it affects. An address error asserts the address parity signal. Both data bus errors depend on error detection being enabled. If not, then there is no indication or affect. Either can be independently enabled.

If they are enabled, then if the error is on the local bus or not on a 64-bit bus, then a standard parity error takes place. This is shown on a subsequent page via route C. Otherwise, unless error detection is disabled in the base register, the result depends on the type of parity checking taking place, again selected in the base register.

If normal parity or read-modify-write parity checking is selected, then the normal parity error on route C or D is followed depending on the bus it relates to. If error check and correction is selected, then the hamming code is used and the remainder of the flow is shown on the next page

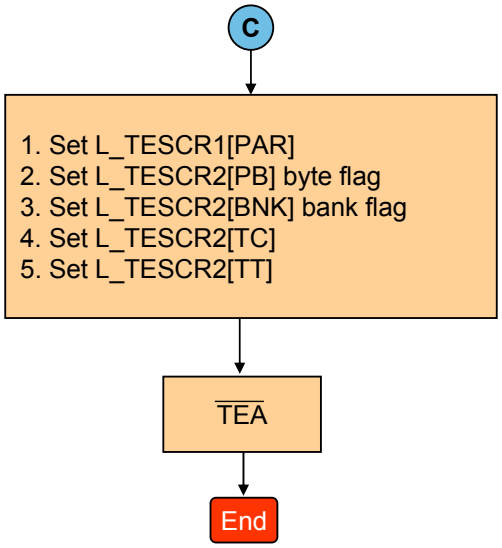
Operation (2 of 3)



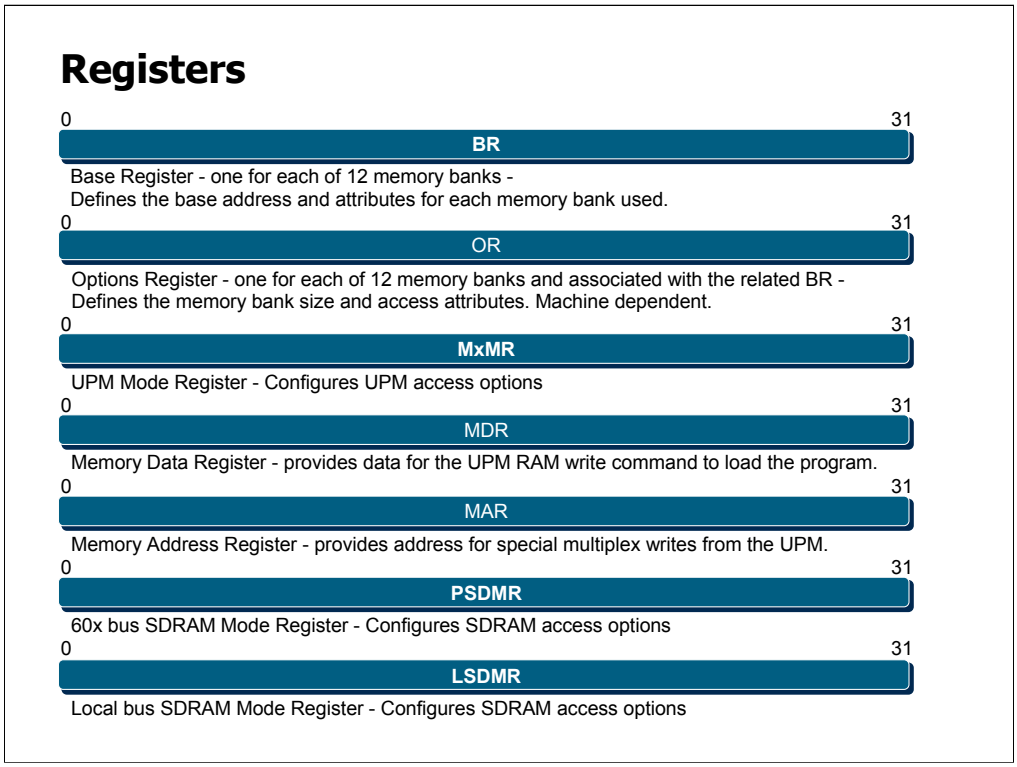
This is a continuation of the ECC flow. If this is a single error, then a count of errors is incremented, an indication that a single error occurred is set, an indication of which byte the error occurred on is set, and which bank the error related to. There is a limit on how many errors will be accepted, and if that reaches the maximum of two hundred and fifty-five then an error is indicated, otherwise the error is corrected and the process ends.

If this is not a single error and it is a two bit error, then there is an indication of a double ECC error, the byte and bank it relates to and the transfer code and type indicated for the transfer. The transfer error and data parity error pins are asserted, and the process ends. If there are more than 2 bit errors, then the normal error route is taken, shown on the next page.

Operation (3 of 3)



In this case the same information is indicated as for the two bit error except that a parity error is indicated instead of a double ECC error. Notice that the result of a parity error is a machine check exception if enabled.

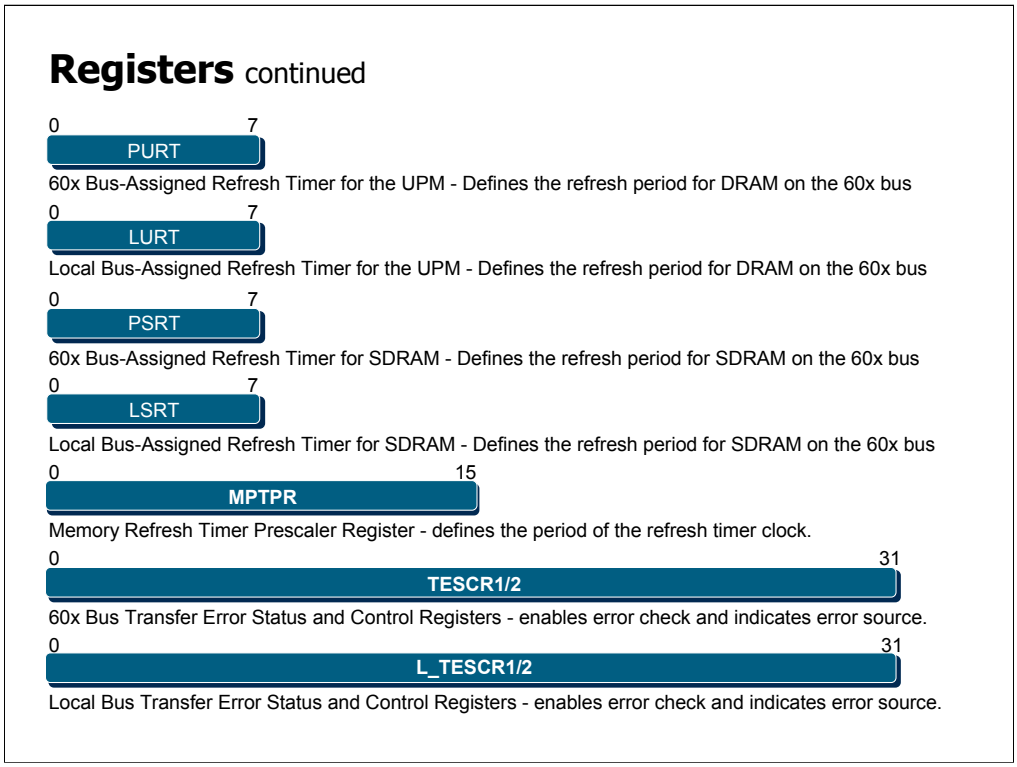


These and on the next page are all the registers associated with the memory controller. Some of them relate to specific machines and so will only be accessed if that machine is in use. Base Register defines the base address and attributes for each memory bank used and selects the machine to control transfers. They are paired with the option registers to define a memory block. There is one for each of 12 memory banks.

Options Register defines the memory bank size and access attributes. Paired with the base register, there is one for each of 12 memory banks. The option registers are machine dependent and so further information is available in the specific sections. There are three UPM Mode Registers designated A, B, and C, one for each UPM. They configure access options selecting a variety of functions controlled by the UPM.

Memory Data Register is used to write the values required into the UPM ram, which is not directly accessible to the user. The ram entry data required is written into this register and then and a ram array write command performed. Alternatively, a ram array read command can be performed and the returned value is here. A value in the Memory Address Register can be output to the address line by the AMX command from the UPM.

The 60x bus SDRAM Mode Register configures SDRAM access options such as timing, address configuration, multiplexing etcetera, for devices connected to the 60x bus. The local bus SDRAM Mode Register does the same thing for the local bus. To view the registers in detail, click on the one of interest.



The 60x Bus-Assigned Refresh Timer for the UPM defines the refresh period for DRAM on the 60x bus. The Local Bus-Assigned Refresh Timer for the UPM does the same thing for devices connected to the local bus. The 60x Bus-Assigned Refresh Timer for SDRAM defines the refresh period for SDRAM on the 60x bus. The Local Bus-Assigned Refresh Timer for the SDRAM does the same thing for devices connected to the local bus.

The four refresh period registers are simple 8-bit registers containing the refresh rate required. The Memory Refresh Timer Prescaler Register defines the period of the refresh timer clock. The 60x Bus Transfer Error Status and Control Registers enables error check and indicates error source on the 60x Bus. There are two registers to provide all the necessary information. The Local Bus Transfer Error Status and Control Registers do the same for the local bus.

To view the registers in detail, click on the one of interest. This completes the memory controller module.