Course Introduction

Purpose:
• The intent of this course is to give you a brief overview of the S08 multi-purpose clock generator (MCG) module, including its clock modes and special features.

Objectives:
• Identify all eight clock modes available in the MCG module.
• Describe any additional functional features in the MCG module.

Content
• 10 pages
• 2 questions

Learning Time
• 25 minutes

This course will present you with a brief overview of the S08 multi-purpose clock generator (MCG) module. You will learn about the important features of this module as well as the different clock modes available. By the end of this course, you will have a better understanding of the basic functionality of the MCG module, and you will be better prepared to select the best clock mode for your application.
Let's take a look at the MCG module.

It includes eight modes of operation: FEI, FBI, FBE, FEE, PBE, PEE, BLPE, and BLPI clock modes.

Three of these modes, FEI, FBI, and BLPI, require no external components and run off of the microcontroller’s internal clock.

All of these modes are software selectable.

For greater flexibility, the user software can switch between MCG modes at any time.

As a rule of thumb, the microcontroller bus frequency is equal to the MCGOUT frequency divided by two.
Here you can see a functional block diagram of the MCG module. The MCG consists of five main blocks.

The oscillator block allows the user to connect an external crystal or resonator for use with the MCG. The user can select either a high frequency range of 1 to 5 MHz in all modes, or a low frequency range of 32 to 38.4 kHz for the crystal or resonator. Check the XOSC and MCG electrical characteristics in the device datasheet for additional high range frequency limits for different MCG modes.

Also, the oscillator block can be used to route a square wave frequency from a signal generator or other equivalent oscillator sources to the system. For increased flexibility, the user can also configure the oscillator block for low power or high amplitude.

The internal reference generator includes a 31.25 to 39.06 kHz internal clock source that is presented as MCGIRCLK in the block diagram. This frequency can be trimmed by writing to the MCGTRM register. For a finer trim, the FTRIM bit is also available in the MCG status and control register.

The FLL block takes the internal or external clock source divided to a reference of 31.25 to 39.06 kHz and filters it before locking at 1024 times the filtered frequency.

The PLL block takes an external clock source divided to a reference of 1 to 2 MHz and filters it before locking to a selected multiplier times the filtered frequency.

Finally, the clock select block controls the switching of different clock sources to the system clock tree. It manages the clock source select; the reference divider between 1 and 128, in powers of 2; and the fixed clock select, which appears as an MCGFFCLK signal. The MCGLCLK signal uses the FLL output divided by 2 as an alternative software-selectable clock source for the background debug controller.
Next, let's discuss the various MCG modes that are available for use. Select a button to learn more about a clock mode. After you have viewed all of the pages, click the forward arrow to go to the next page.
FEI mode is the default MCG mode out of reset.

The internal reference is trimmable with a resolution of 0.2 percent.

After reset, the internal reference frequency of approximately 31.25 kHz to 39.06 kHz multiplied by the fixed multiplier of 1024, equals approximately 32 MHz, which is the DCO frequency.

The bus frequency divider (BDIV) is by default divide by 2, so the resulting MCGOUT signal is 16 MHZ. This means that the default bus frequency out of reset is approximately 8 MHz.

When the MCG is in FEI mode, oscillator pins can be used as general I/O pins because no external connections are required.

In FEI mode, the PLL multiplier is fixed to 1024.

The MCGOUT signal frequency is equal to the digitally controlled oscillator, or DCO frequency divided by BDIV in MCG control register 2. The bus frequency is equal to the MCGOUT signal divided by 2. Therefore, the bus frequency in FEI mode is equal to DCO divided by two times the BDIV value.

There is also a loss of lock interrupt available for PLL loss of lock detection.

The internal reference in the MCG is accurate to approximately plus or minus 0.5% across temperature.

Finally, FEI mode consumes more power than both FBI and FBE modes.

<table>
<thead>
<tr>
<th>MCG Mode</th>
<th>Reference Clock</th>
<th>External Components</th>
<th>Bus Frequency</th>
<th>Clock Protection</th>
<th>Accuracy</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEI Mode</td>
<td>Trimmable with resolution of 0.2 percent</td>
<td>Oscillator pins can be used as general I/O</td>
<td>DCO ÷ (2 x BDIV)</td>
<td>Loss of lock interrupt available</td>
<td>Internal reference accurate to a typical +/- 0.5% across temperature</td>
<td>Higher than FBI or FBE</td>
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<td>FBI Mode</td>
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<td>FBE Mode</td>
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<td>FEE Mode</td>
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<td>PBE Mode</td>
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<td>PEE Mode</td>
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<td>BLPE Mode</td>
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</table>
FBI mode uses the internal reference directly, and allows trimming at a resolution of 0.2 percent.

The internal reference falls between 31.25 and 39.06 kHz.

As in FEI mode, oscillator pins can be used as general purpose I/O pins because no external components are required.

Although FBI mode does not use the FLL block with the DCO, the FLL is still on.

FBI mode does not use the DCO. Therefore, the bus frequency in this mode is equal to the internal reference clock divided by 2 times the BDIV value.

Note that a loss of FLL lock interrupt is available in this mode.

The FBI mode reference is very accurate when trimmed, and this mode consumes less power than both FEI and FEE modes.
The FBE clock mode runs off of an external reference.

When using an external crystal or resonator, the reference frequency must lie between 32 and 38.4 kHz for low range operation and between 1 MHz and 5 MHz for high range operation, as selected by the RANGE bit in MCG control register 2.

When using an external clock, the reference frequency also has an upper limit of 5 MHz.

Again, although the FLL block with the DCO is not used, the FLL is still on and should be configured properly with the RDIV bits.

As in FBI mode, the DCO is not used. Therefore, the bus frequency in FBE mode is equal to the external reference divided by two times the BDIV value.

Also, in FBE mode, loss of lock interrupt and loss of clock reset are software-selectable.

This mode, along with PBE mode, provide the highest clock accuracy because the clock is as accurate as the external source and consumes the lowest power of all non-low power MCG modes.
Like FBE mode, an external crystal, resonator, or clock source is required for FEE mode.

The oscillator frequency must lie in a low range of 32 to 38.4 kHz or a high range of 1 to 5 MHz, as selected by the RANGE bit in MCG control register 2.

Before applying the fixed 1024 multiplier when using an external reference frequency that falls within the high range, the Reference Divider, or RDIV, in MCG control register 1 must first be used to divide the reference down to a value between 31.25 and 39.06 kHz.

Like FEI mode, in FEE mode, the multiplier is also fixed at 1024.

As in FEI mode, the bus frequency in FEE mode is equal to the DCO frequency divided by 2 times BDIV. The DCO falls between 32 and 40 MHz.

Also, in FEE mode, loss of lock interrupt and loss of clock reset are software-selectable.

FEE mode generates a highly accurate system clock.

Power consumption is slightly higher than that of FEI mode in high range, but slightly lower for low range external source frequencies.

### MCG Modes

Select a button to learn about a clock mode.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Reference Clock</th>
<th>External Components</th>
<th>PLL/FLL</th>
<th>Bus Frequency</th>
<th>Clock Protection</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEI</td>
<td>External reference clock source</td>
<td>External crystal, resonator, or clock</td>
<td>FLL: Multiplier fixed to x 1024</td>
<td>DCO + (2 x BDIV); DCO = 32 to 40 MHz</td>
<td>Loss of lock interrupt and loss of clock reset available</td>
<td>Slightly higher or lower than FEI, depending on external source range</td>
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<td>FBI</td>
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<td>FBE</td>
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MCG Modes

Select a button to learn about a clock mode.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Reference Clock</th>
<th>External Components</th>
<th>PLL/FLL</th>
<th>Bus Frequency</th>
<th>Clock Protection</th>
<th>Accuracy</th>
<th>Power Consumption</th>
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<tbody>
<tr>
<td>FEI Mode</td>
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<td>FBI Mode</td>
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<td>FBE Mode</td>
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<td>FEE Mode</td>
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<td>PBE Mode</td>
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<td>BLPE Mode</td>
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<td>BLPI Mode</td>
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The PBE clock mode runs off of an external reference.

When using an external crystal or resonator, the external reference must lie between 32 and 38.4 kHz for low range operation and between 1 MHz and 16 MHz for high range operation, as selected by the RANGE bit in MCG control register 2.

When using an external clock, the reference frequency also has an upper limit of 40 MHz.

Although the PLL block with the VCO is not used, the PLL is still on and should be configured properly with the RDIV and VDIV bits. The PLLS bit in MCG control register 3 should also be equal to 1 here.

Because the voltage controlled oscillator, or VCO, is not used, the bus frequency in PBE mode, like in FBE mode, is equal to the external reference divided by two times the BDIV value.

Also, in PBE mode, loss of lock interrupt and loss of clock reset are software-selectable.

This mode, along with FBE mode, provides the highest clock accuracy because the clock is as accurate as the external source and consumes less power than PEE mode and the FLL engaged modes, but more than any of the FLL bypassed modes.
In PEE mode, the PLL multiplies the reference frequency derived from an external crystal, resonator, or clock source by a VCO divider (VDIV) value. The oscillator frequency must lie in a high range of 1 to 16 MHz, and the external clock frequency must lie in a 1 to 40 MHz range.

When the PLL is operational, the RANGE bit in MCG control register 2 must always be set to 1, to indicate a high range frequency. This is true even when using an external clock. Before applying the VDIV multiplier, the Reference Divider, RDIV in MCG control register 1 must first be used to divide the external clock source frequency to a value between 1 and 2 MHz.

The VDIV bits in MCG control register 3 will then select a multiplication factor between 4 and 40, and MCGOUT will then equal the multiplied frequency divided by the BDIV value.

To ensure the PLL clock is selected instead of the FLL clock, the PLLS bit in MCG control register 3 must be 1. The bus frequency in PEE mode is equal to the VCO output frequency divided by 2 times BDIV.

The VCO output falls between 7 and 55 MHz, although this upper limit is restricted by the maximum CPU clock frequency. When selecting the VDIV bits, it is important to set the multiplier such that the resulting VCO output frequency is within its proper range. For instance, a reference divided to 1 MHz by RDIV cannot be set for a VDIV multiplier of 4 because 1 MHz x 4 is 4 MHz, which is less than the 7 MHz minimum VCO output frequency.

Also, in PEE mode, loss of lock interrupt and loss of clock reset are software-selectable. PEE mode generates a highly accurate system clock; it is almost as accurate as the external source and has less jitter than the clock generated in FEE mode.

Power consumption is slightly higher or lower than the FLL engaged modes depending on the output frequency.
### MCG Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Reference Clock</th>
<th>External Components</th>
<th>PLL/FLL</th>
<th>Bus Frequency</th>
<th>Clock Protection</th>
<th>Accuracy</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEI Mode</td>
<td>External reference clock source</td>
<td>External crystal or resonator</td>
<td>FLL and PLL disabled for lower power consumption</td>
<td>External reference ÷ (2 x BDIV)</td>
<td>Loss of lock interrupt and loss of clock reset available</td>
<td>Highest (as accurate as the external source)</td>
<td>Lower than all modes except FBILP mode</td>
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<td>FBI Mode</td>
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<td>FBE Mode</td>
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<td>FEE Mode</td>
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<td>PBE Mode</td>
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<td>PEE Mode</td>
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<td>BLPE Mode</td>
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<td>BLPI Mode</td>
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</table>

**Select a button to learn about a clock mode.**

BLPE mode is a low power MCG mode. This mode is similar to FBE and PBE modes, but with both the FLL and PLL disabled for lower power consumption. In this mode, MCGLCLK will not be available for BDC communications.

Note also that both the external crystal or resonator and the external clock have a greater available frequency range in BLPE mode because neither the FLL nor the PLL impose restrictions on the reference frequency.

Because both the PLL and FLL are disabled, this mode is optimal for changing the RDIV, PLLS, or VDIV bits when switching between FBE and PBE modes without affecting either a running PLL or FLL clock.

Like FBE and PBE modes, the bus frequency in BLPE mode is the external reference divided 2 times the BDIV value.

A loss of lock interrupt and loss of clock reset are optionally available for system clock protection.

Also, the accuracy of the clock in BLPE mode is as high as the external source.

BLPE mode consumes less power than all of the modes except FBILP mode.
**MCG Modes**

Select a button to learn about a clock mode.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Reference Clock</th>
<th>External Components</th>
<th>PLL/FLL</th>
<th>Bus Frequency</th>
<th>Clock Protection</th>
<th>Accuracy</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEI Mode</td>
<td><em>Direct Use of Internal reference</em>&lt;br&gt;<em>Trimmable with resolution of 0.2 percent</em>&lt;br&gt;<em>Internal reference</em> = 31.25 to 39.06 kHz</td>
<td>*Oscillator pins can be used as general i/O&lt;br&gt;*No external components required</td>
<td>FLL and PLL disabled for lower power consumption (LP=0)</td>
<td>Internal reference ÷ (2 x BDIV)</td>
<td>Loss of lock interrupt available</td>
<td>Very accurate when trimmed</td>
<td>Lowest of all modes</td>
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<td>FBI Mode</td>
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<td>FBE Mode</td>
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<td>FEE Mode</td>
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<td>BLPE Mode</td>
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<td>BLPI Mode</td>
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</table>

BLPI mode is a low power MCG mode. It is exactly like FBI mode but with both the FLL and PLL disabled for lower power consumption.

Because the FLL is disabled, the MCGLCLK will not be available for background debug controller (BDC) communications. The power consumption for BLPI mode is the lowest of all the MCG clock modes because in BLPI mode, the bus is running at a slower frequency than in all other modes.
Mode Switching

This diagram illustrates the proper switching paths between the MCG modes. Because the MCG comes out of reset in FEI mode, only FEE, FBE, and FBI modes can be directly switched to out of reset because they are the only modes with direct paths from FEI mode. To get to any of the other modes, the MCG must first be configured for one of these three initial modes.

For example, if you want to configure the MCG for PEE mode, you must first configure the MCG for FBE mode, then for PBE mode, and lastly for PEE mode.

In the diagram, note that the IREFS bit switches between an internal and external reference clock.

The PLLS bit switches between the FLL and PLL clock, and the CLKS bit selects the output to the system clock.

In every mode, each time the PLLS, IREFS, or CLKS bits are changed, the corresponding bits in the MCG status and control register -- PLLST, IREFST, or CLKST -- must be checked before moving on. Care must be taken to ensure that the RDIV bits are set properly for the mode being switched to.

For instance, in PEE mode, if using a 4 MHz crystal, RDIV must be set to divide-by-2 or divide -by-4 in order to divide the external reference down to the required frequency between 1 and 2 MHz. Also, the RDIV and IREFS bits should always be set properly before changing the PLLS bit so that the FLL or PLL clock has an appropriate reference clock frequency to switch to.
Here are several additional features to take note of when using the MCG module. These include low power or high gain oscillator options, the clock monitor options, and the software-selectable BDIV. Be sure to consult device-specific data sheets to guarantee proper operation of the module.

The HGO bit in MCG control register 2 determines whether the MCG operates in low power or high gain mode.

To minimize power consumption, low power mode will limit the voltage swing on the oscillator pins.

On the other hand, high gain mode drives rail-to-rail voltage swings on the oscillator pins.

The clock monitor in the MCG allows for an optional reset upon loss of external clock and an optional interrupt upon loss of PLL or FLL lock.

The clock monitor options can also be disabled to save power.

The software-selectable BDIV is located in MCG control register 2, and is available in all MCG modes.

It allows the clock source selected by the clock source select (CLKS) bits in MCG control register 1 to be divided down by 1, 2, 4, or 8.

With the BDIV, frequency changes can occur without the FLL or PLL losing lock.

The default value for the BDIV after reset is set to divide by 2.
STOP Effects on MCG

- Exit from Stop 3 can use an external oscillator or the programmed internal clock source
- Exit from all other stop modes always uses the default FEI mode to start up quickly

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>FBI mode</td>
<td>Startup is immediate at trimmed frequency</td>
</tr>
<tr>
<td>FEI mode</td>
<td>Startup is immediate at pre-STOP frequency</td>
</tr>
<tr>
<td>FEE mode</td>
<td>Startup is immediate at pre-STOP frequency</td>
</tr>
<tr>
<td>FBE mode</td>
<td>Startup is delayed based on external reference stabilization time</td>
</tr>
<tr>
<td>PBE mode</td>
<td>Startup is delayed based on external reference stabilization time</td>
</tr>
<tr>
<td>PEE mode</td>
<td>Startup is immediate at pre-STOP frequency</td>
</tr>
<tr>
<td>BLPE mode</td>
<td>Startup is delayed based on external reference stabilization time</td>
</tr>
<tr>
<td>BLPI mode</td>
<td>Startup is immediate at trimmed frequency</td>
</tr>
</tbody>
</table>

NOTE: In Stop 3, current is not affected by MCG mode before entering; it is only affected by the references enabled in STOP.

The MCG module behaves differently during STOP recovery depending on the STOP state prior to wakeup.

Recovery from Stop 3 allows usage of either an external oscillator or the programmed internal clock source. The selected clock source can optionally continue to run, which enables faster startup. Stop 3 recovery occurs under different conditions, depending on the MCG mode in the pre-STOP state.

Here you can see a description of the conditions in each of the MCG modes.

Recovery from all other stop modes always uses the default FEI mode to start up quickly.

Note that current is not affected by the MCG mode before entering Stop 3, but it is affected by the references enabled during STOP. Either the internal reference, the external reference, or both references can be left running in Stop 3.
Question

Which statements about the S08 multi-purpose clock generator (MCG) module are correct? Select all that apply and then click Done.

- It includes eight modes of operation: FEI, FBI, FBE, FEE, PBE, PEE, BLPE, and BLPI.
- All clock modes are software selectable.
- Only the FEE, FBE, and PEE modes can be directly switched to out of reset.
- The oscillator block can be configured for low power or high amplitude.

Done

Here is a question about the features of the S08 MCG module.

Correct.

The S08 MCG includes eight clock modes. All are selectable in software, but only the FEE, FBE, and FBI modes can be directly switched to out of reset. For increased flexibility, the user can configure the oscillator block for low power or high amplitude.
Now, let’s check your understanding of what you have learned about the MCG clock modes.

Correct.

The FEI mode is the default mode out of reset. The PEE mode is less accurate than PBE mode. The BLPE mode is a low power mode. And, the FBE mode is as accurate as an external source.
Course Summary

S08 MCG module:
- Block diagram
- MCG clock modes:
  - FLL Engaged Internal (FEI) clock mode
  - FLL Bypassed Internal (FBI) clock mode
  - FLL Bypassed External (FBE) clock mode
  - FLL Engaged External (FEE) clock mode
  - PLL Bypassed External (PBE) clock mode
  - PLL Engaged External (PEE) clock mode
  - Bypassed Low Power External (BLPE) clock mode
  - Bypassed Low Power Internal (BLPI) clock mode
- Additional and functional MCG features

This course provided you with a brief look at the S08 MCG module.

First, you examined a block diagram for the MCG module.

Next, you learned about the features and functions of the various MCG modes. For example, all of these modes are software selectable, and the user software can switch between MCG modes at any time.

You also explored additional features of the S08 MCG module, including how the module behaves during STOP mode recovery, which depends on the STOP state prior to wakeup.

Now that you have completed this course, you should have a better understanding of the basic functionality of the MCG module and be better prepared to select the best clock mode for your application.