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POWERING INNOVATION

QorIQ P5 Processor: Overcome the Challenges in Porting U-Boot and Linux® OS

FTF-NET-F0180

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NPD Applications Engineering

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Session Introduction

Board bring-up is a key activity for new silicon. Firmware and OS are the first software components run on the reference platforms. Initial bring-up involves debug of silicon, board and the software.

This presentation details the important parts of firmware (u-boot) and OS (Linux) porting/bring-up for the P5020DS reference platform. Freescale's Board Support Package (BSP) provides software that can be modified to run on customer development systems.

This talk will give a glimpse of the ideas, initial steps and strategies to accomplish a basic port of u-boot and Linux for functional validation of the board and processor. We highlight relevant parts of the code needed most commonly during this effort.

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Session Objectives

Learn more about the P5020/P5020DS, P5040/P5040DS

Details of U-boot and Linux porting

- Obtain and build U-boot and Linux from source
- Peruse source trees for making changes specific to your platform
- Identify components and separation of tasks between software components

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Agenda

- Introduction – 15 minutes
- U-boot – 35 minutes
- Device Tree and Linux – 35 minutes
- Summary

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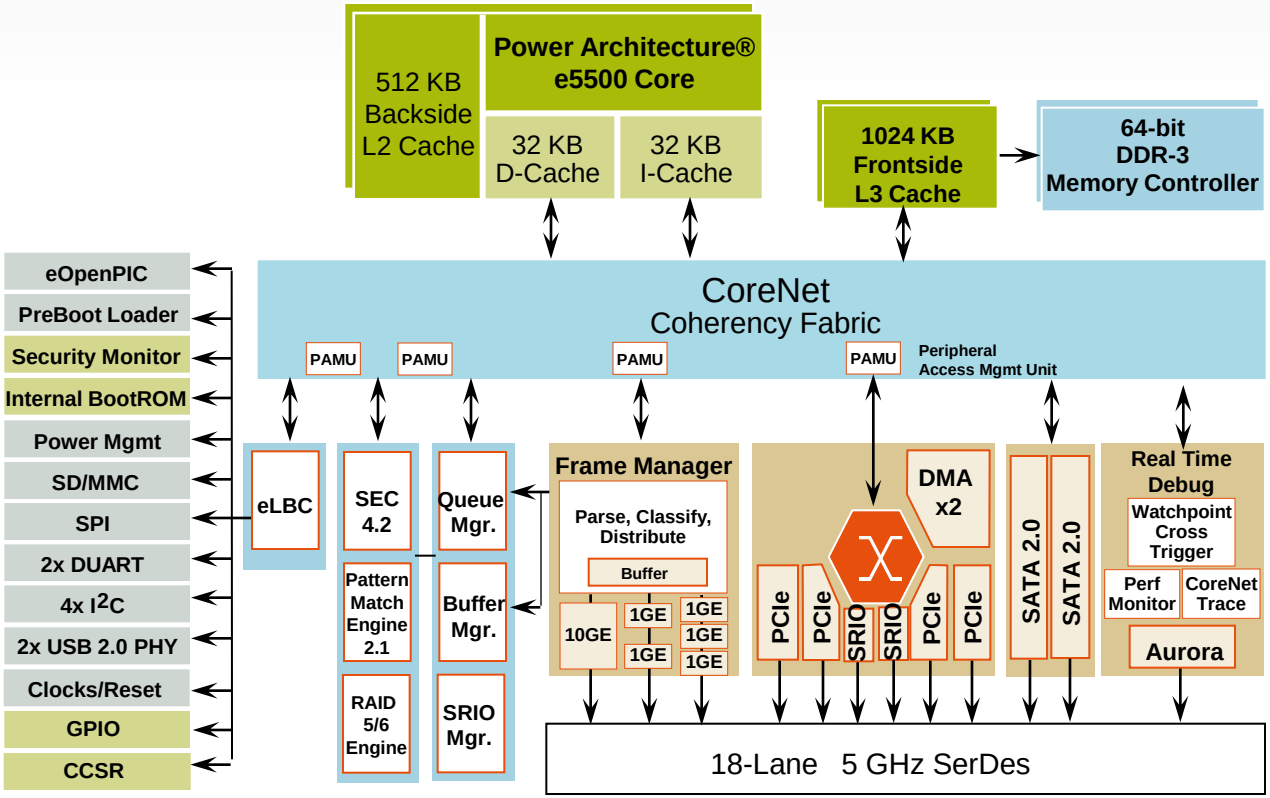
QorIQ™ P5020 Block Diagram



Dual e5500 Power Architecture®

- 2x 64-bit e5500 cores (2GHz)
- Each with 512 KB backside L2 cache
- Dual 1MB Shared L3 Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Controller

- Dual DDR3, 3L up to 1.3 GHz
- 32/64 bit data bus w/ECC

High Speed Interconnect

- 4 PCIe 2.0 Controllers
- 2 SRIO 1.3/2.1 Controllers
- 2 SATA 3Gb/s
- 2 USB 2.0 with PHY

CoreNet Switch Fabric

Ethernet

- 5 x 10/100/1000 Ethernet Controllers
  - Or 4x 2.5Gb/s SGMII
- 1 x 10GE Controllers
- All w/ Classification, H/W Queueing, policing, and Buffer Management, Checksum Offload, QoS, Lossless Flow Control, IEEE 1588
- Up to 1 XAUI, 4 SGMII or 2.5Gb/s SGMII, 2 RGMII

Datapath Acceleration

- SEC 4.2
- PME 2.1
- RapidIO Messaging: Type 9 and 11
- RAID5/6 Engine

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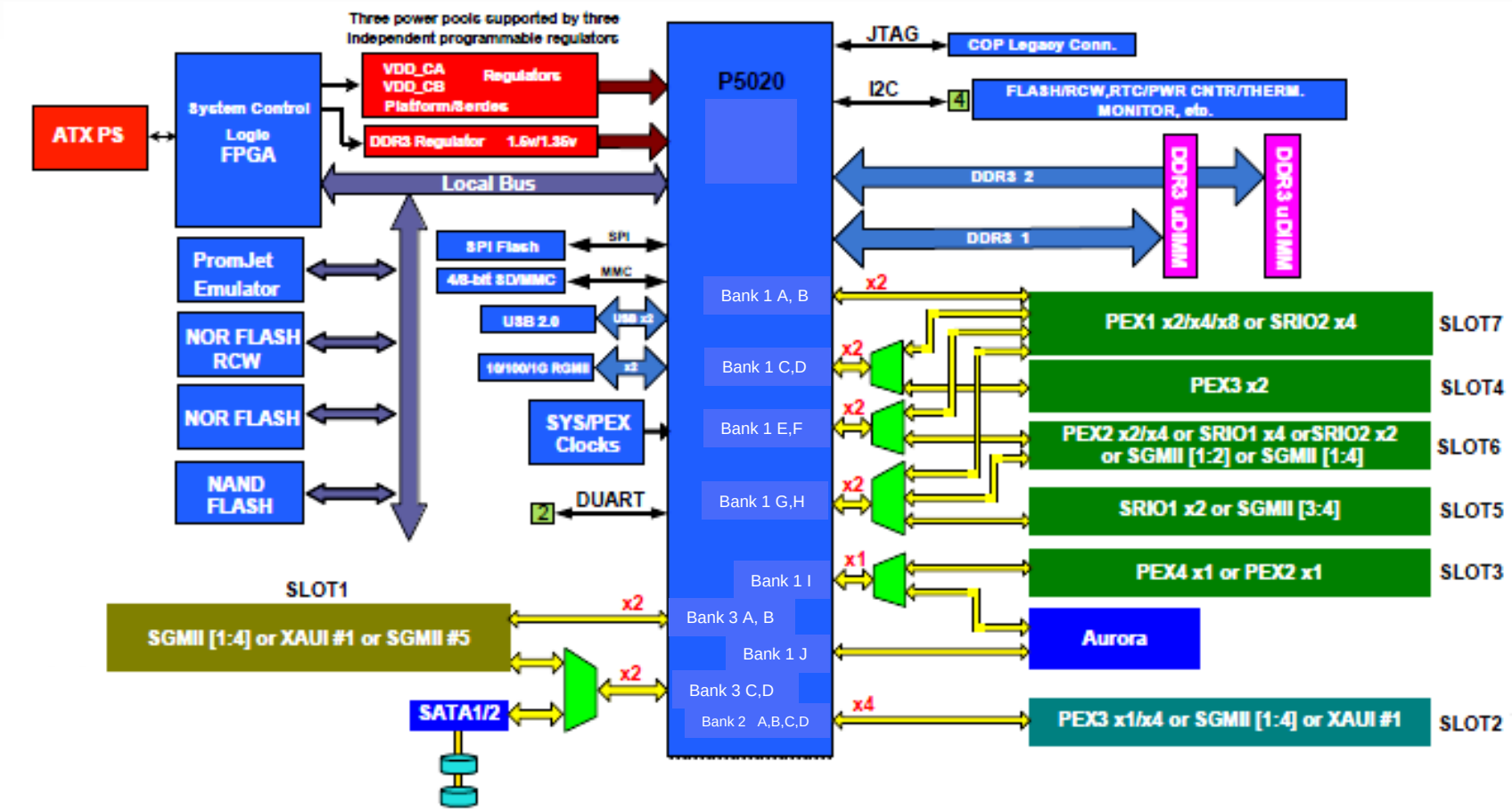

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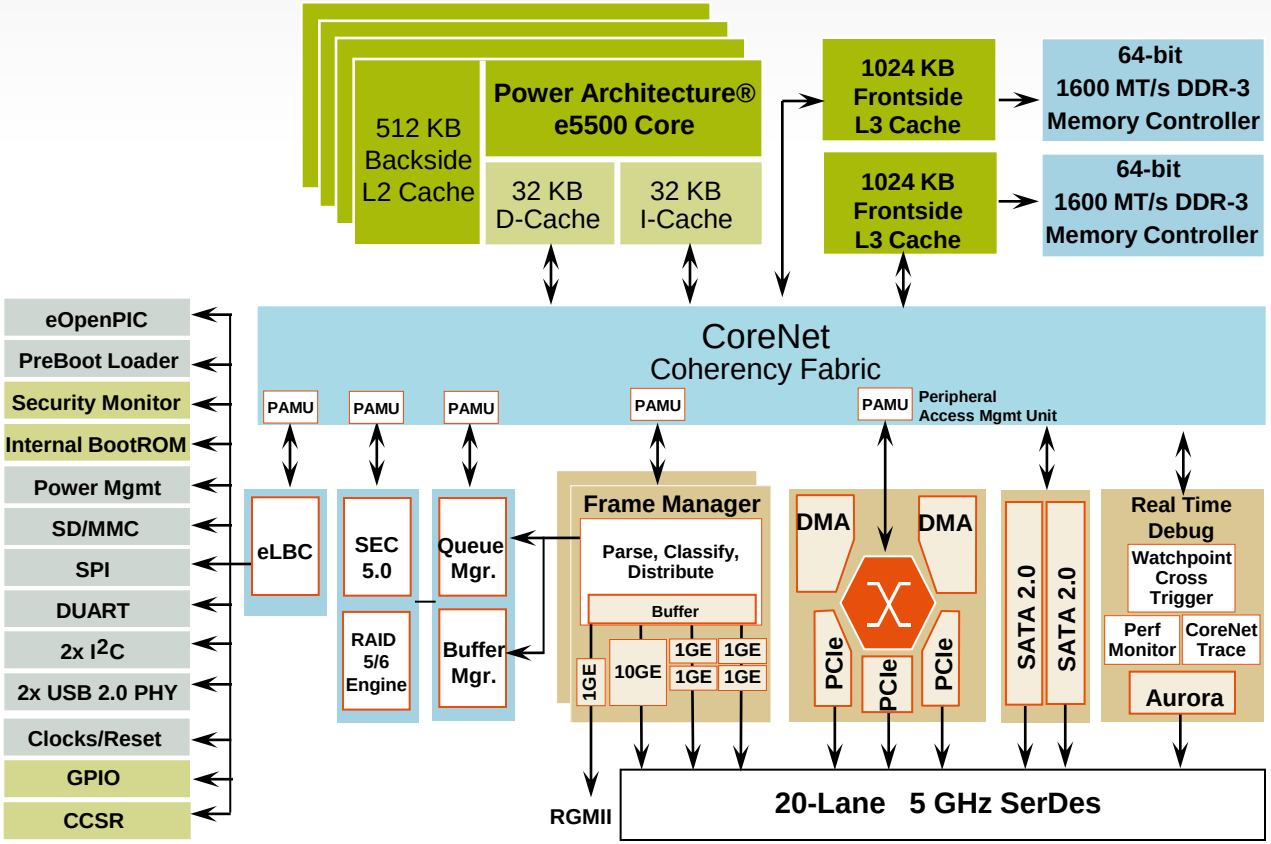
QorIQ™ P5 Series P5040



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- 4x 64-bit e5500 cores (2.2 GHz+)
- Each with 512 KB backside L2 cache
- Dual 1MB Shared L3 Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Controller

- Dual DDR3 SDRAM up to 1.6 GHz
- 32/64 bit data bus w/ECC

High Speed Interconnect

- 3 PCIe 2.0 Controllers
- 2 SATA 3Gb/s
- 2 USB 2.0 with PHY

CoreNet Switch Fabric

Ethernet

- 10 x 10/100/1000 Ethernet Controllers
- 2 x 10GE Controller (XAUI)
- All w/ Classification/Policing, H/W Queuing, policing, and Buffer Management, Checksum Offload, QoS, Lossless Flow Control, IEEE 1588v2, 8 SGMII

Datapath Acceleration

- SEC 5.0
- RAID 5/6 Engine

Device

- 45nm SOI Process
- 1295-pin package

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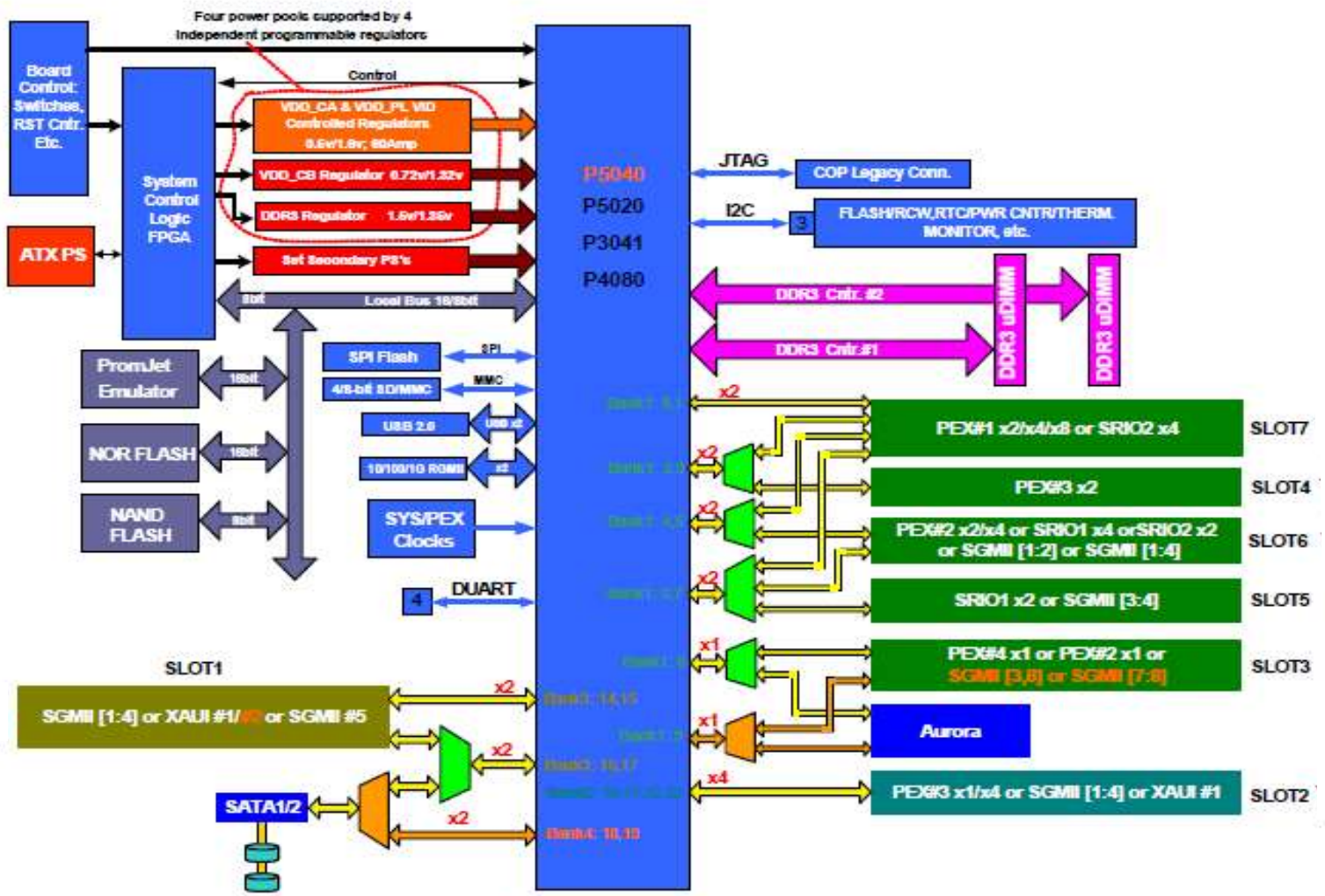
P5040DS Block Diagram



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Getting Started

- Master u-boot repository
  - http://git.denx.de
- Master Linux® repository
  - http://git.kernel.org
- BSP release
  - http://www.freescale.com/linux/
  - Follow instructions in the BSP documentation to extract u-boot package

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Sources

- Use QorIQ DPAA SDK 1.1 as starting point
- Upstream repositories have P5020 support
  - ***git*** SCM
    - Clone the tree locally
      - **git clone git://git.denx.de/u-boot.git**
      - **git clone git://git.kernel.org/linux-2.6.git**
      - Replicates the remote tree with change logs and tags
    - When ready to contribute
      1. Commit changes locally
      2. Create a patch and mail it to the u-boot list
      3. Peer review
      4. Patch applied to master tree for everyone to use
      5. Clean up patch for external world and repeat steps 2-4

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P5020DS U-boot

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Introduction

- What is u-boot?
  - Open source firmware for hardware platforms
  - A boot loader widely used in embedded space
- What does it do?
  - Brings the board to a sane state out of reset
  - Load OS image onto board and start OS
- Origins
  - DENX Software Engineering
  - More at "http://www.denx.de/wiki/U-Boot/WebHome"

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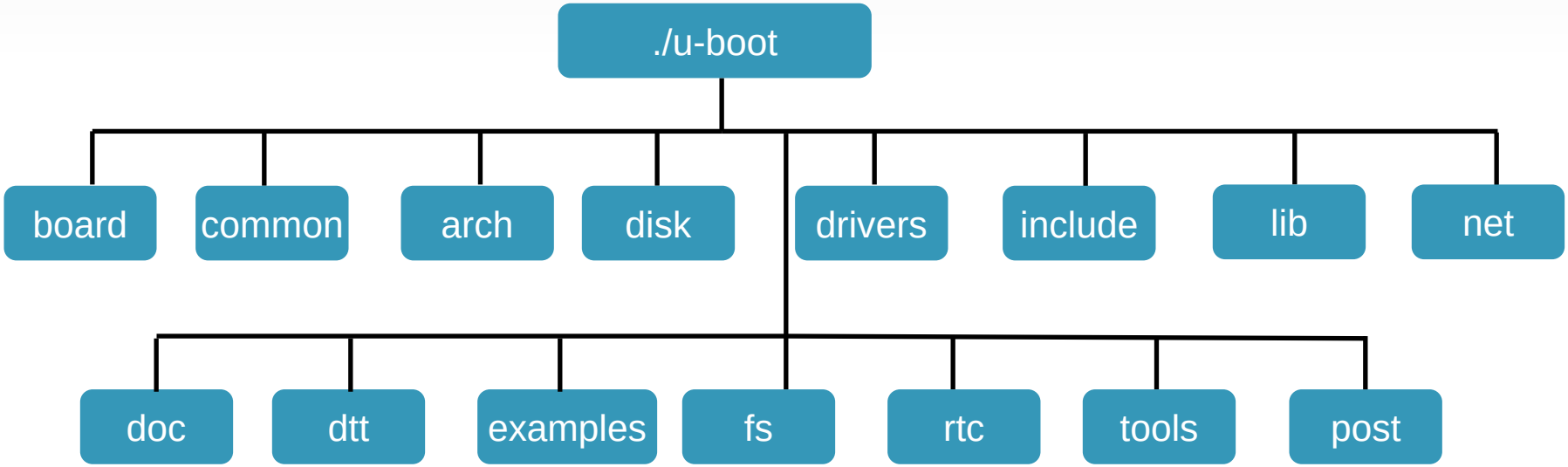
U-boot Directories



Relevant directories for modifications

u-boot/.
u-boot/board
u-boot/lib
u-boot/include
u-boot/arch/powerpc/*
u-boot/common

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Simplified Boot Sequence

- Reset vector points to FLASH (0xfffffffc)
- Begins execution in FLASH
- Initializes DUARTs
- Checks for information on version numbers, clocks and displays on screen
- Initializes DDR
- Relocates itself to DDR
- Continues execution in DDR
- Releases other cores
- Initializes higher level devices – ethernet, PCIe, SATA, USB, etc.
- Begins command interpreter

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U-boot Memory Map for P5020DS

```
/*
 * Memory map
 *
 * 0x0000_0000  0x7fff_ffff        DDR                 2G Cacheable

 * 0xf_fe00_0000                   CCSR                16M non-cacheable

 * 0xc_0000_0000                   PEX 1 Mem           512M non-cacheable
 * 0xc_2000_0000                   PEX 2 Mem           512M non-cacheable
 * 0xc_4000_0000                   PEX 3 Mem           512M non-cacheable
 * 0xc_6000_0000                   PEX 4 Mem           512M non-cacheable
 * 0xf_f800_0000                   PCI IO range        256K non-cacheable

 * 0xf_f400_0000                   Bman                2M
 * 0xf_f420_0000                   Qman                2M

 * Localbus non-cacheable
 *
 * 0xf_e000_0000                   Promjet/free        128M non-cacheable
 * 0xf_e800_0000                   FLASH               128M non-cacheable
 * 0xf_ffdf_0000                   PIXIS               32K non-cacheable TLB0

 * 0xffd0_0000                     L1 for stack        16K Cacheable TLB0
 */
```


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Initialization

- Processor info setup
- MMU, LAW setup
- Clocks
- Serial
- DDR
- Misc CPU init
- Relocate to DDR space
- Flash
- PCIe
- Misc init/MP init
- FM init

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Processor Info Setup

- Add information about P5020 in tables
- Files:
  arch/powerpc/include/asm/config_mpc85xx.h, processor.h
  arch/powerpc/cpu/mpc8xxx/cpu.c
- Code Snippets

```
#elif defined(CONFIG_PPC_P5020)
#define CONFIG_MAX_CPUS                2
#define CONFIG_SYS_FSL_NUM_CC_PLLS     2
#define CONFIG_SYS_FSL_NUM_LAWS        32
#define CONFIG_SYS_FSL_SEC_COMPAT      4
#define CONFIG_SYS_NUM_FMAN            1
#define CONFIG_SYS_NUM_FM1_DTSEC       5
#define CONFIG_SYS_NUM_FM1_10GEC       1
#define CONFIG_NUM_DDR_CONTROLLERS     2
#define CONFIG_SYS_FM_MURAM_SIZE       0x28000
```


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MMU, LAW Setup

- Configuring memory map
- Files:
  - include/configs/P5020DS.h, corenet_ds.h
  - board/freescale/corenet_ds/tlb.c, law.c
  - arch/powerpc/cpu/mpc85xx/tlb.c
  - drivers/misc/fsl_law.c
  - arch/powerpc/include/asm/immap_85xx.h
- Code Snippets:

```
/* *I*G* - Flash, localbus */
    /* This will be changed to *I*G* after relocation to RAM. */
    SET_TLB_ENTRY(1, CONFIG_SYS_FLASH_BASE, CONFIG_SYS_FLASH_BASE_PHYS,
                        MAS3_SX|MAS3_SR, MAS2_W|MAS2_G, 0, 2, BOOKE_PAGESZ_256M, 1),

SET_LAW(CONFIG_SYS_FLASH_BASE_PHYS, LAW_SIZE_256M, LAW_TRGT_IF_LBC),
```


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Stack In Cache

- Drivers written in C code
  - Need stack space to run
  - Lock the cache
  - Unlock before linux boot

*** 0xf_ffdf_0000**	**PIXIS**	**32K non-cacheable TLB0**
*** 0xffd0_0000**	**L1 for stack**	**16K Cacheable TLB0**

***/**

Files:

arch/powerpc/cpu/mpc85xx/start.S

Code Snippets:

```
lis     r6,FSL_BOOKE_MAS0(1, 14, 0)@h
ori     r6,r6,FSL_BOOKE_MAS0(1, 14, 0)@l

lis     r7,FSL_BOOKE_MAS1(1, 1, 0, 1, BOOKE_PAGESZ_16K)@h
ori     r7,r7,FSL_BOOKE_MAS1(1, 1, 0, 1, BOOKE_PAGESZ_16K)@l

lis     r8,FSL_BOOKE_MAS2(CONFIG_SYS_INIT_RAM_ADDR, 0)@h
ori     r8,r8,FSL_BOOKE_MAS2(CONFIG_SYS_INIT_RAM_ADDR, 0)@l

lis     r9,FSL_BOOKE_MAS3(CONFIG_SYS_INIT_RAM_ADDR, 0, (MAS3_SX|MAS3_SW|MAS3_SR))@h
ori     r9,r9,FSL_BOOKE_MAS3(CONFIG_SYS_INIT_RAM_ADDR, 0, (MAS3_SX|MAS3_SW|MAS3_SR))@l
    :
tlbwe
```


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SYSCLK

- SYSCLK value needed to get started
  - Derive core, plat, DDR clocks
- FPGA registers SCLK0, 1, 2
  - Input to ICS307 clock generator code
- Files:
  - Include/Configs/Corenet_ds.H (CONFIG_SYS_CLK_FREQ)
  - Board/freescale/corenet_ds/corenet_ds.c
  - Board/freescale/common/ics307_clk.c
- Code Snippets:

```
/* Calculate frequency being generated by ICS307-02 clock chip based upon
 * the control bytes being programmed into it. */
static unsigned long ics307_clk_freq(unsigned char cw0, unsigned char cw1,
                                     unsigned char cw2)
{
        const unsigned long InputFrequency = CONFIG_ICS307_REFCLK_HZ;
        unsigned long VDW = ((cw1 << 1) & 0x1FE) + ((cw2 >> 7) & 1);
:
}
unsigned long calculate_board_sys_clk(ulong dummy)
{
        ulong val;
        u8 *pixis_base = (u8 *)PIXIS_BASE;
        val = ics307_clk_freq(
            in_8(pixis_base + PIXIS_VSYSCLK0),
```


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Serial

- 2 DUARTs (4 UARTs) on P5020
  - 2 serial outputs on DS
- u-boot provides driver for NS16550 compatible DUARTs
- Serial port very useful for early debug
- Files:
  include/configs/corenet_ds.h
  drivers/serial/ns16550.c, serial.c
- Code Snippets:

```
#define CONFIG_CONS_INDEX       2
#define CONFIG_SYS_NS16550
#define CONFIG_SYS_NS16550_SERIAL
#define CONFIG_SYS_NS16550_REG_SIZE     1
#define CONFIG_SYS_NS16550_CLK          (get_bus_freq(0)/2)

#define CONFIG_SYS_NS16550_COM1 (CONFIG_SYS_CCSRBAR+0x11C500)
#define CONFIG_SYS_NS16550_COM2 (CONFIG_SYS_CCSRBAR+0x11C600)
#define CONFIG_SYS_NS16550_COM3 (CONFIG_SYS_CCSRBAR+0x11D500)
#define CONFIG_SYS_NS16550_COM4 (CONFIG_SYS_CCSRBAR+0x11D600)
```


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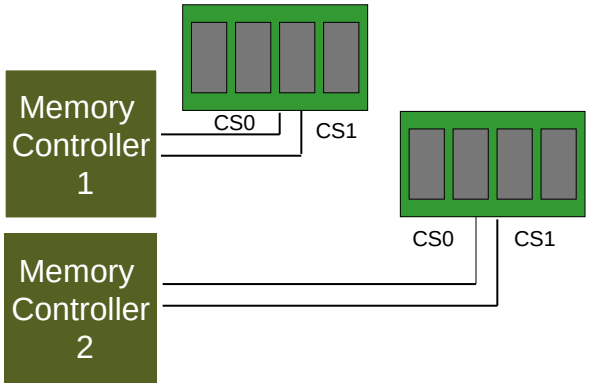
DDR Setup

- Supports multiple controllers and SPD-based (I2C eeprom) initialization
- Supports Interleaving
- Files:
  - arch/powerpc/cpu/mpc8xxx/ddr
  - include/configs/corenet_ds.h
  - board/freescale/corenet_ds/ddr.c ← **board specific parameters**



- Code Snippets:

```
#define CONFIG_DIMM_SLOTS_PER_CTLR      1
#define CONFIG_CHIP_SELECTS_PER_CTRL    (2 * CONFIG_DIMM_SLOTS_PER_CTLR)

#define CONFIG_DDR_SPD
#define CONFIG_FSL_DDR3

#define CONFIG_SYS_SPD_BUS_NUM  1
#define SPD_EEPROM_ADDRESS1     0x51
#define SPD_EEPROM_ADDRESS2     0x52
```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Misc CPU Init

- Set up local bus memory map
  - BRn, ORn
- Enable timebase register
- Files:

  arch/powerpc/cpu/mpc85xx/cpu_init.c
- Code Snippets:

```
void cpu_init_f (void)
{
        volatile ccsr_lbc_t *memctl = (void *)(CONFIG_SYS_MPC85xx_LBC_ADDR);
          :
          :
          #ifdef CONFIG_FSL_CORENET
                corenet_tb_init();
          #endif

           init_used_tlb_cams();

          /* Invalidate the CPC before DDR gets enabled */
          invalidate_cpc();
    }
```


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Initialization

- Processor info setup ✓
- MMU, LAW setup ✓
- Clocks ✓
- Serial ✓
- DDR ✓
- Misc CPU init ✓
- Relocate to DDR space
- Flash
- PCIe
- Misc init, MP init
- FM init

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Relocate To DDR Space

- Relocates u-boot code to top of memory
  - For 2GB on P5020DS, in the last 1MB
  - Set up of stack space, etc.
- Continues to run from DDR after relocation
- Files:
  - arch/powerpc/cpu/mpc85xx/start.S
  - lib_ppc/board.c
- Code Snippets:

```
/*
 * void relocate_code (addr_sp, gd, addr_moni)
 *
 * This "function" does not return, instead it continues in RAM
 * after relocating the monitor code.
 *
 * r3 = dest
 * r4 = src
 * r5 = length in bytes
 * r6 = cachelinesize
 */
        .globl  relocate_code
relocate_code:
        mr      r1,r3           /* Set new stack pointer              */
        mr      r9,r4           /* Save copy of Init Data pointer     */
        mr      r10,r5          /* Save copy of Destination Address   */
```


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NOR Flash

- CFI flash support
- Reads on POR
  - Sets up structures much later in the driver

*** Localbus non-cacheable**

```
*
* 0xf_e000_0000        Promjet/free     128M non-cacheable
* 0xf_e800_0000        FLASH            128M non-cacheable
* 0xf_ffdf_0000        PIXIS            32K non-cacheable TLB0
```

This information is used by the driver to detect the flash using CFI query at both possible addresses and populate its info table

- Files:
  - include/configs/corenet_ds.h
  - drivers/mtd/cfi_flash.c

- Code Snippets:

```
#define CONFIG_FLASH_CFI_DRIVER
#define CONFIG_SYS_FLASH_CFI

#define CONFIG_SYS_FLASH_AMD_CHECK_DQ7
#define CONFIG_SYS_FLASH_BANKS_LIST    {CONFIG_SYS_FLASH_BASE_PHYS + 0x8000000,
                                        CONFIG_SYS_FLASH_BASE_PHYS}
```

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PCIe

- Check for PCIe interfaces on the SOC
- Basic PCIe enumeration

*** 0xc_0000_0000**	**PEX 1 Mem**	**512M non-cacheable**
*** 0xc_2000_0000**	**PEX 2 Mem**	**512M non-cacheable**
*** 0xc_4000_0000**	**PEX 3 Mem**	**512M non-cacheable**
*** 0xc_6000_0000**	**PEX 4 Mem**	**512M non-cacheable**
*** 0xf_f800_0000**	**PCI IO range**	**256K non-cacheable**

- Files:

  include/configs/corenet_ds.h
  drivers/pci/fsl_pci_init.c
  board/freescale/corenet_ds/corenet_ds.c

- Code Snippets:

```
#define CONFIG_SYS_PCIE1_ADDR      (CONFIG_SYS_CCSRBAR+0x200000)
#define CONFIG_SYS_PCIE2_ADDR      (CONFIG_SYS_CCSRBAR+0x201000)
#define CONFIG_SYS_PCIE3_ADDR      (CONFIG_SYS_CCSRBAR+0x202000)
        :
        :
```


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Misc Init/MP Init

- Power-on Reset
  - Core0 comes out of reset at the reset vector 0xFFFF_FFFC and all other cores are in boot hold off mode
    - Core0 runs u-boot
      - After setting BSTRL/BSTAR to secondary core's start page, core0 kicks off each additional secondary core
      - Each secondary core comes out of reset at __secondary_start_page(boot page), initialize resources specific that core (caches, MMU, etc.) and enters a spin loop
    - Core0 loads Linux image and device tree and boots Linux

Figure 4-8. Boot Space Translation Register Low (BSTRL)

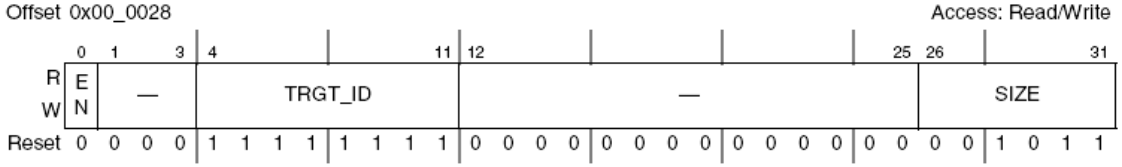

Figure 4-9. Boot Space Translation Attribute Register (BSTAR)

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Multicore Boot Architecture

- ePAPR describes specifics on how secondary CPUs are booted for a system with multiple CPUs
- Default boot architecture
  - The boot program releases all CPUs from hardware reset
  - One CPU is designated to be the client program's boot CPU
  - All other CPUs are secondary and are placed into loop where the CPUs spin, waiting for a spin table field to change that directs them where to go
  - Control is transferred to the client program on the boot CPU
  - When the client program is ready for secondary cores to start, it releases them by writing the spin table field with the desired address
- The architecture allows for other custom-defined secondary CPU release mechanisms as well

Reference: ePAPR (Power.org *Standard for Embedded Power Architecture™ Platform Requirements (ePAPR)*. power.org, 2008.)

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SMP Boot Process: U-boot Boot Process

- In the u-boot source, the entry point is the reset vector 0x0_FFFF_FFFC containing a simple branch to **_start_e500**, which is at the base of default boot page at 0x0_FFFF_F000; both are found in ***arch/powerpc/cpu/mpc85xx/start.S***

Reset vector → call _start_e500()

_start_e500() will:

_start_e500() → Boot other cores → Start command interpreter → Prepare device tree

1. Enable L1 caches
2. Config interrupt vectors
3. Config MMU and LAWs
4. Config L1D RAM
5. Config local bus
6. Config DDR
7. Relocate to DDR

1. Setup BSTRL and BSTAR
2. Release all other cores from boot holdoff using BRR and wait for them to boot.

1. Copy HW device tree to DDR
2. Copy uImage to DDR
3. Copy ramdisk fs to DDR
4. Launch Linux

arch/powerpc/cpu/mpc85xx/mp.c

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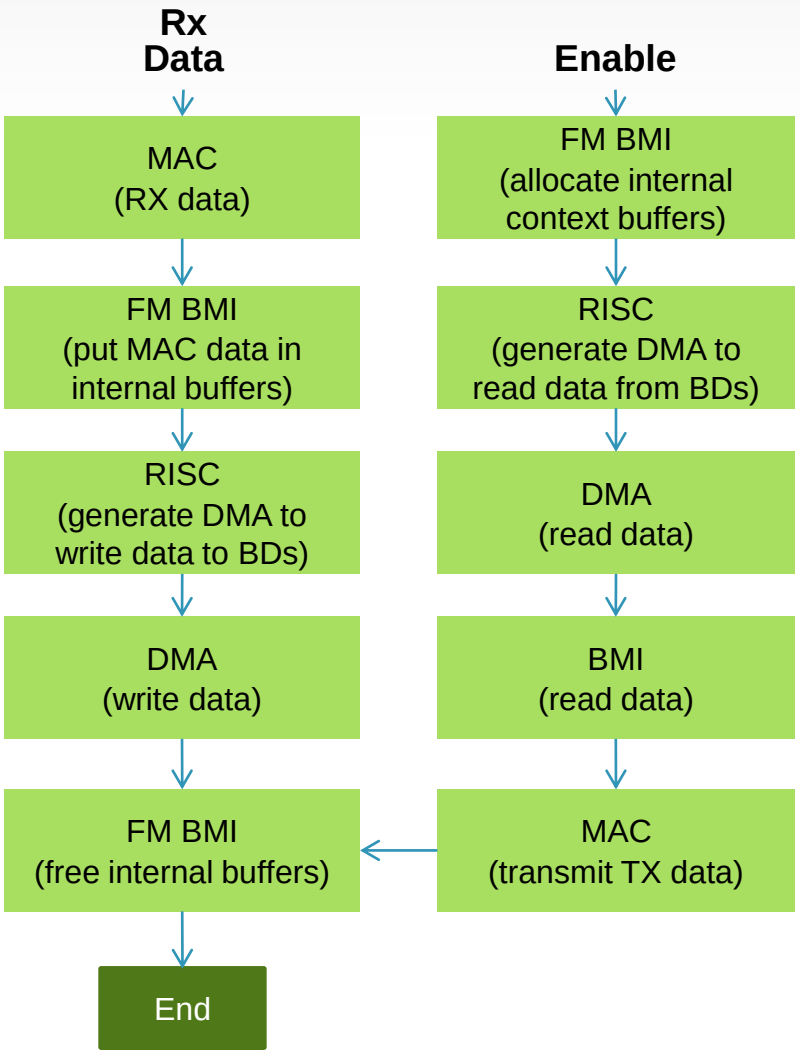
FM Init

- FMan Independent mode to get basic
- networking for tftp downloads
- Needs configuration data
- Configuration data resides at 0xEF000000



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FM Init – Independent mode

- Files:
  include/configs/corenet_ds.h
  drivers/net/fm/*
  board/freescale/corenet_ds/corenet_ds.c
- Code Snippets:

```
int board_eth_init(bd_t *bis)
{
        p5020_setup_serdes();
        /* FM 1 DTSEC */
        if (is_pcie_configured(prtcl, SGMII_FM1)) {
                printf("FM1 SGMII\n");
#ifdef CONFIG_FM1_ETH0
                SET_STD_FM_ETH_INFO(fm1_info[fm1_idx], 1, 0)
                fm1_idx++;
#endif
#ifdef CONFIG_FM1_ETH1
                SET_STD_FM_ETH_INFO(fm1_info[fm1_idx], 1, 1)
                fm1_idx++;
#endif
        :
```


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Other Pieces

- BMAN, QMAN, FMAN
  - LIODNs
  - Device tree fixups for Linux

    arch/powerpc/cpu/mpc85xx/portals.c, liodn.c

- CoreNet Platform Cache
  - Driver enabled by a flag in

    include/configs/corenet_ds.h (CONFIG_SYS_FSL_CPC)

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Add entry for build

- **Files:**

  boards.cfg

- **Code Snippets**:

  P5020DS powerpc mpc85xx corenet_ds freescale

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Building U-boot

- From command line
  - Set the compiler toolchain to compile u-boot
    - Set PATH variable on the build machine
    - Use ARCH=powerpc and CROSS_COMPILE flags

```
make CROSS_COMPILE=powerpc-linux-gnu- ARCH=powerpc distclean
make CROSS_COMPILE=powerpc-linux-gnu- ARCH=powerpc P5020DS_config
make CROSS_COMPILE=powerpc-linux-gnu- ARCH=powerpc
```

- u-boot.bin

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P5020DS NOR Flash Map Cheat Sheet

(from Bank 0 perspective after U-Boot DDR relocation)

- Work out of Bank 0 – Good u-boot
- Switch to alternate banks for testing software

0xE8000000 – 0xE8FFFFFF	Bank 0 PBL Image	Bank 7	SW7[1:4] = 0b0111 U-Boot PBL @ 0xE0000000
0xE9000000 – 0xE9FFFFFF	Bank 1 PBL Image	Bank 6	SW7[1:4] =0b0110
0xEA000000 – 0xEAFFFFFF	BANK 2 PBL Image	Bank 5	SW7[1:4] = 0b0101
0xEB000000 – 0xEBFFFFFF	Bank 3 PBL Image	Bank 4	SW7[1:4] = 0b0100
0xEC000000 – 0xECFFFFFF	Bank 4 PBL Image	Bank 3	SW7[1:4] = 0b0011
0xED000000 – 0xEDFFFFFF	Bank 5 PBL Image	Bank 2	SW7[1:4] = 0b0010
0xEE000000 – 0xEEFFFFFF	Bank 6 PBL Image	Bank 1	SW7[1:4] = 0b0001
0xEF000000 – 0xEFFFFFFF	Bank 7 PBL Image	Bank 0	SW7[1:4] = -0b0000 U-boot @ 0xEFF80000

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Common (Helpful) Commands

⇒ help

Environment variables

⇒ printenv

⇒ setenv

⇒ saveenv

NOR Flash

⇒ flinfo

⇒ erase <start addr> <end addr>

⇒ cp.b <from addr > <to addr in flash> <#bytes>

Network (Used for download)

⇒ **setenv [ipaddr][gatewayip][netmask][serverip] <ip address>**

⇒ **tftp <dest address in RAM> <file on server>**

Other

⇒ imls - Lists all u-boot recognizable images in flash

⇒ i2c - i2c commands to display, read, write i2c devices

⇒ pci - display, read, write PCI/PCIe space

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36-bit addressing

- 36-bit addressing
  - Used to support multiple partitions and resources
  - U-boot sees 4G total (P5020 u-boot leaves the processor configured processor in 32-bit mode)
  - Physical addresses of the IO are moved to the end of the 64GB address space
    - DDR address space starts at 0; now has room to expand

- Current u-boot for P3, P4, P5 includes support only for 36-bit builds

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P5020DS Linux

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Overview

- P5020 Linux overview
  - P5020 BSP Linux – Bare Metal
  - Linux Kernel Configuration
  - Device Tree

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P5020 Linux

- Use bare-metal Linux (as opposed to Linux that runs on Hypervisor) for initial bring-up

- Bare-metal Linux
  - Linux runs directly on HW
  - User state: MSR[PR]=1
  - Hypervisor state: MSR[PR]=0 MSR[GS]=0
  - Guest Supervisor state: MSR[PR]=0 MSR[GS]=1

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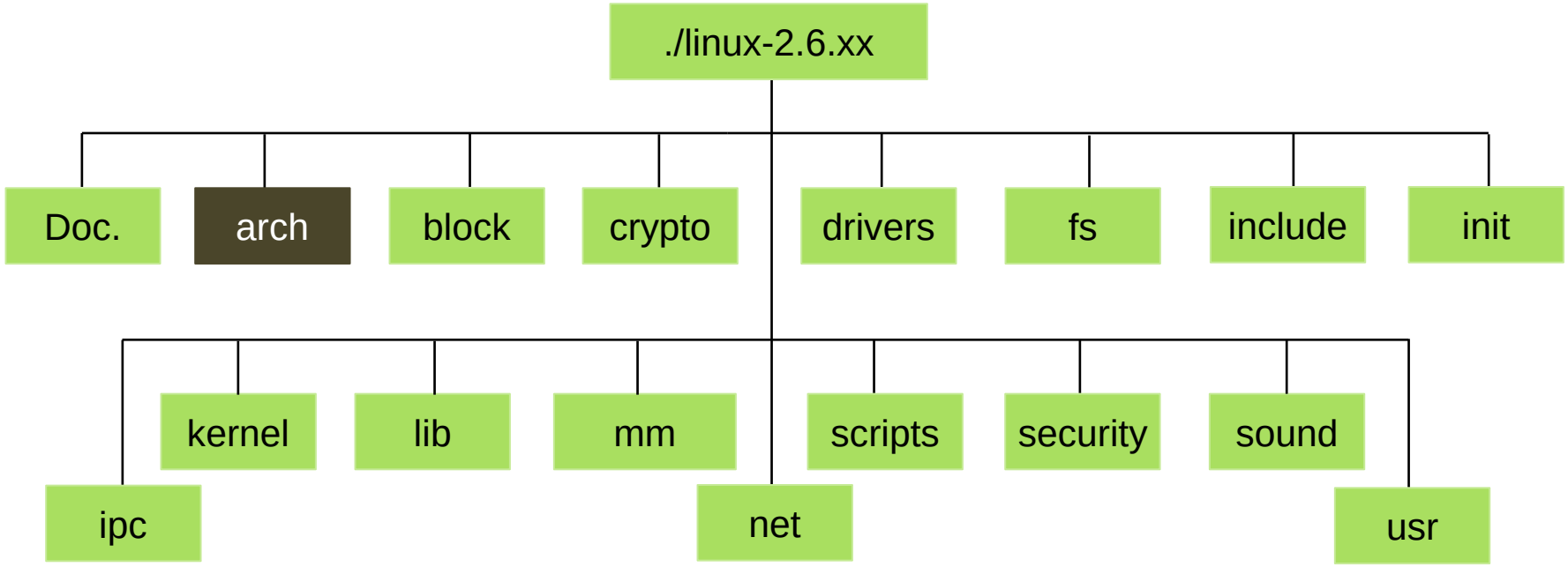
Linux Directory Structure

- arch/powerpc/boot/dts/p5020ds.dts
- arch/powerpc/configs/corenet64_smp_defconfig
- arch/powerpc/boot/
- arch/powerpc/platforms/85xx/



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Adding Platform Code

- Use existing code as example
  - Copy arch/powerpc/platforms/85xx/p5020_ds.c, corenet_ds.c
  - Make appropriate board name changes to match device tree entries
  - Makefile and Kconfig changes

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P5020 Linux Kernel Configuration

- The easiest way to create a .config file is to simply copy the appropriate config file in ./arch/powerpc/configs to .config.
- cp arch/powerpc/configs/corenet32_smp_defconfig .config

- Typing **“make menuconfig”** results in a console-based, menu-driven utility that can be used to specify the desired configuration.
  - Set CROSS_COMPILE and ARCH flags

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P5020DS Device Tree

- Data structure to describe the hardware – architecture, peripherals, system configuration
- Nodes and properties to describe the processor and platform to support in the build
- Values and flags - inputs used by the drivers
- Interrupt controller – sources description
- Interface with u-boot
- Passed to kernel during boot time

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P5020DS Device Tree - Example Nodes

```
/dts-v1/;

/ {
        model = "fsl,P5020DS";
        compatible = "fsl,P5020DS";
        #address-cells = <2>;
        #size-cells = <2>;
        interrupt-parent = <&mpic>;

 cpus {
                #address-cells = <1>;
                #size-cells = <0>;

                cpu0: PowerPC,e5500@0 {
                        device_type = "cpu";
                        reg = <0>;
                        next-level-cache = <&L2_0>;
                        L2_0: l2-cache {
                                next-level-cache =
<&cpc>;
                        };
                };
                    :
                    :
};
```

```
soc: soc@ffe000000 {
                #address-cells = <1>;
                #size-cells = <1>;
                device_type = "soc";
                compatible = "simple-bus";
                ranges = <0x00000000 0xf 0xfe000000
                                0x1000000>;
                reg = <0xf 0xfe000000 0 0x00001000>;

pci0: pcie@ffe200000 {
                compatible = "fsl,p5020-pcie", "fsl,qoriq-pcie-v2.2";
                device_type = "pci";
                #interrupt-cells = <1>;
                #size-cells = <2>;
                #address-cells = <3>;
                reg = <0xf 0xfe200000 0 0x1000>;
                bus-range = <0x0 0xff>;
                ranges = <0x02000000 0 0xe0000000 0xc 0x00000000 0x0
                                                        0x20000000
                        0x01000000 0 0x00000000 0xf 0xf8000000 0x0
                                                0x00010000>;
                clock-frequency = <0x1fca055>;
                fsl,msi = <&msi0>;
                interrupts = <16 2 1 15>;
```


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P5020DS Device Tree - U-boot Fixup Examples

- Cores
  - Timebase frequency
  - Number of cores
    - Remove extra nodes
  - Multicore boot hold-off release information
    - Reserve secondary bootpage information
  - I/D-Cache information
- L2, CPC information
- PCI Express
  - Bus ranges
- Ethernet Nodes
  - Fman frequency
  - Fman firmware inserted into device tree and point nodes
  - status
  - MDIO mux values
  - phy-handle
  - liodns

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P5020DS Device Tree

- Use the device tree compiler to build the appropriate dts file in the ./arch/powerpc/boot/dts directory.

```
dtc -I dts -O dtb -R 8 -b 0 -S 0x3000 p5020ds.dts > p5020ds.dtb
```

OR

```
make scripts (from linux-2.6/)
make p5020ds.dtb
```

- Set CROSS_COMPILE and ARCH flags

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Building Linux

- From command line

```
make CROSS_COMPILE=powerpc-linux-gnu- ARCH=powerpc menuconfig
make CROSS_COMPILE=powerpc-linux-gnu- ARCH=powerpc uImage
```


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Download and Boot Linux

U-boot commands to setup network parameters and download linux images

Network (Used for download)

⇒ setenv [ipaddr][gatewayip][netmask][serverip] <ip address>

⇒ tftp <dest address in RAM> <file on server>

Kernel, Ramdisk, DTB

⇒ tftp 1000000 uImage

⇒ tftp 2000000 rootfs.ext2.gz.uboot

⇒ tftp c00000 p5020ds.dtb

Bootargs to kernel

⇒ setenv bootargs “root=/dev/ram rw console=ttyS0,115200”

Boot command

⇒ bootm 1000000 2000000 c00000

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Summary

- Freescale development system for P5020 – P5020DS

- U-boot, Linux
  - Concepts
  - Porting
  - Building and deploying

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