DDR Basics, Register Configurations & Pitfalls

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Applications Engineer
Agenda

- **Basic DDR SDRAM**
  - Memory Organization & Operation
  - Read and write timing

- **Power QUICC DDR Controllers**
  - Features & Capabilities

- **Power QUICC DDR Controllers**
  - Initialization & Register Configurations

- **Power QUICC DDR Controllers**
  - Pitfalls / Debug Tips
Basic DDR SDRAM
Memory Organization & Operation
Single Transistor Memory Cell

Row (word) line
  
Column (bit) line
  
“1” => Vcc
“0” => Gnd

“precharged” to Vcc/2

Vcc/2

Cbit

Ccol
Single Transistor Memory Cell

Row (word) line

Column (bit) line

“1” => Vcc
“0” => Gnd

“precharged” to Vcc/2

Storage Capacitor

Vcc/2

Cbit

Ccol
Single Transistor Memory Cell

- Row (word) line
- Column (bit) line
- Access Transistor
- Storage Capacitor

- "1" => Vcc
- "0" => Gnd
- "precharged" to Vcc/2
- Vcc/2

- G
- S
- D
Single Transistor Memory Cell

Row (word) line

Column (bit) line

Access Transistor

Storage Capacitor

Vcc/2

“precharged” to Vcc/2

Parasitic Line Capacitance

“1” => Vcc

“0” => Gnd
Memory Arrays

ROW ADDRESS DECODER

B0 B1 B2 B3 B4 B5 B6 B7

W0

W1

W2

SENSE AMPS & WRITE DRIVERS

COLUMN ADDRESS DECODER
Memory Arrays

ROW ADDRESS DECODER

W0  B0  B1  B2  B3  B4  B5  B6  B7

W1

W2

SENSE AMPS & WRITE DRIVERS

COLUMN ADDRESS DECODER
Memory Arrays

![Memory Array Diagram]

- **ROW ADDRESS DECODER**
- **COLUMN ADDRESS DECODER**
- **SENSE AMPS & WRITE DRIVERS**

- B0, B1, B2, B3, B4, B5, B6, B7
Internal Memory Banks

- Multiple arrays organized into banks
- Multiple banks per memory device
  - DDR1 – 4 banks, 2 bank address (BA) bits
  - DDR2 & DDR3 – 4 or 8 banks, 2 or 3 bank address (BA) bits
  - Can have one active row in each bank at any given time
- Concurrency
  - Can be opening or precharging a row in one bank while accessing another bank
- May be referred to as “internal”, “logical” or “sub-” banks
A requested row is **ACTIVATED** and made accessible through the bank’s row buffer.

**READs** and/or **WRITE** are issued to the active row.

The row is **PRECHARGED** and is no longer accessible through the bank’s row buffer.
Example – DDR2 SDRAM

► Infineon HYB18T256800AF or Micron MT47H32M8

► 32M x 8 (8M x 8 x 4 banks)
► 256 Mb total

► 13-bit row address
  • 8K rows
► 10-bit column address
  • 1K bits/row (8K total when you take into account the x8 width)
► 2-bit bank address
Example – DDR2 DIMM

- Infineon HYS72T3200HU or Micron MT9HTF3272A
- 9 each 32M x 8 memory devices
- 32M x 72 overall
- 256 MB total
- Single “rank”
- 9 “byte lanes”
## DDR1/DDR2/DDR3 Basic Command Summary

<table>
<thead>
<tr>
<th>Command</th>
<th>/CS</th>
<th>/RAS</th>
<th>/CAS</th>
<th>/WE</th>
<th>ADDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>NOP</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>ACTIVE</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>BA, Row</td>
</tr>
<tr>
<td>READ</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>BA, Col</td>
</tr>
<tr>
<td>WRITE</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>BA, Col</td>
</tr>
<tr>
<td>PRECHARGE</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>BA</td>
</tr>
<tr>
<td>PRECHARGE ALL</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>A[10]</td>
</tr>
<tr>
<td>REFRESH</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>LOAD MODE REGISTER</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>Bank, OpCode</td>
</tr>
</tbody>
</table>
DDR2-533 Read Timing Example

- **Trcd (ACCTRORW) = 4 clk**
- **Tccd = 2 clk**
- **Trp (RD_TO_PRE) = 2 clk**
- **Trp (PRETOACT) = 4 clk**

**Mem Clk:**
- Tck = 3.75 ns

**/CS, /RAS, /CAS, /WE:**

**Address:**
- BA, ROW
- BA, COL
- BA, COL
- BA

**DQS, DQ:**
- CASLAT = 4 clk

**D0, D1, D2, D3, D0, D1, D2, D3**
DDR2-533 Write Timing Example

Mem Clk

Tck = 3.75 ns

ACTIVE

WRITE

PRECHARGE

/CS

/CRAS

/ACAS

/WE

Address

BA, ROW

BA, COL

BA

DQS

WR_LAT = CASL + AL -1 = 3 clk

Twr (WRREC) = 4 clk

DQ

DM

0 0 0 0
## DDR1/DDDR2/DDDR3 Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>DDR1</th>
<th>DDR2</th>
<th>DDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>TSOP</td>
<td>BGA only</td>
<td>BGA only</td>
</tr>
<tr>
<td>Voltages</td>
<td>2.5V Core, 2.5V I/O</td>
<td>1.8V Core, 1.8V I/O</td>
<td>1.5V Core, 1.5V I/O</td>
</tr>
<tr>
<td>Densities</td>
<td>64Mb-1Gb</td>
<td>256Mb-4Gb</td>
<td>256Mb-8Gb</td>
</tr>
<tr>
<td>Internal Banks</td>
<td>4</td>
<td>4 or 8</td>
<td>8</td>
</tr>
<tr>
<td>Prefetch (min WRITE burst)</td>
<td>2</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>Data Rate</td>
<td>266-400 Mbps</td>
<td>400–800 Mbps</td>
<td>800–1600 Mbps</td>
</tr>
<tr>
<td>CAS / READ Latency</td>
<td>2, 2.5, 3 Clk</td>
<td>3, 4, 5 + AL Clk</td>
<td>5, 6, 7+ AL Clk</td>
</tr>
<tr>
<td>WRITE Latency</td>
<td>1</td>
<td>READ Latency - 1</td>
<td>CAS write Latancy</td>
</tr>
<tr>
<td>I/O Signaling</td>
<td>SSTL_2</td>
<td>SSTL_18</td>
<td>SSTL_15</td>
</tr>
<tr>
<td>Termination</td>
<td>Parallel termination to V_TT for all signals</td>
<td>On-die for data group. V_TT termination for address, command, and control</td>
<td>On-die termination for data, address, command, and control</td>
</tr>
<tr>
<td>Data Strobes</td>
<td>Single Ended</td>
<td>Single or Differential</td>
<td>Differential</td>
</tr>
</tbody>
</table>
PowerQUICC DDR Controllers
Features & Capabilities
DDR1/DDR2/DDR3 Controller Features & Capabilities

- Supports most JEDEC standard x8, x16, x32 DDR1 & 2 & 3 devices
- Memory device densities from 64Mb – through 4Gb
- Data rates up to: 333 Mb/s for DDR1, 800 Mb/s for DDR2 and DDR3
- Devices with 12-16 row address bits, 8-11 column address bits, 2-3 logical bank address bits
- Data mask signals for sub-doubleword writes
- Up to four physical banks (chip selects)
- Physical bank sizes up to 4GB, total memory up to 16GB per controller
- Physical bank interleaving between 2 or 4 chip selects
- Memory controller interleaving when more than 2 controllers are available
- Unbuffered or registered DIMMs
DDR1/DDR2/DDR3 Controller Features & Capabilities (cont.)

► Up to 32 open pages
  • Open row table
  • Amount of time rows stay open is programmable
► Auto-precharge, globally or by chip select
► Self-refresh
► Up to 8 posted refreshes
► Automatic or software controlled memory device initialization
► ECC: 1-bit error correction, 2-bit error detection, detection of all errors within a nibble
► ECC error injection
► Read-modify-write for sub-doubleword writes when using ECC
► Automatic data initialization for ECC
► Dynamic power management
DDR2/DDR3 Controller additional Features & Capabilities

► Partial array self refresh
► Address & command parity for Registered DIMM
► Independent driver impedance setting for data, address/command, and clock
► Mirrored DIMM supported
► Automatic CPO (operational)
► Write-leveling for DDR3
► Automatic ZQ calibration for DDR3
► Fixed or On-the-fly Burst chop mode for DDR3
► Asynchronous RESET for DDR3
Fly By Routing Topology

Introduction of “Fly-by” architecture
• Address, command, control & clocks
• Improved signal integrity…enabling higher speeds
• On module termination

Matched tree routing of clk command and ctrl

Fly by routing of clk, command and ctrl
Fly By Routing Improved SI

**DDR2 Matched tree routing**

**DDR3 Fly by routing**
What is write leveling

During a write cycle, the skew between the clock and strobes are increased with the fly-by topology. The write leveling will delay the strobe (and the corresponding data lane) for each byte lane to reduce/compensate for this delay.
Instead of JEDEC’s MPR method, Freescale controllers use a proprietary method of read adjust method. Auto CPO will provide the expected arrival time of preamble for each strobe line of each byte lane during the read cycle to adjust for the delays cased by the fly-by topology.
Write leveling sequence during the initialization process will determine the appropriate delays to each strobe/data byte lane and add this delay for every write cycle.

- Write leveling used to add delay to each strobe/data line.
PowerQUICC DDR Controllers
Initialization and Register Configurations
**DDR3 Initialization Flow**

1. **Power-up**
   - Asserted at least 200us

2. **DDR Reset**
   - DDR3’s Conduct Precharge
   - Chip selects enabled and DDR clocks begin
   - Need at least 500us from reset deassertion to the controller being enabled.
   - Timed loop may be needed.

3. **DDR CTRL INIT**
   - CKE = HIGH
   - MEM_EN = 1

4. **Stable CLKS**
   - Controller Started

5. **DRAMs Initialized**
   - Mode Register Commands Issued

6. **ZQ Calibration**
   - ZQCL Issued (512 clocks)
   - Also DLL lock time is occurring

7. **Write Leveling**
   - Automatically handled by the controller

8. **Read Adjust**
   - Automatic CAS-to-Preamble (aka Read Leveling)...
   - Plus Data-to-Strobe adjustment

9. **Init Complete**
   - Ready for User accesses
DDR2 Initialization Flow

1. **Power-up**
   - DDR CTRL INIT
   - Chip selects enabled and DDR clocks begin

2. **Stable CLKS**
   - CKE = HIGH

3. **200 us**
   - Precharge All
   - DRAMs Initialized

4. **Controller Started**
   - MEM_EN = 1
   - Init Complete

   - Issued by controller
   - Mode Registers Programmed
   - tDLL = 512 clocks

   Ready for User accesses
Register configuration

► Two general type of registers to be configured in the memory controller
► First register type are set to the DRAM related parameter values, that are provided via SPD or DRAM datasheet
► Second register type are the Non-SPD values that are set based on customer’s application. For example:
  • On-die-termination (ODT) settings for DRAM and controller
  • Driver impedance setting for DRAM and controller
  • Clock adjust, write data delay, Cast to Preamble Override (CPO)
  • 2T or 3T timing
  • Burst type selection (fixed or on-fly burst chop mode)
  • Write-leveling start value (WRLVL_START)
What Can We Adjust to Optimize the Timing?

- 1) CLK_ADJUST
- 2) WR_DATA_DELAY
- 3) CPO
- 4) 2T_EN, 3T_EN
- 5) WRLVL_EN
- 6) Burst chop mode
CLK_ADJUST & WR_DATA_DELAY

Internal Clock

MemClk (CLK_ADJUST = 0)

MemClk (CLK_ADJUST = 1/2)

Cmd/Addr Bus

DQS (WR_DATA_DELAY = 0)

DQ (WR_DATA_DELAY = 0)

DQS (WR_DATA_DELAY = 1/2)

DQ (WR_DATA_DELAY = 1/2)

WR_LAT = (CASL + AL - 1) = 3

TDQSS = ± 1/4 cycle

WR_DATA_DELAY = 1/2
Pitfalls / Debug Tips - Clock Adjust

► Addr/Cmd are always launched from the same location, memory clock is shifted with DDR_SDRAM_CLK_CNTL[CLK_ADJUST]
  • Used to meet setup/hold for Addr/Cmd

► Use a scope to verify that clock is centered inside of the Addr/Cmd valid eye.
  • Look at heavily loaded signal (/RAS, /CAS, /WE, Addr, BA)
  • Look at lightly loaded signal (/CS, ODT, CKE)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0–4</td>
<td>—</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 5–8  | CLK_ADJUST | Clock adjust
        | 0000  | Clock will be launched aligned with address/command                                            |
        | 0001  | Clock will be launched 1/8 applied cycle after address/command                                 |
        | 0010  | Clock will be launched 1/4 applied cycle after address/command                                 |
        | 0011  | Clock will be launched 3/8 applied cycle after address/command                                 |
        | 0100  | Clock will be launched 1/2 applied cycle after address/command                                 |
        | 0101  | Clock will be launched 5/8 applied cycle after address/command                                 |
        | 0110  | Clock will be launched 3/4 applied cycle after address/command                                 |
        | 0111  | Clock will be launched 7/8 applied cycle after address/command                                 |
        | 1000  | Clock will be launched 1 applied cycle after address/command                                  |
        | 1001–111 | Reserved                                                                                       |
Eye Diagrams
Eye Diagrams
Eye Diagrams
Eye Diagrams
Pitfalls / Debug Tips – Write Data Delay

► Controlled via TIMING_CFG_2[WR_DATA_DELAY]

► Used to meet \( t_{DQSS} \) timing requirements
  • In addition to compensating for CLK_ADJUST setting

► Verify using a scope
  • Must be measured after DDR_SDRAM_CLK_CNTL[CLK_ADJUST] has been optimized

► Erroneous values may cause failures on writes to DRAM

<table>
<thead>
<tr>
<th>WR_DATA_DELAY</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>19–21</td>
<td>Write command to write data strobe timing adjustment. Controls the amount of delay applied to the data and data strobes for writes. See Section 9.5.9, “DDR SDRAM Write Timing Adjustments,” for details.</td>
</tr>
<tr>
<td>000</td>
<td>0 clock delay</td>
</tr>
<tr>
<td>001</td>
<td>1/4 clock delay</td>
</tr>
<tr>
<td>010</td>
<td>1/2 clock delay</td>
</tr>
<tr>
<td>011</td>
<td>3/4 clock delay</td>
</tr>
<tr>
<td>100</td>
<td>1 clock delay</td>
</tr>
<tr>
<td>101</td>
<td>5/4 clock delay</td>
</tr>
<tr>
<td>110</td>
<td>3/2 clock delay</td>
</tr>
<tr>
<td>111</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Pitfalls / Debug Tips - CAS to Preamble

- Set via TIMING_CFG_2[CPO]
- Use application note AN2583 section 4.2 to calculate
- Must be calculated after DDR_SDRAM_CLK_CNTL[CLK_ADJUST] has been optimized
- Use the center value if more than one valid CPO available.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4–8</td>
<td>CPO¹</td>
<td>MCAS-to-preamble override. Defines the number of DRAM cycles between when a read is issued and when the corresponding DQS preamble is valid for the memory controller. For these decodings, “READ_LAT” is equal to the CAS latency plus the additive latency.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00000  READ_LAT + 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00001  Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00010  READ_LAT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00011  READ_LAT + 1/4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00100  READ_LAT + 1/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00101  READ_LAT + 3/4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00110  READ_LAT + 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00111  READ_LAT + 5/4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01000  READ_LAT + 3/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01001  READ_LAT + 7/4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01010  READ_LAT + 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01011  READ_LAT + 9/4</td>
</tr>
</tbody>
</table>
2T/3T Timing

- Puts Addr/Cmd signals on the bus for 2 or 3 clock cycles instead of 1
- Does not affect Control signals

When to use?
- Two dual-rank unbuffered DIMMs
- 36 loads on Addr/Cmd lines

Typically not required for:
- One dual-rank unbuffered DIMM
- 18 loads on Addr/Cmd lines

When not to use?
- Registered DIMMs
PowerQUICC DDR Controllers
Pitfalls / Debug Tips
### Pitfalls / Debug Tips - DDR Type POR Configuration

#### Table 4-16. DDR DRAM Type

<table>
<thead>
<tr>
<th>Functional Signal</th>
<th>Reset Configuration Name</th>
<th>Value (Binary)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>LGPL0, LGPL1</td>
<td>cfg_dram_type[0:1]</td>
<td>00</td>
<td>Reserved</td>
</tr>
<tr>
<td>Default (11)</td>
<td></td>
<td>01</td>
<td>DDR1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.5V, CKE low at reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td>DDR2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.8V, CKE low at reset (default)</td>
</tr>
</tbody>
</table>

#### Table 4-20. DDR DRAM Type

<table>
<thead>
<tr>
<th>Functional Signal</th>
<th>Reset Configuration Name</th>
<th>Value (Binary)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>LGPL0/LFCLE</td>
<td>cfg_dram_type</td>
<td>0</td>
<td>DDR3</td>
</tr>
<tr>
<td>Default (1)</td>
<td></td>
<td></td>
<td>1.5 V, CKE low at reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>DDR2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.8 V, CKE low at reset (default)</td>
</tr>
</tbody>
</table>
Pitfalls / Debug Tips - ECC and DDR Error Registers

► ECC should be enabled if possible
  • DDR_SDRAM_CFG[ECC_EN] enables ECC
  • DDR_SDRAM_CFG_2[D_INIT] initializes data and ECC in DRAM
  • If ECC cannot be enabled, it may be more difficult to detect DDR generated errors

► ERR_DETECT register should be checked for DDR errors
  • ACE – Automatic calibration error
  • MBE – Multi-bit ECC error
  • SBE – Single-bit ECC error
  • MSE – Memory select error
Program write latency based on DRAM type

- DDR1 -> Write latency = 1 DRAM cycle
- DDR2 -> Write latency = (Read latency – 1) DRAM cycles
- DDR3 -> Write latency = CWL

Programming CAS latency too high can degrade performance

- Check DRAM datasheet based on frequency used and specific DRAM device

When ODT is used, other rules must be followed to allow ODT to assert early enough

- DDR2: Write latency + additive latency >= 3 cycles
- DDR3: TIMING_CFG_5 [WODT_ON], [WODT_OFF] = WL-1 cycles for fixed or fly-by burst chop
Pitfalls / Debug Tips - DDR Mode Registers

- Values programmed into DDR mode registers must match DDR controller configuration registers
  - CAS latency
  - Burst length
  - Write recovery
    - Not a straight decode in Mode Register
  - Active powerdown exit time
  - Additive latency
  - Differential DQS enable

- DLL reset and OCD calibration fields are controlled automatically by the DDR controller
*Pitfalls / Debug Tips - Programming twtr, trrd, and trtp

Use caution when calculating:

- TIMING_CFG_1[WRTORD] (twtr)
- TIMING_CFG_1[ACTTOACT] (trrd)
- TIMING_CFG_2[RD_TO_PRE] (trtp)
- DDR2: Minimum value for each parameter is 2 DRAM clocks
- DDR3: Minimum value for each parameter is 4 DRAM clocks
Pitfalls / Debug Tips - 200 us Delay

- 200 μs for DDR2 and 512 us for DDR3 must pass between stable clocks and CKE assertion

- Clocks are stable after DDR_SDRAM_CLK_CNTL[CLK_ADJUST] is programmed and any chip select has been enabled via CSn_CONFIG[CS_n_EN]

- CKE is asserted after DDR_SDRAM_CFG[MEM_EN] is set

- Software must provide delay between these 2 steps
References
Useful References

▶ Books:

▶ Freescale AppNotes:
  • AN2582 Hardware and Layout Design Considerations for DDR Memory Interfaces
  • AN2910 Hardware and Layout Design Considerations for DDR2 Memory Interfaces
  • AN2583 Programming the PowerQUICC III / PowerQUICC II Pro DDR SDRAM Controller
  • AN3369 PowerQUICC DDR2 SDRAM Controller Register Setting Considerations

▶ Micron AppNotes:
  • TN-46-05 General DDR SDRAM Functionality
  • TN-47-02 DDR2 Offers New Features and Functionality
  • TN-41-02 DDR3 ZQ calibration

▶ JEDEC Specs:
  • JESD79E Double Data Rate (DDR) SDRAM Specification
  • JESD79-2B DDR2 SDRAM Specification
  • JESD79-3A DDR3 SDRAM Specification
Thank you for attending this presentation. We’ll now take a few moments for the audience’s questions and then we’ll begin the question and answer session.