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DDR3 Design Considerations for PCB Applications

AN111

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Introduction

► Customers are beginning to inquire and / or expect DDR3 support on their new product offerings, especially as the price cross-over point nears.

► The first device with DDR3 support was 8572.

► The first development system with DDR3 will be P2020.

► As such, more and more FSL products are supporting DDR3 moving forward.

► In this session we will look at key distinctions between DDR3 vs. DDR1 & DDR2, with key emphasis placed on elements that are important to hardware / board design engineers.
Overview of Presentation

- DDR3 SDRAM Attributes.
- DDR Controller Highlights.
- DDR3 Signaling.
- DDR3 Routing Methodology.
- Memory Pins, New Features.
- PCB Design Pitfalls.
DDR3 – Same players

- Supported by all major memory vendors

[Logos of Micron, ELPIDA, Samsung, Hynix, Infineon, Qimonda, and Nanya]
Cross-over Point

<table>
<thead>
<tr>
<th></th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td>14%</td>
<td>3%</td>
<td>2%</td>
<td>1%</td>
</tr>
<tr>
<td>DDR2</td>
<td>83%</td>
<td>78%</td>
<td>64%</td>
<td>33%</td>
</tr>
<tr>
<td>DDR3</td>
<td>3%</td>
<td>19%</td>
<td>34%</td>
<td>60%</td>
</tr>
</tbody>
</table>
## DDR SDRAM Highlights and Comparison

<table>
<thead>
<tr>
<th>Feature/Category</th>
<th>DDR1</th>
<th>DDR2</th>
<th>DDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>TSOP</td>
<td>BGA only</td>
<td>BGA only</td>
</tr>
<tr>
<td>Densities</td>
<td>128Mb -1Gb</td>
<td>256Mb - 4Gb</td>
<td>512Mb -8Gb</td>
</tr>
<tr>
<td>Voltage</td>
<td>2.5V Core, 2.5V I/O</td>
<td>1.8V Core, 1.8V I/O</td>
<td>1.5V Core, 1.5V I/O</td>
</tr>
<tr>
<td>I/O Signaling</td>
<td>SSTL_2</td>
<td>SSTL_18</td>
<td>SSTL_15</td>
</tr>
<tr>
<td>Internal Memory Banks</td>
<td>4</td>
<td>4 to 8</td>
<td>8</td>
</tr>
<tr>
<td>Data Rate</td>
<td>200-400 Mbps</td>
<td>400–800 Mbps</td>
<td>800–1600 Mbps</td>
</tr>
<tr>
<td>Termination</td>
<td>Motherboard termination to $V_{TT}$ for all signals</td>
<td>On-die termination for data group. $V_{TT}$ termination for address, command, and control</td>
<td>On-die termination for data group. $V_{TT}$ termination for address, command, and control</td>
</tr>
<tr>
<td>Data Strobes</td>
<td>Single Ended</td>
<td>Differential or single</td>
<td>Differential</td>
</tr>
</tbody>
</table>
### DDR SDRAM Highlights and Comparison (cont.)

<table>
<thead>
<tr>
<th>Feature/Category</th>
<th>DDR1</th>
<th>DDR2</th>
<th>DDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Burst Length</td>
<td>BL= 2, 4, 8 (2-bit prefetch)</td>
<td>BL= 4, 8 (4-bit prefetch)</td>
<td>BL= 8 (Burst chop 4) (8-bit prefetch)</td>
</tr>
<tr>
<td>CL/tRCD/tRP</td>
<td>15 ns each</td>
<td>15 ns each</td>
<td>12 ns each</td>
</tr>
<tr>
<td>Master Reset</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>ODT (On-die termination)</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Driver Calibration</td>
<td>No</td>
<td>Off-Chip (OCD)</td>
<td>On-Chip with ZQ pin (ZQ cal)</td>
</tr>
<tr>
<td>Write Leveling</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Typical Freescale DDR2/3 Controller Highlights

► Interface speed
  • DDR2 - up to 800 MHz
  • DDR3 - up to 800 MHz today (MPC8572, MPC8526)
    ▪ Evaluating higher speeds 1066 MHz and up to 1600 MHz

► Support Interface width
  • 64/72-bit data bus – high end product
  • 32/40-bit data bus – low end products
  • 16/24-bit data bus – low end products

► Discrete, unbuffered, and registered DIMM support
  • Memory device densities from 64Mb – through 8Gb
  • Up to four chip selects supported
  • Support for x8/x16 DDR devices – x4 devices are not supported

► Full ECC (Error Correction Code) support
  • Single error correction/detection, double error detection
  • Error injection for software development

► Self refresh support
Typical Freescale DDR2/3 Controller Highlights (cont’d)

► Read-Modify-Write support for Atomic Inc, Dec, Set, Clear, and sub-double word writes
► All timing parameters are under SW control
► Automatic Data Initialization (easy ECC support)
► Differential data strobes
► Dedicated Open Row Table for each sub-bank
  • Up to 32 simultaneous open rows with 4 chip selects
► Up to six diff clock pairs
  • Eliminates the need for any external clock PLLs
► ODT support (both internally and externally)
► On-chip ZQ driver calibration
► SSTL-1.8, and SSTL-1.5 compatible IOs
Key DDR3 Memory Improvements and Additions

► Lower signaling standard
► Reduced power
► Improved device pinout
► Fly-by architecture
► Write Leveling
► Dynamic ODT for improved Write signaling
► Driver calibration
► Device Reset
► DIMM address mirroring
DDR3 Signaling – Example SSTL-1.5

Transmitter

VDDQ (1.5V nominal)

VOH(MIN)

0.925V

0.850V

0.765V

0.750V

0.735V

0.650V

0.575V

VOL (MAX)

VSSQ

Receiver

ViHAC

ViHDC

VREF + AC Noise

VREF + DC Error

VREF - DC Error

VREF - AC Noise

VILDC

VILAC

Freescale Semiconductor Confidential and Proprietary Information. Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2007.
- Supply voltage reduced from 1.8V to 1.5V
  - ~ 30% power reduction (Micron claim)
  - ~ 25% is JEDEC’s official claim
    - Compared to DDR2 at same frequency bin

- Lower I/O buffer power
  - 34 ohm driver vs. 18 ohm driver at memory device

- Improved bandwidth per Watt

![Graph showing power relative to DDR2 for different DDR and DDR3 speeds. DDR2 533, DDR2 667, DDR2 800, DDR3 1067, DDR3 1333, DDR3 1600.](image)
Improved Pinout

► Improved power delivery
  • More power and ground balls

► Improved signal quality
  • Better power & ground distribution
  • And better signal referencing

► Fully populated ball grid
  • Stronger reliability

► Improved pin placement
  • Less pin skew
  • Tighter timing leaving chip
Fly By Routing Topology

Introduction of “Fly-by” architecture

- Address, command, control & clocks
- Improved signal integrity…enabling higher speeds
- On module termination
Fly By Routing Improved SI

**DDR2 Matched tree routing**

**DDR3 Fly by routing**
Fly By Skew Across All receivers

This illustrates the skew created by DDR3 fly by routing
The need for write-leveling....

- **tDQSS requirement:**
  - DQS/DQS# rising edge to CK/CK# rising edge
  - Clock to Strobe should be within a certain range for proper write operation to DDR3 SDRAMs
- **tDQSS spec:** +/- 0.25*tck
Write-Leveling… How it works
Read Adjustment

- Automatic CAS to preamble calibration
- Data strobe to data skew adjustment

Instead of JEDEC’s MPR method, Freescale controllers use a proprietary method of read adjust method which will work with DDR2 and DDR3. This provides comparable performance to JEDEC’s DDR3 MPR method.
Dynamic ODT – System Motivation

Example of termination scheme in application

<table>
<thead>
<tr>
<th>Transaction</th>
<th>Slot 1</th>
<th>Slot 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write to Slot 1</td>
<td>RTT_WR = 120 Ω</td>
<td>RTTNom = 20 Ω</td>
</tr>
<tr>
<td>Write to Slot 2</td>
<td>RTTNom = 20 Ω</td>
<td>RTT_WR = 120 Ω</td>
</tr>
</tbody>
</table>

Write to slot 1

Write to slot 2

Without Dynamic ODT

With Dynamic ODT

Significant improvement of write signal integrity with DDR3 dynamic ODT
New DDR3 Pins

Introduction of an asynchronous RESET# pin

- Prevent Illegal commands and/or unwanted states
  - Cold reset
  - Warm reset
- Known initialization
  - Resets all state information
  - No power-down required
  - Destructive to data contents
New DDR3 Pins… cont’d

► VREF broken into separate banks (..at the DDR3 memories)
  • VREFCA
    ▪ Used for the command / address signals
    ▪ Decoupled to VDD plane
  • VREFDQ
    ▪ Used for the data signals
    ▪ Decoupled to VDD plane

► Key premise – Noise reduction and coupling between the groups

At the DDR3 controller the same source driving VREFDQ to the memories would drive the controller VREF pin.
NEW DDR3 pins – ZQ Calibration Pin

► The RZQ resistor is connected between the DDR3 memory and ground
  • Value = 240 Ohm +/- 1%
  • Permits driver and ODT calibration over process, voltage, and temperatures

► Easier and more accepted than DDR2’s (optional) OCD method.

► Our controllers support both ZQ calibration commands
  • ZQCL – used during initialization (..takes longer)
  • ZQCS – used during normal operation (…periodic and takes less time)

Table 9-26. DDR_ZQ_CNTL Field Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ZQ_EN</td>
<td>ZQ Calibration Enable. This bit determines if ZQ calibrating will be used. This bit should only be set if DDR3 memory is used (DDR_SDRAM_CFG[SDRAM_TYPE] = 3'b111). 0 ZQ Calibration will not be used. 1 ZQ Calibration will be used. A ZQCL command will be issued by the DDR controller after POR and anytime the DDR controller is exiting self refresh. A ZQCS command will be issued every 32 refresh sequences to account for VT variations.</td>
</tr>
</tbody>
</table>
Freescale Controller Driver Calibration

► Our Freescale controller also does driver calibration
  • Enabled by software
  • Occurs automatically during initialization after MEM_EN is set

► MDIC precision resistors are used at our controller
  • Value = 40 Ohms 1% tolerance
DIMM Mirroring...

The DDR3 IP fully supports address mirroring

<table>
<thead>
<tr>
<th>Edge Connector Signal</th>
<th>SDRAM Pin, Standard</th>
<th>SDRAM Pin, Mirrored</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>A0</td>
<td>A0</td>
</tr>
<tr>
<td>A1</td>
<td>A1</td>
<td>A1</td>
</tr>
<tr>
<td>A2</td>
<td>A2</td>
<td>A2</td>
</tr>
<tr>
<td>A3</td>
<td>A3</td>
<td>A4</td>
</tr>
<tr>
<td>A4</td>
<td>A4</td>
<td>A3</td>
</tr>
<tr>
<td>A5</td>
<td>A5</td>
<td>A6</td>
</tr>
<tr>
<td>A6</td>
<td>A6</td>
<td>A5</td>
</tr>
<tr>
<td>A7</td>
<td>A7</td>
<td>A8</td>
</tr>
<tr>
<td>A8</td>
<td>A8</td>
<td>A7</td>
</tr>
<tr>
<td>A9</td>
<td>A9</td>
<td>A9</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>A15</td>
<td>A15</td>
<td>A15</td>
</tr>
<tr>
<td>BA0</td>
<td>BA0</td>
<td>BA1</td>
</tr>
<tr>
<td>BA1</td>
<td>BA1</td>
<td>BA0</td>
</tr>
<tr>
<td>BA2</td>
<td>BA2</td>
<td>BA2</td>
</tr>
</tbody>
</table>

Non-Mirrored  Mirrored
NEW DDR3 pins – TDQS/TDQS#

► TDQS/TDQS# New pin on x8 DDR3 devices
  • Not present on x4 or x16 devices
  • Allows combinations of x4/x8 devices in the same system.

► We don’t support TDQS/TDQS#
  • We do not support x4 devices… so this function is not supported
Byte lane routing example
120 Ohm / Half Driver / 1 DIMM

Good margins across all data beats

Required
Tsu = 95 ps
Th = 170 ps

<table>
<thead>
<tr>
<th>Measured Setup (Average)</th>
<th>646 ps</th>
<th>443 ps</th>
<th>440 ps</th>
<th>452 ps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured Hold (Average)</td>
<td>427 ps</td>
<td>405 ps</td>
<td>432 ps</td>
<td>850 ps</td>
</tr>
</tbody>
</table>
Common Design Pitfalls
Design Pitfalls Summary

- Pitfall 1 Noisy Vref: Care must be taken to isolate Vref
- Pitfall 2 Weak Vref: Insure adequate current for Vref
- Pitfall 3 Ref Plane: Insure excellent reference plane for all DDR signals
- Pitfall 4 Data Tuning: Data bits within 10 mil, Byte lanes within 0.5”
- Pitfall 5 Proper Termination: Discrete implementations require term.
- Pitfall 6 POR Config: Insure correct DDR (2/3) is set for controller
- Pitfall 7 Expandability: Hook up unused address lines
- Pitfall 8 Incorrect Topology: Insure use of JEDEC routing topologies
- Pitfall 9 Separate VDDQ/VDDIO: VDDQ and VDDIO are common on DDR DIMM Modules, not on controller.
Design Pitfalls Summary (Continued)

► Pitfall 10 Slew Rate: Must account for de-rated slew rate for system timing (See JEDEC Table)

► Pitfall 11 Testability: Insure there is test and measurement access to DDR signals

► Some other noteworthy pitfalls
  • Not using ECC
    ▪ Highly Recommended for first prototypes. De-pop for production
  • Missing pull-up on MAPAR_ERR (registered DIMMs) and MAPAR_OUT
Design Pitfalls
Backup Slides
Pitfall 1 – Noisy VREF

Figure 80 — Illustration of $V_{\text{Ref}(\text{DC})}$ tolerance and $V_{\text{Ref} \text{ac-noise}}$ limits

- $V_{\text{Ref}(t)}$ may temporarily deviate from $V_{\text{Ref}(\text{DC})}$ by no more than $\pm \ 1\% \ V_{\text{DD}}$
- $V_{\text{Ref}(\text{DC})}$ is the linear average of $V_{\text{Ref}(t)}$ over a very long period of time (e.g. 1 sec)
Pitfall 1 – Measuring $V_{REF}$

- Measuring at device will likely give greater than 50 mV peak-to-peak
  - Result of coupled noise from DDR device
- $V_{REF}$ system noise should be measured at capacitor nearest the memory device
### Pitfall 1 – Protecting VREF

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VREF</strong></td>
<td></td>
</tr>
<tr>
<td>18.</td>
<td>Has $V_{REF}$ been routed with a wide trace? (Minimum of 20–25 mil recommended.)</td>
</tr>
<tr>
<td>19.</td>
<td>Has $V_{REF}$ been isolated from noisy aggressors? In addition, maintain at least a 20–25 mil clearance from $V_{REF}$ to other traces. If possible, isolate $V_{REF}$ with adjacent ground traces.</td>
</tr>
<tr>
<td>20.</td>
<td>Has $V_{REF}$ been proper decoupled? Specifically, decouple the source and each destination pin with 0.1uf caps.</td>
</tr>
</tbody>
</table>
Pitfall 2 – Wimpy $V_{\text{REF}}$ source

- $V_{\text{REF}}$ current consumption is typically 1.5-2.0 mA
- For most DDR regulators…. this is easily handled
Pitfall 3 – Reference Plane discontinuities

► Contiguous reference plane
  • GND – Data
  • Pwr – Address / Cmd
► Use stitching vias if switching layers

► Keep away from plane voids
► Avoid crossing plane splits
► Avoid trace over anti-pad
Pitfall 4 – Data Tuning

Within byte lane +/- 10 mil

Across all byte lanes match to within 0.5 inches
Pitfall 5 – Forgetting Termination

Still needed for soldered-down implementations.

DIMM modules have the termination on the module.
Pitfall 6 – POR config selection

Table 4-18. DDR DRAM Type

<table>
<thead>
<tr>
<th>Functional Signal</th>
<th>Reset Configuration Name</th>
<th>Value (Binary)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSEC2_TXD[1]</td>
<td>cfg_dram_type</td>
<td>0</td>
<td>DDR2 1.8V, CKE low at reset</td>
</tr>
<tr>
<td>Default (1)</td>
<td></td>
<td>1</td>
<td>DDR3 1.5V, CKE low at reset (default)</td>
</tr>
</tbody>
</table>

Above example assumes 8572. Other devices may utilize a different functional pin for the POR setting.
Pitfall 7 – Expandability

Rule of thumb:
For DDR3 - Every address (A0-A15), and all three bank address (BA0-BA2) line from our controllers should be connected to the memory subsystem.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Pin Nomenclature</th>
<th>Signal Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A13</td>
<td>NC</td>
<td>No connection to internal die. Okay to run trace to PCB pad.</td>
<td>Used on x4/x8 512 Mb and 1 Gb devices and all configurations of the 2 Gb or 4 Gb.</td>
</tr>
<tr>
<td>A14</td>
<td>NC</td>
<td>No connection to internal die. Okay to run trace to PCB pad.</td>
<td>Used on x4/x8 2 Gb devices and all 4 Gb configurations.</td>
</tr>
<tr>
<td>A15</td>
<td>NC</td>
<td>No connection to internal die. Okay to run trace to PCB pad.</td>
<td>Used on 4 Gb (x4/x8).</td>
</tr>
<tr>
<td>BA2</td>
<td>NC</td>
<td>No connection to internal die. Okay to run trace to PCB pad.</td>
<td>Used on all configurations of the 1 Gb, 2 Gb, and 4 Gb.</td>
</tr>
</tbody>
</table>
Pitfall 8 – Not using proven JEDEC topologies
Pitfall 9 – Separate VDDQ/VDDIO

- **PowerQUICC® Controller**
- **VDDQ (io pwr)**
- **VDD (ddr pwr)**

Separate planes are not viable with standard JEDEC DIMM memory modules.

VDDQ & VDDIO are same plane on the modules.
Pitfall 10– Slew Rate De-rating (setup & hold)

Table 47 — Derating values for DDR2-667, DDR2-800

<table>
<thead>
<tr>
<th>CK/CK Differential Slew Rate</th>
<th>VIL,AC</th>
<th>1.5 V/ns</th>
<th>1.6 V/ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+159</td>
<td>+153</td>
<td>+153</td>
</tr>
<tr>
<td>1</td>
<td>+150</td>
<td>+150</td>
<td>+150</td>
</tr>
<tr>
<td>1</td>
<td>+150</td>
<td>+150</td>
<td>+150</td>
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<td>+150</td>
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<td>+150</td>
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</tr>
<tr>
<td>1</td>
<td>+150</td>
<td>+150</td>
<td>+150</td>
</tr>
</tbody>
</table>

Source: JEDEC 79-2C

Source: Xcell Journal

Tangent line slew rate for de-rating
Correct valid eye time wrt to voltage margin
Pitfall 11 – No debug or testability on BGA devices
Power up and Initialization Sequence
Backup Slides
DDR3 Initialization Flow

Power-up

DDR Reset

- Asserted at least 200us
- DDR3’s Conduct Precharge

DDR CTRL INIT

- Chip selects enabled and DDR clocks begin

Stable CLKS

Controller Started

- CKE = HIGH
- MEM_EN = 1

DRAMs Initialized

Mode Register Commands Issued

ZQ Calibration

ZQCL Issued (512 clocks)
Also DLL lock time is occurring

Write Leveling

Read Adjust

- Automatically handled
  By the controller
- Automatic CAS-to-Preamble
  (aka Read Leveling)....
  Plus Data-to-Strobe adjustment

Init Complete

- Ready for User accesses

Need at least 500us from reset deassertion to the controller being enabled.

Timed loop may be needed.
DDR2 Initialization Flow

1. **Power-up**
   - Chip selects enabled and DDR clocks begin

2. **DDR CTRL INIT**
   - CKE = HIGH

3. **Stable CLKS**
   - 200 us

4. **Controller Started**
   - MEM_EN = 1

5. **Precharge All**
   - Issued by controller

6. **DRAMs Initialized**
   - Mode Registers Programmed
   - Issued by controller

7. **Wait t_{DLL}**
   - t_{DLL} = 512 clocks

8. **Init Complete**
   - Ready for User accesses
Burst Length

 ► Burst Length control (BC4/8 on the fly)
   • 8-bit pre-fetch is standard for DDR3 memories
   • Thus, burst length of 8 is default

 DDR3’s also support ‘pseudo BL4’ using burst chip
Power-up : Power Rails

DDR3 memories have two power pins defined.

- Same voltage level of 1.5V nominal
- Separate pins help reduce power supply noise/interruption
  - VDD – Core Power
  - VDDQ – IO Power

Therefore, there will be 2 different cases:

- Case 1 – two separate sources
- Case 2 – Single voltage source for both rails
The following should be applied whether a single voltage source or a separate voltage sources are used:

- **Apply Power:**
  - \( \text{RESET#} \) is recommended to be maintained below \( 0.2V \times VDD \) (min 200us) and all other inputs may be undefined
  - The voltage ramp time between 300mV to \( VDD_{\text{min}} \) must be no greater than 200ms
    - \( VDD > VDDQ, VDD-VDDQ < 0.3V \)
  - The voltage levels on all other pins should not exceed \( VDD/VDDQ \) or be below \( VSS/VSSQ \)
Starting with DDR3, a reset function is supported
• All devices have a dedicated RESET# pin, operating at CMOS levels
• Low pass filter incorporated – prevents accidental glitches
• Voltage level of the pin should be carefully maintained to prevent loss of data

Reset should be done after the power supply voltage level(s) are properly up and stabilized

Reset can also be issued whenever “Warm-booting” is needed.

Destructive to data contents, therefore memories will need to be re-initialized
Stable clocks

- Clocks are started as soon as a chip select is enabled.
  - Controller will ensure that the appropriate clock to CKE relationship is met
Once clocks are stabilized, the next step should be to set the Mode Register.

- Mode Registers set the operational mode of the DDR3 DRAMs
- Order of programming
  - MR2 -> MR3 -> MR1 -> MR0

Several new features for DDR3, such as
- MR0: Burst length control (BC4/8 on the fly)
- MR1: Write leveling enable
- MR2: RTT_WR, CWL, ASR
Mode Register Set 0

Address Field

Mode Register 0

Write recovery for autorecharge

<table>
<thead>
<tr>
<th>A11</th>
<th>A10</th>
<th>A9</th>
<th>WR(cycles)</th>
<th>BL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Reserved</td>
<td>8</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>3*2</td>
<td>4</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>6*2</td>
<td>7</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>7*2</td>
<td>8</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>8*2</td>
<td>9</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>10*2</td>
<td>10</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>12*2</td>
<td>11</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
<td>12</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A3</th>
<th>Read Burst Type</th>
<th>A1</th>
<th>A0</th>
<th>BL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Nibble Sequential</td>
<td>0</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>1</td>
<td>Interleave</td>
<td>0</td>
<td>1</td>
<td>4 or 8 (on the fly)</td>
</tr>
<tr>
<td></td>
<td>Item #1586.05.06 (Mar. '05)</td>
<td>1</td>
<td>0</td>
<td>4 (Fixed)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A12</th>
<th>DLL Control for Precharge PD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Slow exit (DLL off)</td>
</tr>
<tr>
<td>1</td>
<td>Fast exit (DLL on)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A11</th>
<th>A10</th>
<th>A9</th>
<th>MR Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MR0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>MR1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>MR2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>MR3</td>
</tr>
</tbody>
</table>
Mode Register Set 2

MR2 Programming

Address Field

Mode Register 2

A7: Self-Refresh Temperature (SRT) Range
0: Normal operating temperature range
1: Extended (optional) operating temperature range

A6: Auto Self-Refresh (ASR)
0: Manual SR Reference (SRT)
1: ASR enable (Optional)

A5

A4

A3

A2 A1 A0 Partial Array Self-Refresh (Optional)
0 0 0 Full Array
0 0 1 Half Array (BA[2:0]=000, 001, 010, & 011)
0 1 0 Quarter Array (BA[2:0]=000, & 001)
0 1 1 Half Array (BA[2:0]=000)
1 0 0 3/4 Array (BA[2:0]=010,011,100,101,110, & 111)
1 0 1 Half Array (BA[2:0]=100, 101, 110, & 111)
1 1 0 Quarter Array (BA[2:0]=110, & 111)
1 1 1 1/8th Array (BA[2:0]=111)

A10 A9 R/W
0 0 Dynamic ODT Off (Write does not affect R/W value)
0 1 RZO4
1 0 RZQ2
1 1 Reserved

A3 A2 CAS write Latency (CWL)
0 0 0 5 (tCK > 2.5ns)
0 0 1 6 (2.5ns < tCK < 1.875ns)
0 1 0 7 (1.875ns < tCK < 1.5ns)
0 1 1 8 (1.5ns < tCK < 1.25ns)
1 0 0 Reserved
1 0 1 Reserved
1 1 0 Reserved
1 1 1 Reserved

BA1 BA0 MR Select
0 0 MR0
0 1 MR1
1 0 MR2
1 1 MR3
Driver Calibration

- DDR3 SDRAMs require a ZQ resistor (240ohm +/- 1%) external to the device.
  - Used as a reference for driver and ODT calibration
  - Allows both to remain stable – independent of thermal variation during operation

- Therefore, the last step in the initialization process is ZQ_long calibration sequence – after which the DDR3 memories are now ready for normal operation