Comparison of High-Speed Interconnects: Ethernet, PCI Express® and RapidIO® Technology

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Agenda

► Interconnect Trends

► Technical Overview

► Comparison

► Summary and Conclusion
Our Customer Feedback on Interconnects

- I want more CPU cycles → Quit spending them moving data
- I don’t want to change next time → Support living standards with a living ecosystem
- I want to meet my technical requirements → Implement QoS, scalable BW, multicore ready, high availability…
- I don’t want to rewrite my software → Use common usage models and software APIs
- I want it cheap → Use multi-vendor standards
Interconnect Trends

1st Generation Point-to-Point
- Packet switched
- PHY: Source-sync differential
- Lowest pin count
Example: HT/P-RapidIO® ≤ 3 GHz

Hierarchical Bus
- Bridged Hierarchy
- Broadcast
- PHY: Single-ended
Example: PCI/PCI-X/SCSI ≤ 133MHz

Shared Bus
- Single segment
- Broadcast
- PHY: Single-ended
- Highest pin count
Example: VME ≤ 66MHz

2nd Generation Point-to-Point
- Packet switched
- PHY: SERDES differential
- Lowest pin count

Ex: PCIe, S-RapidIO, SATA, SAS ≥ 10 GHz
Interconnect Roles

- Chip-to-chip
- Board-to-Device
- Board-to-board
- Chassis-to-chassis
Technical Overview
Ethernet Overview

- **WAN scale interconnect**
  - Box-to-box, board-to-board, backplane
  - Connect thousands to millions of endpoints
  - Physical layer defined for LAN-scale interconnection
    - Closet to computer
    - Backplane
  - Optical, twisted pair and backplane copper media
- **Target market**
  - GigE WAN to workstations, PCs and laptops
  - 10GE now used in aggregation settings
    - High performance switches, routers and LAN backbones
- **Specification history**
  - First spec (10Mbps) ~1975 by Xerox
  - 100Mbps spec in 1995
  - 1Gbps spec in 1998
  - 10Gbps spec in 2002
    - 10G Copper (10GBase-T) in 2006
  - Recent relevant additions
    - Backplane Ethernet (802.3ap-2007)
    - Data Center Bridging (DCB)
- **Gigabit Ethernet ubiquitous now**
  - 10G Copper PHYs shipping
- **Extensible layered specification**
- **Point-to-point packetized architecture**
  - High header overhead
  - Variable packet size
  - 46-1500 byte packet L2 PDU
  - Up to 9000 byte jumbo frames
Layer 2 Packet Type: 1500 Byte Max Packet PDU

Total = 294 Bytes
(256 Byte PDU)
Ethernet + TCP/IP

TCP/IP Packet Type: 1460 Byte Max User PDU

Total = 334 Bytes
(256 Byte User PDU)
PCI Express® Overview

- Chassis-scale interconnect
  - Chip-to-chip, Board-to-board
  - Required legacy PCI compatibility
  - Physical layer defined for board + connector
  - Copper-on-board and cable media
- Successor to PCI 2.3/PCI-X 2.0
  - Fully SW/firmware backward compatible to PCI
- Target market
  - PC and Servers space
  - Embedded where suitable
- Specification history
  - Rev 1.0 (Gen1) completed in 2002
    - External cable spec released Feb 2007
  - Rev 2.0 (Gen2) completed in 2006
  - Rev 3.0 (Gen3) expected “late 2009”
    - 8 GTransfers/s
  - Recent relevant additions
    - Multiroot/single-root IO Virtualization
    - Cable Spec
- PCIe Gen2 now widely deployed
  - First Gen2 Intel Silicon (X38 chipset) Sep 2007
- Extensible layered specification
- Point-to-point packetized architecture
  - Relatively low overhead
  - Variable size packets
  - 128-4096 byte PDU
# PCI Express® Protocol

<table>
<thead>
<tr>
<th>Bit</th>
<th>Feature</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Rsvd</td>
</tr>
<tr>
<td>1</td>
<td>TLP Sequence Number</td>
</tr>
<tr>
<td>2</td>
<td>R</td>
</tr>
<tr>
<td>3</td>
<td>FMT</td>
</tr>
<tr>
<td>4</td>
<td>Type</td>
</tr>
<tr>
<td>5</td>
<td>R</td>
</tr>
<tr>
<td>6</td>
<td>TC</td>
</tr>
<tr>
<td>7</td>
<td>Rsvd</td>
</tr>
<tr>
<td>8</td>
<td>Tag</td>
</tr>
<tr>
<td>9</td>
<td>Last DW BE</td>
</tr>
<tr>
<td>10</td>
<td>First DW BE</td>
</tr>
<tr>
<td>11</td>
<td>Address[31:16]</td>
</tr>
<tr>
<td>12</td>
<td>Address[15:2]</td>
</tr>
<tr>
<td>13</td>
<td>R</td>
</tr>
<tr>
<td>14</td>
<td>Packet PDU</td>
</tr>
<tr>
<td>15</td>
<td>Packet PDU</td>
</tr>
<tr>
<td>16</td>
<td>Optional TLP Digest (ECRC)</td>
</tr>
<tr>
<td>17</td>
<td>Optional TLP Digest (ECRC) Cont</td>
</tr>
<tr>
<td>18</td>
<td>LCRC</td>
</tr>
<tr>
<td>19</td>
<td>LCRC Cont</td>
</tr>
<tr>
<td>20</td>
<td>Next Packet/DLLP</td>
</tr>
<tr>
<td>21</td>
<td>Total = 278 Bytes</td>
</tr>
</tbody>
</table>

### Memory Write: 4096 Byte Max Packet PDU

- **Total = 278 Bytes**
- **(256 Byte PDU)**

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Chassis scale interconnect
- Chip-to-chip, Board-to-board, backplane
- Initially a processor interconnect as Motorola/Mercury collaboration
- Physical layer defined for board + connectors
- Copper-on-board and cable media

Target market
- Embedded systems
  - Wireless infrastructure, media, networking, compute & defense
- CPU I/O, Line-card aggregation, backplane
- Extensive dataplane features
  - QoS, VCs, datagrams, encapsulation

Specification History
- Rev 1.0 completed in 1999
- Rev 1.2 completed in 2002
- Rev 1.3 completed in 2005
- Rev 2.0 completed in 2007
  - 5-6G PHY, 2, 8 and 16x lanes + Virtual Channels
- Recent relevant additions
  - Data streaming, encapsulation, traffic management

Extensible layered specification

Point-to-point packetized architecture
- Low overhead
- Variable packet size
- Maximum 256 byte PDU
- SAR support for 4 Kbyte messages
RapidIO® Packet Format: SWRITE

SWRITE Packet Type: 256 Byte Max Packet PDU

Total = 268 Bytes
(256 Byte PDU)

Address

Packet PDU

Early CRC

Packet PDU

CRC

Payload

Logical Layer

Transport Layer

Physical Layer
RapidIO® Packet Format: Message

Type 11 Packet Type: 256 Byte Max Packet PDU, 4KB w/SAR

Total = 268 Bytes
(256 Byte PDU)
RapidIO® Packet Format: Data Streaming

**Type 9 Packet Type: 256 Byte Max Packet PDU, 64KB w/SAR**

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
<th>Position</th>
</tr>
</thead>
<tbody>
<tr>
<td>AckID</td>
<td>Acknowledgment Identifier</td>
<td>0 1</td>
</tr>
<tr>
<td>CRF</td>
<td>Control and Reset Field</td>
<td>2 3</td>
</tr>
<tr>
<td>Prio</td>
<td>Priority</td>
<td>4 5</td>
</tr>
<tr>
<td>FTYPE</td>
<td>Frame Type</td>
<td>6 7</td>
</tr>
<tr>
<td>Target ID</td>
<td>Target Identifier</td>
<td>8 9</td>
</tr>
<tr>
<td>Source ID</td>
<td>Source Identifier</td>
<td>10 11</td>
</tr>
<tr>
<td>Class-of-Service</td>
<td>Class Identification</td>
<td>12 13</td>
</tr>
<tr>
<td>S</td>
<td>Stream Identifier</td>
<td>14 15</td>
</tr>
<tr>
<td>E</td>
<td>EarlyCRC</td>
<td>16 17</td>
</tr>
<tr>
<td>Rsvd</td>
<td>Reserved</td>
<td>18 19</td>
</tr>
<tr>
<td>O</td>
<td>Octet order</td>
<td>20 21</td>
</tr>
<tr>
<td>P</td>
<td>Payload</td>
<td>22 23</td>
</tr>
<tr>
<td>StreamID</td>
<td>Stream ID</td>
<td>24 25</td>
</tr>
<tr>
<td>Packet PDU</td>
<td>256 Byte PDU</td>
<td>26-31</td>
</tr>
<tr>
<td>Early CRC</td>
<td>2 Bytes Padding</td>
<td></td>
</tr>
<tr>
<td>2 Bytes Padding</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRC</td>
<td>Checksum</td>
<td></td>
</tr>
</tbody>
</table>

**Total = 268 Bytes** (256 Byte PDU)
Comparison
# Logical Layer Comparison

<table>
<thead>
<tr>
<th></th>
<th>Ethernet</th>
<th>PCI Express®</th>
<th>RapidIO®</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory-mapped R/W</td>
<td>No</td>
<td>Read/Write</td>
<td>Read/Write</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Configuration</td>
<td>Configuration</td>
</tr>
<tr>
<td>Write w/Response?</td>
<td>N/A</td>
<td>None</td>
<td>NWRITE_R</td>
</tr>
<tr>
<td>Supported address sizes</td>
<td>N/A</td>
<td>32, 64-bits</td>
<td>34, 50, 66-bits</td>
</tr>
<tr>
<td>Global Shared Memory</td>
<td>Not Defined</td>
<td>Not Defined</td>
<td>Yes</td>
</tr>
<tr>
<td>Messaging/Datagram</td>
<td>1500-9000B Payloads</td>
<td>Msg: Cntl/Int Messages MsgD: User Defined</td>
<td>Type 9: 64KB Payloads Type 10: Doorbells Type 11: 4KB Payloads</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Traffic Class, Virtual Channels</td>
<td>4-16M Type 9: StreamID, CoS Type 11: mbox/xmbox</td>
</tr>
<tr>
<td>Channelization</td>
<td>10-100s, L2 Type, VLAN Tags, UDP/TCP Ports,</td>
<td>8 Traffic Class, Virtual Channels</td>
<td></td>
</tr>
<tr>
<td>Virtualization</td>
<td>Not Defined</td>
<td>SR-IOV, MR-IOV Specifications</td>
<td>Not Defined</td>
</tr>
</tbody>
</table>
## Transport Layer Comparison

<table>
<thead>
<tr>
<th></th>
<th>Ethernet</th>
<th>PCI Express®</th>
<th>RapidIO®</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Topologies</strong></td>
<td>Any</td>
<td>Tree</td>
<td>Any</td>
</tr>
<tr>
<td><strong>Peer-to-peer?</strong></td>
<td>Yes</td>
<td>Data only</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Max number of endpoints</strong></td>
<td>$2^{48}$ (L2) $2^{32}$ (IPv4) $2^{128}$ (IPv6)</td>
<td>Large (Address-dependent)</td>
<td>$2^8$ (Small) $2^{16}$ (Large)</td>
</tr>
<tr>
<td><strong>What fields must switches modify?</strong></td>
<td>L2: None IP: TTL, MAC, FCS</td>
<td>TLP, Seq Num, LCRC</td>
<td>AckID</td>
</tr>
<tr>
<td><strong>Multicast</strong></td>
<td>Yes</td>
<td>Msg only (Data defined in new ECN)</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Delivery</strong></td>
<td>L2: Best Effort TCP/IP: Guaranteed</td>
<td>Guaranteed</td>
<td>Rev 1.x: Guaranteed Rev 2.0: +Best Effort</td>
</tr>
</tbody>
</table>
## Physical Layer Comparison: Ethernet

<table>
<thead>
<tr>
<th></th>
<th>1000Base-CX</th>
<th>XAUI</th>
<th>Backplane Ethernet</th>
<th>Future 40G (40GBase-KR4)</th>
<th>Future 100G (802.3ba)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Per port data rate</td>
<td>1G</td>
<td>10G</td>
<td>10G</td>
<td>10G</td>
<td>40G</td>
</tr>
<tr>
<td>Per lane baud rate</td>
<td>1.25G</td>
<td>3.125G</td>
<td>10.3125G</td>
<td>3.125G</td>
<td>10.3125G</td>
</tr>
<tr>
<td>Signal pairs</td>
<td>1x</td>
<td>4x</td>
<td>1x</td>
<td>4x</td>
<td>4x</td>
</tr>
<tr>
<td>Channel</td>
<td>25 m coax</td>
<td>50 cm board</td>
<td>100 cm backplane + 2 connectors</td>
<td>100 cm backplane + 2 connectors</td>
<td>100 cm backplane + 2 connectors</td>
</tr>
<tr>
<td>Encoding</td>
<td>8b10b</td>
<td>8b10b</td>
<td>64b66b</td>
<td>8b10b</td>
<td>64b66b</td>
</tr>
<tr>
<td>Signaling</td>
<td>NRZ PECL AC Coupled</td>
<td>NRZ AC Coupled</td>
<td>NRZ AC Coupled</td>
<td>NRZ AC Coupled</td>
<td>TBD</td>
</tr>
<tr>
<td>Status</td>
<td>Shipping</td>
<td>Shipping</td>
<td>Emerging</td>
<td>Emerging</td>
<td>Spec in 2009?</td>
</tr>
<tr>
<td>Notes</td>
<td>Also SGMII, 1000Base-T Proprietary</td>
<td>Intended for MAC-PHY</td>
<td>Pre-emphasis, DFE, optional FEC</td>
<td>Optional FEC</td>
<td></td>
</tr>
</tbody>
</table>
## Physical Layer Comparison: PCI Express®

<table>
<thead>
<tr>
<th></th>
<th>Gen1</th>
<th>Gen2</th>
<th>Gen3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Per lane data rate</strong></td>
<td>2G</td>
<td>4G</td>
<td>8G</td>
</tr>
<tr>
<td><strong>Per lane baud rate</strong></td>
<td>2.5G</td>
<td>5.0G</td>
<td>???</td>
</tr>
<tr>
<td><strong>Signal Pairs</strong></td>
<td>1x, 2x, 4x, 8x, 12x, 16x, 32x</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Channel</strong></td>
<td></td>
<td>~40-50 cm + 2 connectors</td>
<td></td>
</tr>
<tr>
<td><strong>Encoding</strong></td>
<td>8b10b</td>
<td>8b10b</td>
<td>???</td>
</tr>
<tr>
<td><strong>Signaling</strong></td>
<td>Custom AC Coupled</td>
<td>Custom AC Coupled</td>
<td>Custom AC Coupled</td>
</tr>
<tr>
<td><strong>Status</strong></td>
<td>Shipping</td>
<td>Emerging</td>
<td>Final spec late 2009?</td>
</tr>
<tr>
<td><strong>Notes</strong></td>
<td></td>
<td></td>
<td>Products 2010?</td>
</tr>
</tbody>
</table>
## Physical Layer Comparison: RapidIO®

<table>
<thead>
<tr>
<th></th>
<th>Rev 1.3</th>
<th>Rev 2.0</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data rate</strong></td>
<td>1.0, 2.0, 2.5</td>
<td>4.0, 5.0</td>
<td>10G</td>
</tr>
<tr>
<td><strong>Baud Rate</strong></td>
<td>1.25, 2.5, 3.125</td>
<td>5.0, 6.25</td>
<td>TBD</td>
</tr>
<tr>
<td><strong>Signal Pairs</strong></td>
<td>1x, 4x</td>
<td>1x, 2x, 4x, 8x, 16x</td>
<td>TBD</td>
</tr>
<tr>
<td><strong>Channel</strong></td>
<td>~80-100 cm + 2 connectors</td>
<td>~80-100 cm + 2 connectors</td>
<td>100 cm + 2 connectors</td>
</tr>
<tr>
<td><strong>Encoding</strong></td>
<td>8b10b</td>
<td>8b10b</td>
<td>TBD</td>
</tr>
<tr>
<td><strong>Signaling</strong></td>
<td>XAUI AC Coupled</td>
<td>OIF AC Coupled</td>
<td>TBD</td>
</tr>
<tr>
<td><strong>Status</strong></td>
<td>Shipping</td>
<td>2010</td>
<td>2011?</td>
</tr>
<tr>
<td><strong>Notes</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Protocol Efficiency

NOTE: Includes header & ACK overhead
Effective Bandwidth

- SRIO 4x 3.125G
- PCI Express x4
- 10G Ethernet: UDP
- 1G Ethernet: UDP
Quality-of-Service (QoS) Dependencies

- QoS depends on proper hooks across the interconnect fabric
  - Hierarchical Flow Control
    - Addresses short, medium and long-term congestion events
    - Link and end-to-end
  - Ability to define many streams of traffic
    - Often defined as a logical sequence of transactions between two endpoints
  - Ability to differentiate classes of traffic among streams
  - Ability to reserve and allocate bandwidth to streams and classes
QoS Comparison: Ethernet

- No universal QoS standard
- Many Layer 2+ switches support VLAN Priority Tagging (802.1d/q)
  - Eight classes
- Increasing number of routers support MPLS at L3

UDP Packet Type: 1472 byte User PDU
QoS Comparison: PCI Express®

► 8 Traffic Classes (TC)
  • No ordering between TCs
► 8 Virtual Channel (VC)
  • Separate buffer resources per VC
  • TCs are mapped onto VCs
    ▪ TC to VC mapping per port
      – No VC field in TLP
► Flexible arbitration
  • Arbitrary, RR, WRR
► Most implementations support a single TC/VC
QoS Comparison: RapidIO®

► All implementations must support 3 prioritized flows
  • No ordering between flows
  • Allows shared buffer pool across flows
► Switches required to provide some improved service
  • Extent of improvement is implementation dependant
► Dataplane Extensions adds carrier-grade QoS
  • Support for thousands of flows, hundreds of traffic classes
  • End-to-end traffic management
Flow Control Comparison

- **Ethernet**
  - Link-to-link flow control
    - PAUSE frames
    - 802.1Qbb priority-based flow control (new for DCB)
  - L2 Bridge-to-endpoint
    - Leverages VLAN tags
    - Rate limit
    - 802.1Qau congestion notification (new for DCB)
  - L3+ end-to-end flow control
    - ECN, TCP windowing, others

- **PCI Express®**
  - Link-to-link flow control

- **RapidIO®**
  - Link-to-link flow control
  - Switch/Endpoint-to-endpoint
    - XON, XOFF
  - Fine-grained end-to-end flow control
    - Data Streaming Logical Layer
Several data use models supported by high speed interconnects
- Address-based memory-mapped Read/Write
- Address-less messaging and datagrams

Memory-mapped read/write
- Very efficient but scales poorly beyond a few devices
- Software moves data using low-level memory-mapped read/writes
  - Address range of target device is located
    - Often using a previously constructed structure produced by an initialization and system discovery routine
  - Target buffer is allocated within the producer’s space
    - e.g. mmap in Linux
  - Data is moved using a bcopy or DMA operation
  - When data transfer is complete, producer notifies the consumer
    - Interrupt, memory semaphore etc
    - How SW knows last data committed at consumer can be an issue
      - Write w/Response very helpful
Several data use models are supported by high speed interconnects
• Address-based memory-mapped Read/Write
• Address-less messaging and datagrams

Messaging and datagrams
• Less efficient but scales well
• Some abstract service types
  ▪ Unreliable connectionless messages
    – Comparable to Ethernet UDP
  ▪ Reliable connectionless messages
  ▪ Reliable connection-oriented messages
  ▪ Reliable connection-oriented byte streams
    – Comparable to Ethernet TCP
• Software typically calls various underlying APIs supplied by drivers to move data
  ▪ Calls abstract underlying interconnect protocols and controllers
    – Allocate(buffer 0)
    – Open(AZ) connection to consumer Z on device A
    – Send(0)
    – Close(AZ) connection to consumer Z on device A
  ▪ Notification of arrival at device A handled locally by consumer
Many interconnect services
- APIs attempt to abstract underlying interconnect protocols
- Many such APIs have been defined

<table>
<thead>
<tr>
<th>Discovery &amp; Initialization</th>
<th>Shared Memory</th>
<th>Sockets (TCP, UDP, IP)</th>
<th>RDMA</th>
<th>TIPC</th>
<th>...</th>
<th>Proprietary</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interconnect Hardware</td>
<td>Low-level Hardware Device Driver</td>
<td>Applications</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Software APIs
Software API Comparison

► Ethernet
  • Many services and APIs are supported for many OS environments
    ▪ Sockets
    ▪ RDMA
    ▪ TIPC
    ▪ Others…

► PCI Express®
  • Memory-mapped read/write only
    ▪ Linux
      – /dev to locate device
      – mmap() to open buffer at consumer
    ▪ Proprietary services

► RapidIO®
  • Many proprietary services on Read/Write and messaging
  • Power Architecture™ processors
    ▪ rionet
      – Ethernet network stack using RapidIO messaging as packet transport
      – Work on optimizations using R/W transport
  • DSP
    ▪ FSL SmartDSP
      – RapidIO R/W with DMA API
      – Ethernet over Messaging
    ▪ TI DSP/BIOS
      – RapidIO Message Queue Transport (MQT)
High-bandwidth interconnects require low CPU overhead usage model
- Hardware support for logical, transport and link layer
- Low overhead DMA with QoS support
Ethernet Performance

- Microsecond+ fall through latencies (~100us?)
  - Not just the hardware, data has to traverse the SW stack
- High CPU overhead
  - Rule of thumb appears to be borne out in data for TCP/IP termination SW overhead
    - 1 Hz of CPU per bit of throughput (per direction)
  - Wire speed achievable with GHz class processors
    - Some CPU will be left but how much depends on
      - Protocol being terminated
      - Offload features of GigE interfaces
  - Too often advanced off-load features cannot be leveraged
    - OS & SW stack support issues
- UDP or MAC/Layer 2 solutions sometimes use proprietary higher layer protocols
  - Can defeat the value of off-the-shelf “standards-based” solution
- Error correction at endpoint stacks introduce latency jitter and determinism issues
- Works well when application requires < 30% fabric utilization
  - Lack of flow control problematic for systems that can’t significantly overprovision
PCI Express® & RapidIO® Performance

► Latency
  • Sub-microsecond switch latencies
  • PCI Express switches must manage address mapping

► End-to-end latency
  • Lower latency than Ethernet since latency does not include a SW stack

► Architecture
  • PCI Express switches allow limited peer-to-peer communication
    ▪ Multiple hosting for redundancy problematic
    ▪ Maintenance responses as well as wake-up beacons must move upstream
    ▪ Some switches support non-transparent bridging
      – Create two separate spaces for each host
      – Non-standard and implementation specific
    ▪ Must collect INTx messages and some power management transactions

► RapidIO switches straightforward and orthogonal in architecture
  • Strict peer-to-peer
  • Packet headers architected to reduce logic
  • No need to recalculate CRC
Some Economics

- RapidIO®, PCI Express® and Ethernet with modest TCP/IP offload have similar underlying silicon costs
  - PCI Express controller is slightly larger than RapidIO
  - Aggressive TCP/IP Offload engine larger than PCI Express and RapidIO endpoints

- Interesting fact about switches
  - Available established vendors for all three interconnects similar: 2-3

- Leveraging Ethernet volume economics not always a reality
  - L2+ Ethernet switches suitable for aggregation and backplanes are not high volume
    - 16-24 ports, QoS features and SERDES PHYs for backplane
    - 12-16 ports, QoS features for aggregation
  - Terminating TCP/IP imposes significant processor overhead
    - Dedicate processor or reduce performance and/or application features
Summary and Conclusion
<table>
<thead>
<tr>
<th>Attribute</th>
<th>Ethernet</th>
<th>PCI Express®</th>
<th>RapidIO®</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low latency</td>
<td>SW Stack</td>
<td></td>
<td></td>
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<tr>
<td>Low CPU overhead</td>
<td>Limited TOE</td>
<td></td>
<td></td>
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<tr>
<td>QoS: Flow Control</td>
<td>Link Only</td>
<td>Link Only</td>
<td></td>
</tr>
<tr>
<td>QoS: Channelization w/Flow Control</td>
<td>VLAN, No FC</td>
<td>1-2 VC Avail.</td>
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<tr>
<td>QoS: Jitter</td>
<td>SW Stack</td>
<td></td>
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<tr>
<td>Multicast</td>
<td></td>
<td>(w/o New ECN)</td>
<td></td>
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<tr>
<td>Virtualization Support</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High availability (hot plug, multiple hosting)</td>
<td></td>
<td>Tree/Bridge</td>
<td></td>
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<tr>
<td>Large number of endpoints</td>
<td></td>
<td></td>
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<tr>
<td>Peer-to-peer for data</td>
<td></td>
<td></td>
<td>(w/o MR-IOV)</td>
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<tr>
<td>Peer-to-peer for management</td>
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<tr>
<td>High port bandwidth (&gt;10G)</td>
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<tr>
<td>Commodity off-the-shelf endpoints (graphics, NICs, HBAs, etc)</td>
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</table>

**Summary by Attribute**

- **Good Fit**: Suitable for the application or requirement.
- **Marginal**: May be suitable under certain conditions or with modifications.
- **Poor Fit**: Not suitable for the application or requirement.
Summary Conclusion

► Ethernet ubiquitous as LAN-scale interconnect
  • GigE ubiquitous, 10G Ethernet will segment market for first time
  • Broad endpoint silicon and software support
  • Useful in low bandwidth embedded applications

► PCI Express® widely deployed in PC/Server space
  • Significant role in the embedded space
    ▪ Where there is an intersection with the PC & Server space
    ▪ Where PCI has been used
  • Backplane interconnect role in the embedded space will be limited
    ▪ Unwieldy when connecting large numbers of endpoints
    ▪ Similar switch ecosystem to RapidIO® and Ethernet
  • Broad switch, IP and endpoint ecosystem

► RapidIO deployed with growing ecosystem
  • Expanding from initial Military/Aero, DSP and line card aggregation role
  • Best positioned for multicore applications
  • Will gradually expand role onto the backplane
    ▪ Efficient protocol supporting both control and data plane
    ▪ Variety of PHY speeds
  • Cost competitive against 1G and 10G Ethernet
  • Established and diverse ecosystem