Enabling the Migration to an All-IP Network

Colin Cureton
Product Marketer
Enable next generation broadband networking systems to deliver a seamless user experience via processors offering:

- High-performance cores for control and data plane
- Leading-edge performance for power
- Intelligent IP and security processing
- Flexible, programmability
- Ability to leverage historical and future software investment
- Low risk “value-add” ecosystem
Evolution within Specific Applications

Network Evolution

3G Network

- MSC Server / MGW
- RNC
- Node B
- WCDMA (HSDPA)
- ATM

LTE Evolved 3G Network

- aGW
- eNB
- X2
- S1
- IP Routing

- Evolved RAN
  - Low latency
  - Low cost, simple Architecture

- Consolidated GSN/RNC Functions

- LTE Radio
  - Low Latency RLC/PHY
  - 50M – 100Mbps
  - OFDM, MIMO

Technology Challenges

- Significantly higher data rates – to 100/50 Mbps (down/up)
- Flexible spectrum (FDD/TDD), co-existing with 3G
- Improved spectral efficiency (using OFDM and MIMO)
- Improved control plane and user plane latency
- “All IP” network friendly
- Reduced cost for operator and user

Base Station Platform Benefits

- Higher processing performance
- Scalable, programmable performance
- OFDM /MIMO DSP signal processing
- Low latency interconnect and optimized scheduling
- Integrated IP interconnect
- Consolidation, reuse, power savings
**Transitional Challenges**

► **Application Challenges:**

- Acceleration of network connected devices
  - Mix of services: voice and data
  - Mix of protocols: IP, Ethernet, MPLS, TDM, ATM, IMA, A-bis/A-ter, PseudoWire…
  - Mix of physical layer: E1/T1, PDH, SDH/SONET, OFDM-base microwave, g.SHDSL, ADSL2+, PON, Point2Point Ethernet. …

- Growing broadband wireline/wireless data-rates (including Gigabit IP forwarding)

- Lower power to reduce OPEX and carbon footprint
Migrating to all IP - Options for OEMs

- Distinct legacy or IP only support

- Systems are designed with either:
  - Network interface cards (NICs) only capable of supporting legacy or IP interfaces
  - OR
  - Distinct components on the system to support legacy and IP

- Requires design, support maintenance of distinct solutions for IP and legacy data path solutions.

- Multi-protocol design

- Systems are designed to support legacy and future all IP requirements

- Single hardware and software designs, consistent programming model for data path (DP) and core

- Balance of DP and core performance to allow system to be optimized for different protocols and applications
Power Architecture® Technology Platform Roadmap
Increasing Performance, Reducing Power

Increasing Performance (Frequency, System Performance)

- PowerQUICC® I
- PowerQUICC II
- PowerQUICC II Pro
- PowerQUICC III
- MPC86XX

Decreasing Power

- QorIQ™ P1 platform
  45 nm process technology
- QorIQ™ P2 platform
  45 nm process technology
- QorIQ™ P3 platform
  45 nm process technology
- QorIQ P4 platform
  45 nm process technology
- QorIQ™ P5 platform
  45 nm process technology

Next Generation Core and Platform –
> Increased frequency
> Higher bandwidth
> Improved system performance within five power bands

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QorIQ™ P4 Series P4080 Block Diagram

- Eight e500 cores to 1.5 GHz
- 128 KB backside L2 cache
- 2 MB front side L3 cache
- 2x 10GE + 8x GE
- Enhanced local bus controller
- 18 lanes 5 GHz SerDes
  - Three PCI Express® 2.0 controllers
  - Two Serial RapidIO® 1.2 controllers
- Two USB controllers with ULPI interface to external PHY
- Aurora debug port
- CoreNet coherency fabric
  - Eliminates shared bus contention and supports dramatically higher address issue bandwidth to “feed” multiple cores
  - Scales to support more than 32 cores
  - Can support heterogeneous cores
- Tri-level cache hierarchy
  - Power Architecture™ cores with backside L2 caches
  - Multiple L3 shared caches
  - Multiple memory controllers
- On-demand application acceleration
  - Frame Manager, Buffer Manager, Queue Manager
  - Crypto and pattern match acceleration
- Virtualization
  - Autonomous core operation
  - Memory protected from bad code
**Dual-core P2020 Block Diagram**

- **Dual e500 core built on Power Architecture™ technology**
  - 800 - 1200 MHz
  - 512 KB frontside L2 cache w/ ECC, hardware cache coherent
  - 36-bit physical addressing, DP-FPU

- **System unit**
  - 64-/32-bit DDR2/DDR3 with ECC
  - Integrated SEC 3.1 security engine
  - Open-PIC interrupt controller, Perf Mon, 2x I²C, timers, 16 GPIO’s, DUART
  - 16-bit enhanced local bus supports booting from NAND flash
  - One USB 2.0 host controller with ULPI interface
  - SPI controller supporting booting from SPI serial flash
  - SD/MMC card controller supporting booting from flash cards
  - Three 10/100/1000 Enhanced Triple Speed Ethernet Controllers (eTSEC) w/ jumbo frame support, SGMII interface
    - Enhanced features: parser/filer, QOS, IP-checksum offload, lossless flow control
    - IEEE® 1588v2 support
  - Two Serial RapidIO® controllers with integrated message unit operating up to 3.125 GHz
  - Three PCI Express® 1.0a controllers operating at 2.5 GHz

- **Process and package**
  - 45 nm SOI, 0C to 125C Tj with -40C to 125C Tj option
  - 689-pin TePBGAII
MPC8569 PowerQUICC® III
Bridging the Gap to the All-IP Network

- e500 Core built on Power Architecture® technology
  - 800 MHz to 1.33 GHz
  - 512 KB L2 cache w/ ECC
  - 36-bit physical addressing
  - Double Precision Floating Point
- System interfaces
  - 64-bit or 2x32-bit DDR2/3 w/ ECC
  - 800 Mbps/pin data rate
  - 16-bit Local Bus for SRAM/flash
  - Timers, DUART, 2x I²C, GPIO, SPI
  - USB 2.0 full speed
- High-speed serial interfaces
  - Dual SGMII
  - Dual x1 Serial RapidIO® or PCI Express®
- QUICC Engine™
  - 4 RISCs up to 667 MHz
  - Maximum of eight Ethernet interfaces, one per UCC:
    - 4 x Gigabit Ethernet (up to 2 w/SGMII)
    - Up to 8 x 10/100 Ethernet
  - Multi-PHY UTOPIA/POS-PHY L2 (16-bit)
  - IEEE® 1588 support v2
  - 16 x T1/E1 (512 x 64kbps channels)
- Security engine (SEC3.0)
  - ARC4, 3DES, AES, RSA/ECC, RNG, XOR, Single pass SSL/TLS, Kasumi, SNOW
- Four-channel DMA
- 45 nm SOI process technology
- Target <7W power (@ 800 MHz e500)
QUICC Engine™ – Protocol Termination vs. Interworking

► Protocol Termination:
  • Both control and data plane traffic are terminated by the CPU
  • Predominant approach used with CPM based PowerQUICC devices
  • Protocol processing and interworking is performed by CPU software

► Protocol Interworking:
  • Data plane traffic is forwarded directly by QUICC Engine™ technology. Control plane traffic is terminated by the CPU.
  • Benefits: Greater headroom in CPU, improved throughput, minimized latency and jitter
  • Powerful API and drivers provided to facilitate effective use of interworking

• Interworking applications are typically complex from a Freescale solution perspective, and often customer specific, as they rely upon implementing functions previously done using CPU software in microcode

• Termination applications rely upon customer implemented software, and therefore are less complex from a Freescale solution perspective
Device drivers:
• Modular set of platform, peripheral and protocol device drivers
• Operating system independent APIs (e.g. bare board) for customer application use and porting
  ▪ Operating system porting guide provided
• Platform level drivers supported – MMU, cache, interrupt controller, memory controllers, timers, DUART, I2C, security, etc.
• Built-in use cases demonstrating functionality and performance
• Complete device driver source code and comprehensive documentation provided

Comprehensive feature set, including:
• Interrupt or polling modes for communication peripherals
• Statistics gathering
• Protocol interworking
• Support for both default (simple) and advanced (detailed) driver configurations
• External memory management for parameters, tables and buffer descriptors (BDs)
• Memory management support for system bus, secondary bus and local bus

Hardware support:
• Support for MDS processor and I/O boards
QUICC Engine™ Linux® Drivers
(offer consistent user space and bare board API)

QUICC Engine Linux driver package contains:
- Low-level drivers (bare board)
- User space libraries
- The user space API is a mirror of the bare board API

Supported features include:
- Ethernet termination
- ATM termination
- IMA termination
- PPP termination
- ATM2ETH interworking
- ETH2ETH interworking
- PPP2ETH interworking
- ATMoIMA2ETH interworking
- Packet filtering
Software Migration – Preserving API Architecture

API

<table>
<thead>
<tr>
<th>Legacy Features</th>
<th>API</th>
<th>Legacy IP Specific</th>
<th>IP Only (Today)</th>
<th>Common Features</th>
<th>IP Specific</th>
<th>Future DPAA</th>
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Features

IP Features
Software Migration

Application Code

Libraries

Operating System

BB Application Code

API

Driver

Driver

Driver

Hardware

Legacy Architecture

IP Only Architecture

Future DPAA

Software

Hardware
### Freescale: Enabling the Migration to an All-IP Network

<table>
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<tr>
<th>High Performance cores for control and data plane</th>
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<td>Clear migration path between devices</td>
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<td>Low Risk “value-add” eco-system</td>
<td>One of the most established eco-systems in the industry</td>
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</table>
Thank you for attending this presentation

We’ll now take a few moments for the audience’s questions and then we’ll begin the question and answer session