MSC8156 DSP Processor and the Baseband Market

Barry Stern
Baseband DSP Product Line, Marketing Manager
Agenda

- Baseband Market Evolution and Freescale Focus
- MSC8156 DSP Highlights
  - Device Block Diagram
  - New DSP Core and Platform
  - MAPLE-B – Baseband Accelerators
- MSC8156 Enablement
  - Hardware & Software
- Summary
Freescale High-End DSPs

... Deliver scalable, programmable solutions that extend the user migration to new services

Multicore DSPs for Multistandard Wireless Base Stations

- 3G-LTE & 3G Macro
- TDD-LTE Macro
- WiMAX Macro
- WiMAX Pico
- TD-SCDMA base station

Multicore DSPs for Voice and Video Gateways

- Trunking Gateway
- High-End IPBX
- Video Conferencing MCU
- VoIP Carrier-Class Media Gateway
- Wireless TRAU Gateways

Common denominator: Drive for optimal programmable DSP performance density (Cost, Power)
Broadband Wireless Timelines

**Freescale Focus**
- 3G-LTE
- HSPA+
- Advanced-LTE
- WiMAX/802.16m

**Notes:** Throughput rates are peak theoretical network rates. Radio channel bandwidths indicated. Dates refer to expected initial commercial network deployment except 2008 which shows available technologies that year. No operator commitments for UMB.
3G Evolution – from Thin to Thick Data Pipe

3G-LTE Significantly Outperforms 3G Standards

- Increasing integration for high data rates and low latencies
- Algorithm differentiation and flexibility require high-performance multicore DSP for programmability combined with integrated baseband accelerators for cost and power efficiency

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<tr>
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<tbody>
<tr>
<td>WCDMA</td>
<td>HSDPA</td>
<td>HSUPA</td>
<td>3G-LTE</td>
<td></td>
</tr>
<tr>
<td>0.5 Mbps at 5 MHz</td>
<td>Up to 14 Mbps DL at 5 MHz</td>
<td>Up to 5 Mbps UL at 5 MHz</td>
<td>300+ Mbps DL at 20 MHz</td>
<td></td>
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<tr>
<td>HSPA+</td>
<td></td>
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<tr>
<td>Up to 42 Mbps DL at 5 MHz</td>
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<tr>
<td>HSUPA</td>
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</tr>
<tr>
<td>Up to 5 Mbps UL at 5 MHz</td>
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</table>
Wireless Peak Data Rates over Time

- HSPA DL and UL peak throughputs expected to double every year on average
- Limitations not induced by the technology itself but time frames required to upgrade infrastructure and transport networks, obtain devices with corresponding capabilities and interoperability tests

Rysavy research
Freescale Building Blocks for Wireless Base Stations

3G Network

3G RAN
Evolving to All-IP

ATM
RNC
Node B
WCDMA (HSPA)

IP
RNC
Node B

14.4 Mbps

3G-LTE Evolved Network

aGW
Consolidated GSN/RNC Functions

S1
IP

X2
IP

eNB
LTE Radio
Low Latency PHY
up to 300 Mbps
OFDM, MIMO

Rich Multimedia & VoIP capable

Evolved RAN
IP Routing
High bandwidth,
Low latency
Low-cost,
Simpler Architecture

Key Technology Challenges

High Speed Data Rate
100Mbps (DL), 50Mbps (UL)

Low Latency
in RAN < 5ms

Scalable Capacity
Spectrum Efficiency Scalable bandwidth

Ease of Upgrade
reasonable OPEX/CAPEX

Power/Cost Optimal Architecture

Freescale Solutions

All IP Network
Security

New RAN Architecture
IP Routing

LTE Radio
SC-FDMA (UL), OFDMA (DL)
FEC, MIMO

Flexible Spectrum
RF Linearity

PHY Processing

MAC Processing

Timing Synchronization
IEEE1588

High Speed Interfaces

High Power RF

Multicore DSP
High Performance Platform

Baseband Accelerators

Multicore QorIQ
Scalable CPU Platforms

sRIO, PCI-Ex, GigE
SerDES, LVDS

Packet process, Security
Eth. Protocols, Encryption

LDMOS Technology
High Eff, Low cost package

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Layer 1 PHY, Layer 2 MAC
- No FPGA/ASIC required
- Scalable platform
MSC8156 Multicore DSP – Highlights
Wireless Infrastructure Baseband Processor
 MSC8156 Highlights

► Target Wireless Base Station Systems
  • 3G-LTE, TDD-LTE, WiMAX, HSPA+ and TD-SCDMA
  • Meets all leading future wireless technologies

► Multi-Standard Technology
  • Single Sector 3G-LTE
  • Multi-sector WiMAX
  • Multi-carrier TD-SCDMA
  • Multi-sector HSPA along with external chip rate acceleration

► Pioneering Expertise
  • Leveraging multicore architecture expertise by introducing its 4th generation multicore DSP
  • First to implement Turbo/Viterbi accelerators in DSP—compliant to latest OFDMA standards

► Highly Efficient Internal Memory
  • Large on die low latency memory:
    ▪ 6x512KB of L2/M2 + 1MB M3 = 4Mbyte

► MAPLE-B Accelerator
  • High throughput, multi-standard compliant, re-programmable

MSC8156 Device Performance
• Optimized Programmable Performance
  • Based on next generation SC3850 DSP core, delivers up to 48 GMACS
    ▪ 6 GHz effective performance
  • Added Intelligent application specific accelerators
  • High-speed standard interfaces
    ▪ 2xSRIO, 2xSGMII, 2xDDR-3, PCI-Express
  • Highly optimized multilevel memory
  • High speed DDR interface
MSC8156 DSP
Now Sampling

• Target applications
  • PHY layer processing for FDD-LTE, TDD-LTE, HSPA+, TD-SCDMA, WiMAX channel cards in NodeB BTS

• Key advantages
  • Industry’s highest performance Programmable DSP, outperforms competition
  • Featuring six fully-programmable 1GHz DSP cores delivering 6GHz of DSP processing power plus innovative, multistandard application specific accelerators
  • Supports at least 3G-LTE 10Mhz sector, UL+DL including MiMO in a single device

• Status
  • Samples and ADS shipments to multiple industry leading OEMs started 8/1/09
  • Functionality validation: Fully Covered
StarCore® DSP Core Architecture Roadmap

- Enhanced Control code Support
  - 8 MAC/cycle

- MMU Support
- Additional ASI
- Enhanced Video
- Dynamic Branch Prediction
- Additional SIMD Instructions

- Memory Protection
- Prediction

V2
- Up to 6-Issue VLIW Architecture
- VLES
- SIMD

V3
MSC711x, MSC8101/3, MSC8122/26/12/13, Wireless subscriber

V5
MSC8144/ E
1 GHz and beyond (90nm)
SC3400 products...

V6
MSC8156
SC3850 products...

V7
MSC8144/ E
VLES
SIMD

products...

1 GHz and beyond (90nm)
SC140e products...

V2, V3, V5, V6, V7

MSC8122/26/12/13, Wireless subscriber

SC1000 products...

V5
MSC8144/ E
1 GHz and beyond (90nm)
SC3400 products...

V6
MSC8156
SC3850 products...

V7
products...

V5
MSC8144/ E
1 GHz and beyond (90nm)
SC3400 products...

V6
MSC8156
SC3850 products...

V7
products...
StarCore® DSP Core Architecture

StarCore core consists of the following main units:

- Data arithmetic logic unit (DALU) that contains four instances of an arithmetic logic unit (ALU) and a data register file
- Address generation unit (AGU) that contains two address arithmetic units (AAU) and an address register file
- Program Control Unit (PCU)
SC3850 DSP Sub-System Features – Caches

► Caches optimized to give best performance reducing TTM
► L1 caches
  • Instructions and Data caches both: 32 KB, 8 way
    ▪ Data cache supports Write Back allocate and Write Through policies
  • Advanced automatic pre-fetching:
    ▪ Line pre-fetch with critical word first and next line pre-fetch
  • SW-controlled pre-fetching with cache control instructions

► L2/M2 memory system
  • 512 KB, configurable as L2 cache or M2 SRAM in 64 KB banks
  • M2 SRAM accessible by DMA
  • L2 cache: 8-ways, unified program and data
  • Programmable cache way partitioning according to address ranges
  • Low latency to the core (10-12 cycles)
  • SW-triggered DMA like Pre-fetch channels operate in the background
  • DMA based “Stashing” to DDRz
MAPLE Baseband Acceleration - Positioning

Flexibility:
- Technologies/standards modifications
- Algorithmic modifications
- Architecture options
- Solution scalability

Cost:
- Power dissipation
- Silicon area

Programmable System Interface (PSIF)
- 1 to 4 RISC controllers
- 1-12 Processing Elements
- 1-4 System DMA’s & internal DMA’s

- Legoland integrations
- From Macro to Femto
- Mix and match different PE’s for various solution scalability and derivatives
MAPLE-B Block Diagram

PSIF : Programmable System Interface
TVPE : Turbo/Viterbi Processing Engine
FFTPE : FFT Processing Engine
DFTPE : DFT Processing Engine
CRCPE : CRC processing Engine

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## MAPLE-B Performance and Standards Compliance

### WiMAX Systems

<table>
<thead>
<tr>
<th>Feature</th>
<th>MAPLE-B (MSC8156)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>Optional support for sub-block de-interleaving</td>
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<tr>
<td>Viterbi Decoding</td>
<td>Optional support for periodic de-puncturing</td>
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<tr>
<td>FFT/IFFT</td>
<td>Optional support for guard bands insertion</td>
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<td>CRC, Insertion for DL and check for UL</td>
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### 3G LTE FDD/TDD Systems

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<td>Optional support for guard bands insertion</td>
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<td></td>
</tr>
<tr>
<td>CRC, Insertion for downlink and check for uplink</td>
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### UMTS – WCDMA, HSPA+

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3GPP TS 36.212 FEC & CRC

IEEE® 802.16 Rev2

3GPP TS 25.212 (FDD) FEC & CRC
3GPP TS 25.222 (TDD) FEC & CRC
MSC8156 Other Building Blocks

- Security engine acceleration – enabling data protection for MAC/L2 processing

- Dual Serial RapidIO® – x4 @3.125G, high throughput interfaces connecting to antenna, L2/MAC processor and other DSPs on channel card

- Dual gigabit Ethernet – control path

- PCI Express® – x4 @ 2.5G, high throughput interface connecting to L2/MAC processor or FPGA

- DDR 2/3 – high throughput memory interfaces

- TDM – 4 interfaces, each 256 channels
Freescale’s 1st Wave 45nm Products

- **PowerQUICC® MPC8569**
  - Flip Chip PBGA
  - CHRT and IBM
  - Sampling
  - Functionality, performance execution on track

- **Multicore DSP MSC8156**
  - Flip Chip PBGA
  - CHRT and IBM
  - General Sampling
  - Functionality, performance execution on track

- **QorIQ™ P2020**
  - Wire Bond TEPBGA-II
  - CHRT and IBM
  - Sampling
  - Functionality, performance execution on track
MSC8156 DSP Enablement
CodeWarrior™ Development Studio for StarCore® v10.0
A complete development environment under Eclipse

► Eclipse IDE
  • Configuration wizards
  • Plug-In architecture
  • 3rd party community

► StarCore Build Tools
  • C/C++ optimizer compilers

► Software Simulators
  • Multicore functional accurate simulator
  • Core platform cycle accurate simulator
  • MAPLE integrated into multicore simulator

► SmartDSP - Operating Systems
  • Pre-emptive, high performance, field deployed, networking stacks
  • Royalty-free

► Starcore Debugger
  • Multicore and multi-DSP
  • MSC8144 and MSC8156 targets

► Trace & Profile
  • Trace data offload via Ethernet using SmartDSP HEAT technology
MSC8156 ADS (Evaluation Board)

- DSP – MSC8156 Multicore DSP
- Memories – DDR2/3, 1 GByte each
- Ethernet Switches – SGMII & RGMII
- SGMII/RGMII PHY
- TDM – 2x E1/T1 Framers & PTMC
- AdvancedMC™ (AMC) connector
  - Dual 1000BaseX
  - Dual Serial RapidIO® x4/PCI Express® x4
  - TDM
- Board form factor – Dual-width AMC
- Availability – Now
### MSC8156 - 3G-LTE Reference Software/Hardware

<table>
<thead>
<tr>
<th>Item</th>
<th>Standard</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>L1</strong></td>
<td>3GPP TS</td>
<td><strong>Enablement Software for MSC8156:</strong></td>
</tr>
<tr>
<td><strong>Software</strong></td>
<td>36.211/</td>
<td>- ANSI-C Source for Channel estimation SISO/MIMO</td>
</tr>
<tr>
<td></td>
<td>36.212/</td>
<td>- UL MU-MIMO</td>
</tr>
<tr>
<td></td>
<td>36.213/</td>
<td>- DL MIMO</td>
</tr>
<tr>
<td></td>
<td>36.214</td>
<td>- MMSE modulation demapping</td>
</tr>
<tr>
<td></td>
<td>3GPP TS</td>
<td>- UL / DL HARQ</td>
</tr>
<tr>
<td></td>
<td>36.300</td>
<td>- Turbo Encoder</td>
</tr>
<tr>
<td><strong>L2/L1</strong></td>
<td></td>
<td>- Well defined L2/L1 Interface</td>
</tr>
<tr>
<td><strong>Interworking</strong></td>
<td>3GPP TS</td>
<td>- Reuse possible across devices</td>
</tr>
<tr>
<td></td>
<td>36.201</td>
<td><strong>Board</strong></td>
</tr>
<tr>
<td><strong>AMC</strong></td>
<td></td>
<td><strong>Multi-Standard Baseband AdvancedMC (AMC) Platform</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Sample quantities as Development Reference</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Cards available to decrease time-to-market</td>
</tr>
<tr>
<td><strong>Platform</strong></td>
<td>3GPP TS</td>
<td><strong>Quick Start integrated reference platform</strong></td>
</tr>
<tr>
<td></td>
<td>36.201</td>
<td>- Running L1/L2 multicore system software</td>
</tr>
</tbody>
</table>
MSC8156AMC – Reference Development System

- **High Density DSP Platform**
  - 3x MSC8156 Multicore DSP – each with:
    - 6x SC3850 StarCore® DSP cores at 1GHz + MAPLE-B baseband accelerator
    - 2x 512MByte of 64-bit DDR3 memory

- **Connectivity**
  - Four 3.125Gbaud SRIO (x4) interfaces from backplane to DSP farm via SRIO switch
  - Two 1000 Base-X Gigabit Ethernet interfaces from backplane to DSP farm via Ethernet switch

- **Module Management Controller (MMC)**
  - Hot swapping
  - Board Control

- **Target Applications**
  - 3G-LTE, WCDMA, WiMAX base stations and Media Gateway systems
  - Design reference and enablement platform for customers and third parties

- **Form Factor**
  - Single Width AdvancedMC

- **Availability**
  - Alpha: July ‘09
  - General: Q3’09
MSC8156 Solution - Delivering Low BOM Costs Channel Cards

LTE- FDD:
• Single Sector 20 MHz, 2x4 MIMO UL, 4x4 MIMO DL
• Up to 300 Mbps DL, Up to 150 Mbps UL

WiMAX-TDD:
• 3 Sectors 10 MHz 2x4 MIMO UL, 4x4 MIMO DL
• Up to 100 Mbps/Sector DL
• Up to 14 Mbps/Sector UL
Summary
MSC8156 - Solution for Multistandard base stations

Multistandard Baseband Solution

- 3G-LTE Solution
  20 MHz 3G-LTE, 1 sector, MiMO
  144Mbps downlink & 76Mbps uplink

- HSPA+ Solution
  Multi-sector HSPA+ with external chip rate acceleration

- WiMAX Solution
  10 MHz, 3 sectors, 2Tx by 4Rx antenna single device handles 150Mbps downlink & 42 uplink

- 3G-LTE
  TDD-LTE
  WiMAX
  HSPA+
  TD-SCDMA

- TD-SCDMA Solution
  6 Carrier base station handling symbol rate and chip rate

- Processing power equivalent to 6GHz DSP plus FPGA/ASIC
- Based on new SC3850 programmable DSP core
- Embedded with high throughput multistandard baseband accelerators
- Industry’s first 45nm, six core DSP ideal for infrastructure
- Ready for deployment of cost-optimized base stations of 3G-LTE
Wireless Infrastructure DSP Roadmap

Binary Code Compatible

- Tri & Dual core
- 400/300-MHz SC140 Starcore cores
- 8 (16-bit) GMACs
- 1.4 Mbyte RAM
- 90nm
- 2008 introduction

MSC8122/3

- Quad core
- 500-MHz SC140
- 8 (16-bit) GMACs
- Integrated Turbo & Viterbi COPs
- 1.4 Mbyte RAM
- Ethernet, Serial
- 90nm

MSC8126

- Quad core
- 1-GHz SC3400 cores
- 16 (16-bit) GMACs
- 10.5 Mbyte RAM
- Dual 1G Ethernet (SGMII)
- ATM/Utopia
- Integrated Security Accelerator
- Serial RapidIO® port x4 (3.125 Gbaud)
- 90nm

MSC8156

- Six core DSP
- Supporting 3G-LTE, TDD-LTE, WiMAX, TD-SCDMA, 3GPP, 3GPP2
- Six core 1-GHz SC3850 StarCore DSP
- 48 (16-bit) GMACs
- MAPLE Accelerator
- 4 Mbyte RAM
- Dual 1G Ethernet (SGMII)
- Integrated Security Accelerator
- Dual DDR3 800MHz-64b
- Dual Serial RapidIO® port x4
- PCI Express® x4
- 45nm

MSBA8100

- Accelerator device for 3G-LTE, TDD-LTE, WiMAX, TD-SCDMA, 3GPP, 3GPP2
- Turbo, Viterbi, FFT, DFT
- 512 KB internal RAM
- DDR2
- PCI
- Dual Serial RapidIO® ports x4 (3.125 Gbaud)
- Companion for MSC8144
- 90nm

MSC81xx

- Next Generation SC3850 based DSPs
- 45nm

MSC81xx

In Development

- Tri & Dual core
- 400/300-MHz SC140 Starcore cores
- 8 (16-bit) GMACs
- 1.4 Mbyte RAM
- 90nm

MSC81xx

Future

- Quad core
- 500-MHz SC140
- 8 (16-bit) GMACs
- Integrated Turbo & Viterbi COPs
- 1.4 Mbyte RAM
- Ethernet, Serial
- 90nm

MSC81xx

Production

- Quad core
- 1-GHz SC3400 cores
- 16 (16-bit) GMACs
- 10.5 Mbyte RAM
- Dual 1G Ethernet (SGMII)
- ATM/Utopia
- Integrated Security Accelerator
- Serial RapidIO® port x4 (3.125 Gbaud)
- 90nm

MSC81xx

Sampling

- Quad core
- 500-MHz SC140
- 8 (16-bit) GMACs
- Integrated Turbo & Viterbi COPs
- 1.4 Mbyte RAM
- Ethernet, Serial
- 90nm

MSC81xx

2004 – 2005

2006 – 2007

2008

2009

2010

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Freescale’s Value Add Base Station Solutions

► MSC8156 enables OEMs opportunity to take full advantage of LTE capabilities
  • Supports legacy 3G technologies as well as the newest wireless standards to enable using same DSP for multiple technologies or in a multistandard base stations
  • 6 GHz raw performance with fully programmable cores
  • Embeds the unique MAPLE-B technology that accelerates Turbo and Viterbi, MiMO, CRC, Fast Fourier Transform (FFT), Inverse Fast Fourier Transform (IFFT), Discrete Fourier Transform (DFT), Inverse Discrete Fourier Transform (IDFT) operations currently performed in FPGA/ASIC custom devices

► Manufactured at most advanced process technology
  • Helps to significantly increase performance and design energy efficient solution while integrating functionality compared to previous generations process technologies
  • Help OEMs deliver cost effective solution, to design small form factor channel cards that take up less space, increased functionality and consumes less power giving the opportunity to provide differentiated and competitive solutions for their customers

► High speed and standard interfaces pertinent to different board topologies
  • Meet required throughputs
  • Equipped with off-the-shelf ecosystem

► Cost-optimized solutions
  • Reduces channel card bill of material by reducing chip count and eliminates the need attach costly, customized and power hungry dedicated devices
  • The combination of 6 cores DSP plus baseband accelerator into a single SoC can be used for final and cost optimized system production

► Future Roadmap
  • Addressing the need for highly optimized solutions
  • Forward looking for further cost optimized 3G/4G-LTE Solutions
Freescale Introduces Product Longevity Program

► The embedded market needs long-term product support, which allows OEMs to provide assurance to their customers.
► Freescale has a longstanding track record of providing long-term production support for our products.
► Freescale is pleased to introduce a formal product longevity program for the market segments we serve.
  • For the automotive and medical segments, Freescale will manufacture select devices for a minimum period of 15 years.
  • For all other market segments in which Freescale participates, Freescale will manufacture select devices for a minimum period of 10 years.
► A list of applicable Freescale products is available at www.freescale.com.
Thank you for attending this presentation. We’ll now take a few moments for the audience’s questions and then we’ll begin the question and answer session.