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SD/MMC Deep Dive

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Objectives

- Familiarize the audience with the MMC/SD standards
- Describe some of the differences between MMC and SD
  - Spec Differences
  - Physical Differences
- Basic understanding of Freescale's enhanced secure digital host controller (eSDHC)
  - Hardware Considerations
  - Software Program Model
- Describe the steps to booting from SD/MMC on QorIQ or PowerQUICC devices

Agenda

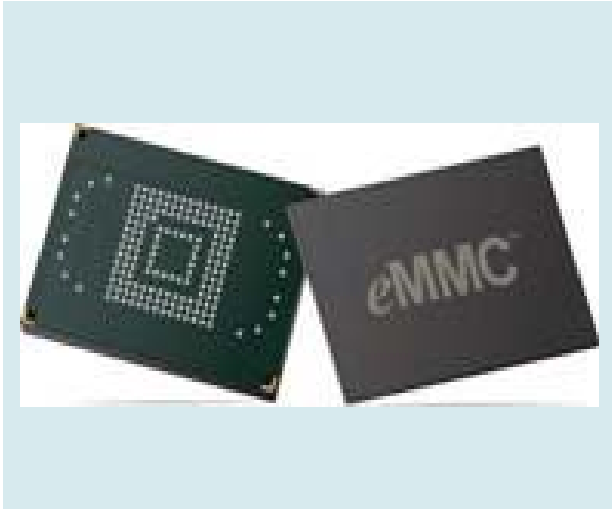
- SD/MMC Standards Overview
  - SD (Security Digital) Card
  - MMC (MultiMedia Card)
- eSDHC (Enhanced Secure Digital Host Controller)
  - Hardware Considerations
  - Software Drivers
- Boot From a SD/MMC Card
  - Configurations
  - Utility Application
  - U-boot
  - Demo

Standards & Status

- Current Standards
  - MMC 4.4 (JESD84-A44)
  - SD Card 3.0, eSD Addendum 2.10
  - SD Host Controller 3.0
- QorIQ/PowerQUICC
  - Support MMC 4.2 (JESD84-B42) / SD 2.0 / SD Host Controller 2.0
    - P4080
    - P4040
    - P5020
    - P3041
    - P2020
    - P1020
    - P1022
    - P8569
    - P8536
    - P837x (Used a storage only, cannot boot from)

SD / MMC cards

- MMC Cards
  - MMC / MMCplus (3.3 V)
  - RS- MMC
  - MMCmobile (Dual Volt)
  - MMCmicro
  - eMMC
- SD Cards
  - SDHC
  - SD
  - MiniSD
  - MicroSD



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MMC Cards

- MMC 4.2 (MMCA 4.2) (JEDEC, JESD84-B42)
  - Based on an advanced 13-pin bus
  - *SPI mode*
  - High Voltage (2.7 – 3.6 V)
  - Dual Voltage (2.7 – 3.6, 1.7 – 1.95 V) (Rev 3.2, 01/2002)
  - Bus width: 1-bit, 4-bit, 8-bit (Rev 4.0, 12/03)
  - Max Speed
    - Clock: 26 / 52 Mhz. 20 Mhz Backward-Compatible
    - Data: 416 Mbits/sec (8*52)
  - Max Capacity
    - Byte Address Mode: 2GB
    - Block Address Mode: > 2GB
  - Security: write protection
  - 2 form factors: (24mm x 32 (18) mm x 1.4mm)
  - MMCPlus / MMCmobile(Dual Volt)
    - > 2.4MB/s

- SD 2.0 (May, 2006)
  - Based MMC spec (9-pin Interface)
  - *SPI mode*
  - High Voltage (2.7 – 3.6 V), Dual (undefined in this spec)
  - SD Memory vs SDIO
  - Bus width: 1-bit, 4-bit
  - Max Speed (Speed class: 0, 2, 4, 6)
    - Clock: 25 / 50 Mhz.
    - Data: 200 Mbits/sec (4*50)
  - Max Capacity
    - Standard (Byte Address Mode): 2GB
    - SDHC (Block Address Mode): 2 - 32GB
  - Security: write protection
  - 3 form factors: (Standard SD, miniSD, microSD)

Current Standards – MMC

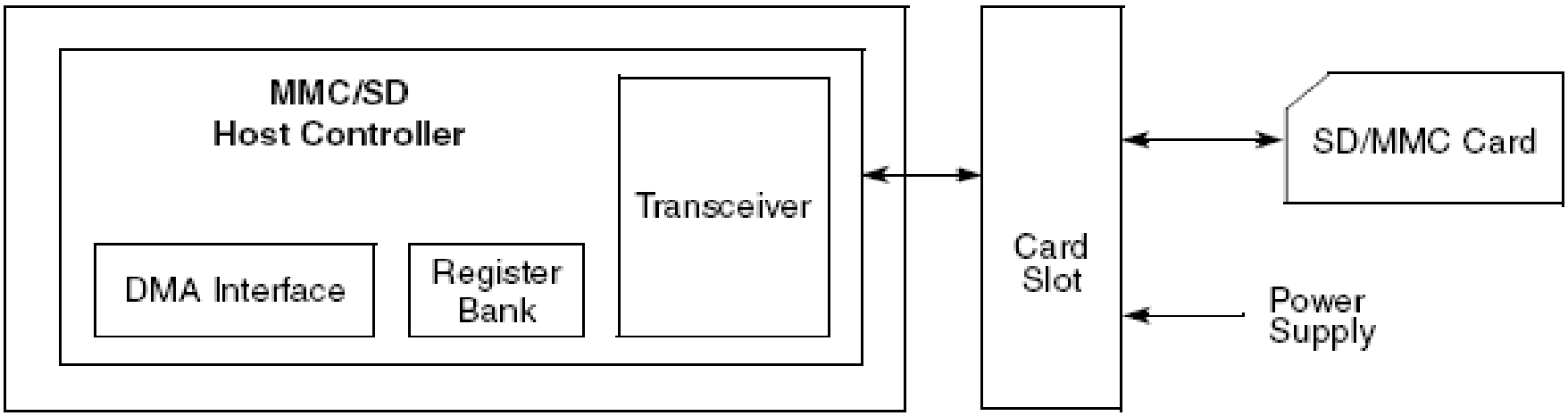
- JESD84-A44 (MMCA 4.4) (March, 2009)
  - eMMC cards (silicon)
  - Max Capacity: 2 TB
  - Updated Extended CSD register
    - Min Wrt/Rd performance for 8 bit at 52 MHz in DDR mode
  - Security: Replay Protected Block/Secure Erase/Trim
    - Message Authentication Code (HMAC SHA-256)
  - Max Speed: DDR: 104 MB/sec; SDR: 52 MB/sec
    - DDR: fixed block size of 512 B
  - Multiple Partition Support
  - Boot Operation Mode
  - Sleep Mode (CMD5): Vcc off

Current Standards – SD

- SD 3.01 (Feb, 2010)
  - SDXC (Extended Capacity): 32 GB – 2 TB
  - Signaling Voltage (3.3/1.8 V) CMD11
  - Max Speed (UHS-I: UHS50, UHS104)
    - Data (3.3 V signaling): 25 MB/sec (4*50)
    - Data (1.8 V signaling): 104 MB/sec (4*208); DDR50: 50MB/sec
    - Start from 3.3 V, CMD11 to switch to 1.8 V
- eSD Addendum (Nov, 2008)
  - Sleep mode
  - Partition/Boot
- SD Host Controller 3.0 (Feb, 2010)
  - ADMA
  - Registers Added:
    - Host Control 2
    - Preset Value (Clock, driver strength)
    - Shared Bus Control
  - Set Block Count Command (CMD23)

Freescale eSDHC

- Works with SD/miniSD/SDHC, MMC/MMC*plus*/RS-MMC cards
- Card bus clock frequency up to 52 MHz
- Supports 1-/4-bit SD mode, 1-/4-/8-bit MMC modes
- Single- and multi-block read and write
- Fully configurable 128 × 32-bit FIFO for read/write data
- Internal DMA capabilities



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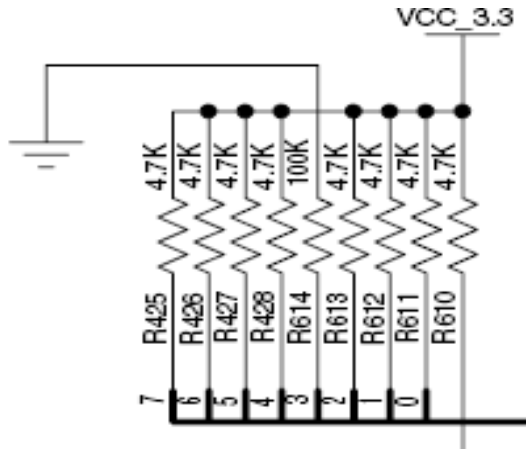
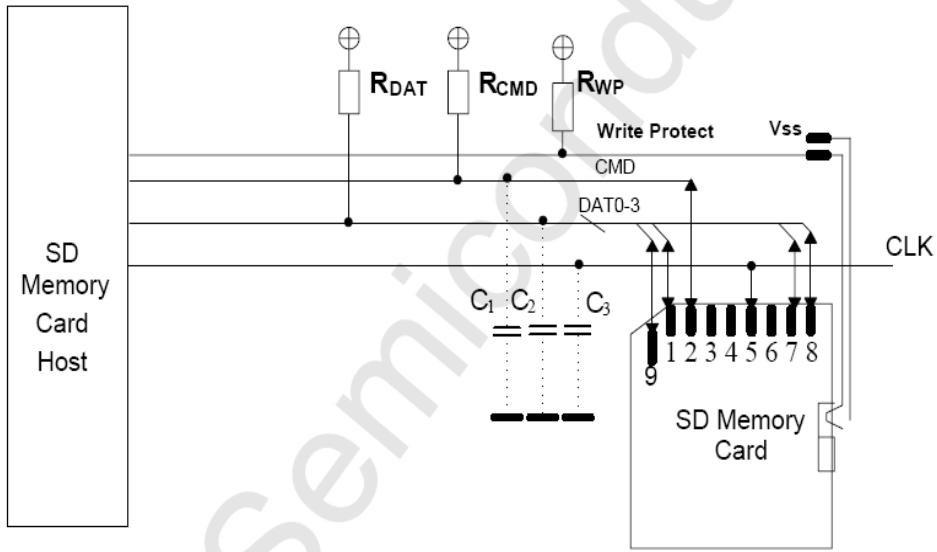
- Pull-up Resistor
  - MMC
    - CMD: 4.7 --- 100 KΩ
    - DAT: 50 --- 100 KΩ
  - SD
    - CMD/DAT: 10 --- 100 KΩ
- DAT3 as Card Detect (CD) pin
  - Only for SD cards
  - 100 KΩ Pull-down recommended
  - ACMD42 (on/off)





Memory Mapped registers

- DSADDR - DMA System Address Register
  - Check PRSSTAT[DLA] cleared before access
- BLKATTR - Block Attribute Register
  - Number of data blocks
  - Block size in terms of bytes in each block
- CMDARG – Command Argument Register
- XFERTYP – Transfer Type Register
  - Writing to this register will issue a command
  - Check PRSSTAT[CIHB] before write
  - Check PRSSTAT[CDIHB] before write if Tx/Rx data
- DATPORT – Buffer Data Port Register
  - 32-bit data port register used to access the internal buffer
  - Do not read if a write transaction is in operation

Memory Mapped registers

- PRSSTAT – Present State Register
  - The status of the eSDHC to the host driver
- PROCTL – Protocol Control Register
  - Configure DAT3 as CD pin
  - Bit mode
- SYSCTL – System Control Register
  - Setup SDHC clock, and timer out value
- IRQSTAT – Interrupt Status Register
- IRQSTATEN – Interrupt Status Enable Register
- IRQSIGEN – Interrupt Signal Enable Register
  - Which interrupt signal will set a bit in IRQSTAT

Memory Mapped registers

- AUTOC12ERR – Auto CMD12 Error Status Register
  - Only valid when IRQSTAT[AC12E] is set
- HOSTCAPBLT – Host Controller Capabilities Register
  - Voltage range
  - High Speed (25 – 50 MHz for SD, 26 – 52 MHz for MMC)
- CMDRSP 0-3 – Command response 0 - 3 Registers

Response Type	Meaning of Response	Response Field	Response Register
R1,R1b (normal response)	Card status	R[39:8]	CMDRSP0
R1b (Auto CMD12 response)	Card status for Auto CMD12	R[39:8]	CMDRSP3
R2 (CID, CSD register)	CID/CSD register [127:8]	R[127:8]	{CMDRSP3[23:0], CMDRSP2, CMDRSP1, CMDRSP0}
R3 (OCR register)	OCR register for memory	R[39:8]	CMDRSP0
R4 (OCR register)	OCR register for I/O etc.	R[39:8]	CMDRSP0
R6 (publish RCA)	New published RCA[31:16] and card status[15:0]	R[39:9]	CMDRSP0

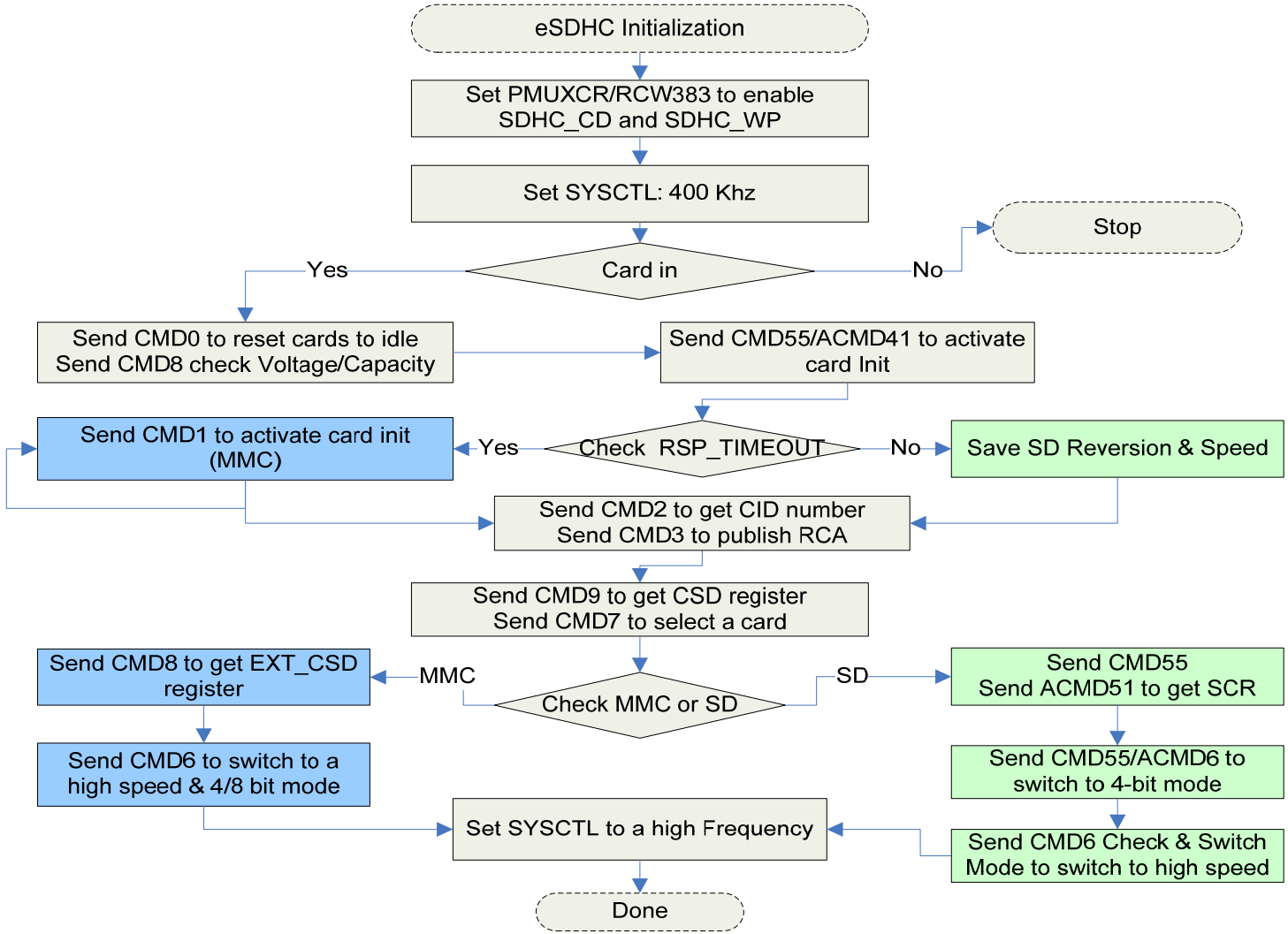
Memory Mapped registers

- WML – Watermark Level Register
  - Write/Read watermark level: number of 32-bit words
  - Min Value: 2 (8 bytes)
  - Max Read: 16 (64 Bytes)
- FEVT – Force Event Register
  - Write only: 1 set the corresponding bit in IRQSTAT if…
- HOSTVER – Host Controller Version Register
  - Read only
- DCR – DMA Controller Register
  - Snoop should be set if DMA is enabled

Other Memory Mapped registers

- PMUXCR – Alternate Function Signal Multiplex Control Register
  - Data Mux for date line 4-7 with SPI_CS
  - CD/WP pins with GPIO
  - 8536/P2020/8569/P102x
- RCW 383 bit/369-370
  - Data Mux for date line 4-7 with SPI_CS
  - CD/WP pins with GPIO
  - P4080/P3040/P5020

Card Initialization and Identification Flow



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Boot From a SD/MMC card

- Boot_Rom Based Booting
  - MPC8536/MPC8569/P2020/P1020/P1022/P1023/P1010
    - cfg_rom_loc: 0111
- PBL (Pre-Boot Bloader) Based Booting
  - P4080/P3040/P5020/P2040
    - cfg_rcw_src: 0_01100

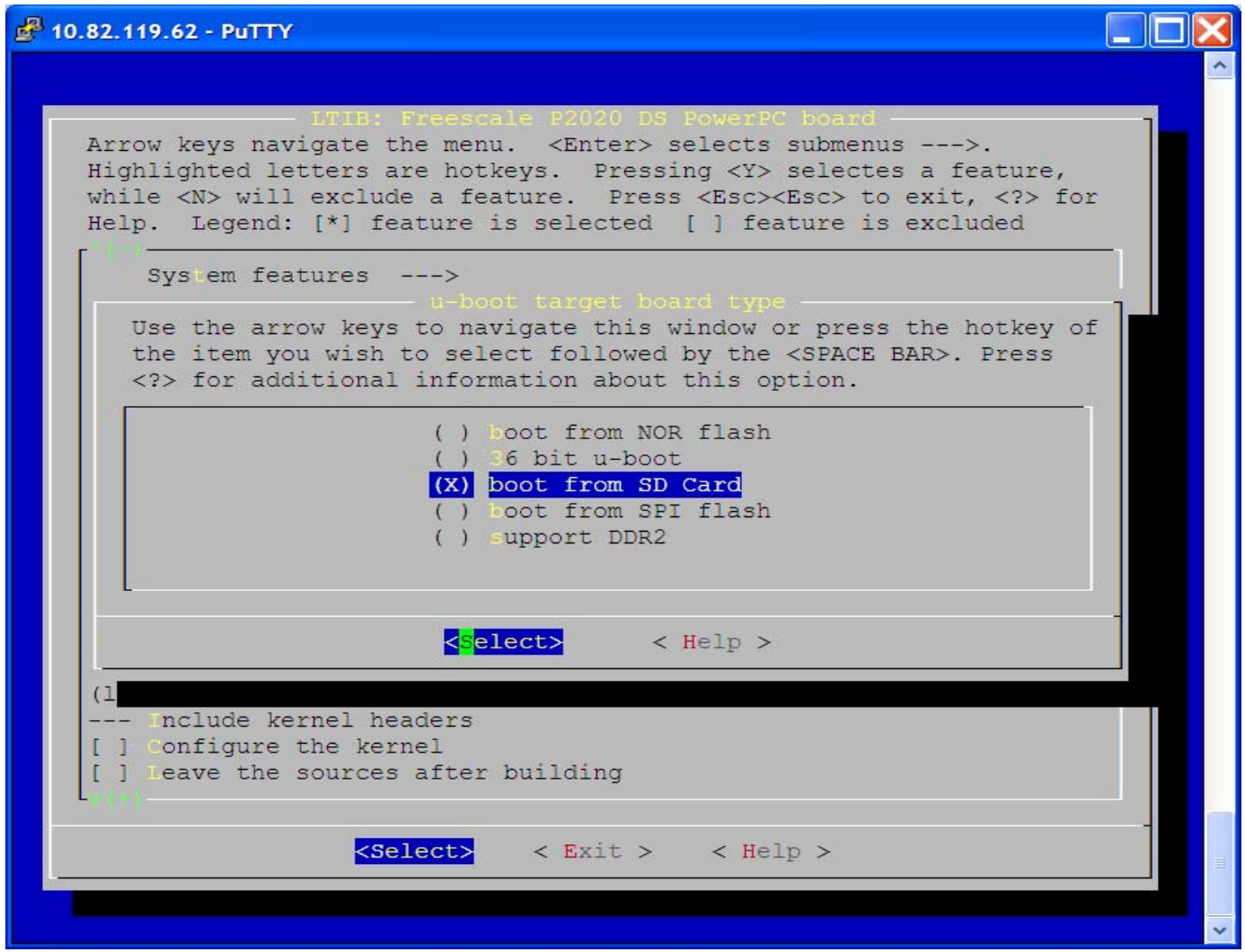
Boot_Rom Based Booting

- On-chip Boot ROM
- Ram Based u-boot or Special Build Boot Loader Code
- Configuration File
- Utility Tool
- SD/MMC card Format

On-chip Boot ROM

- A simple eSDHC driver
- 8 KB size (Address: 0xFFFF_E000)
- Initialization
  - Setup a TLB1:
    - Size: 2 Gbytes
    - IMG (Caching-inhibited, Memory coherence required, Guarded)
    - Permission: SX/SW/SR
  - Set the PMUXCR: CD/WP pins exposed
  - Switch to high speed if necessary
- Read
  - Internal DMA
- Error Indication: System keep resetting

Ram Based u-boot



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Ram Based u-boot

- Changes needed:
  - config.h

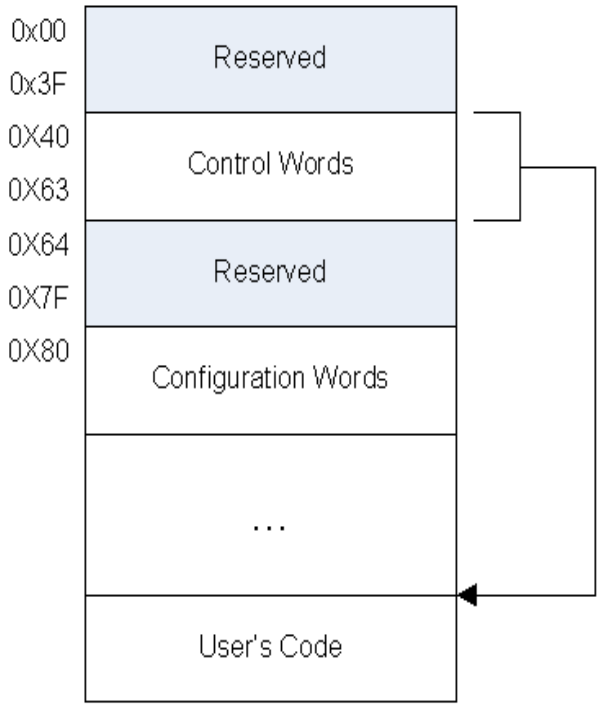
```
#define CONFIG_MK_SDCARD 1
```

  - config.mk

```
ifeq ($(CONFIG_MK_SDCARD), y)
TEXT_BASE = $(CONFIG_RAMBOOT_TEXT_BASE)
ifdef CONFIG_SYS_FSL_BOOT_DDR
RESET_VECTOR_ADDRESS = 0x1107fffc
else
RESET_VECTOR_ADDRESS = 0xf8fffffc
endif
endif
```

Configuration File

- Data Structure
  - 0x40: BOOT signature (0x424F4F54)
  - 0x48: User's code length in bytes
  - 0x50: Source Address
    - Standard card: byte address
    - High capacity card: block address
  - 0x60: number of configuration words
    - Max 40 Pairs (FAT)
  - Configuration Words
    - At least 1 LAW
    - L2SRAM (L2 size >= 512 KB) (Better)
    - DDR (L2 < 512 KB)



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Utility Tool / SD/MMC Card Format

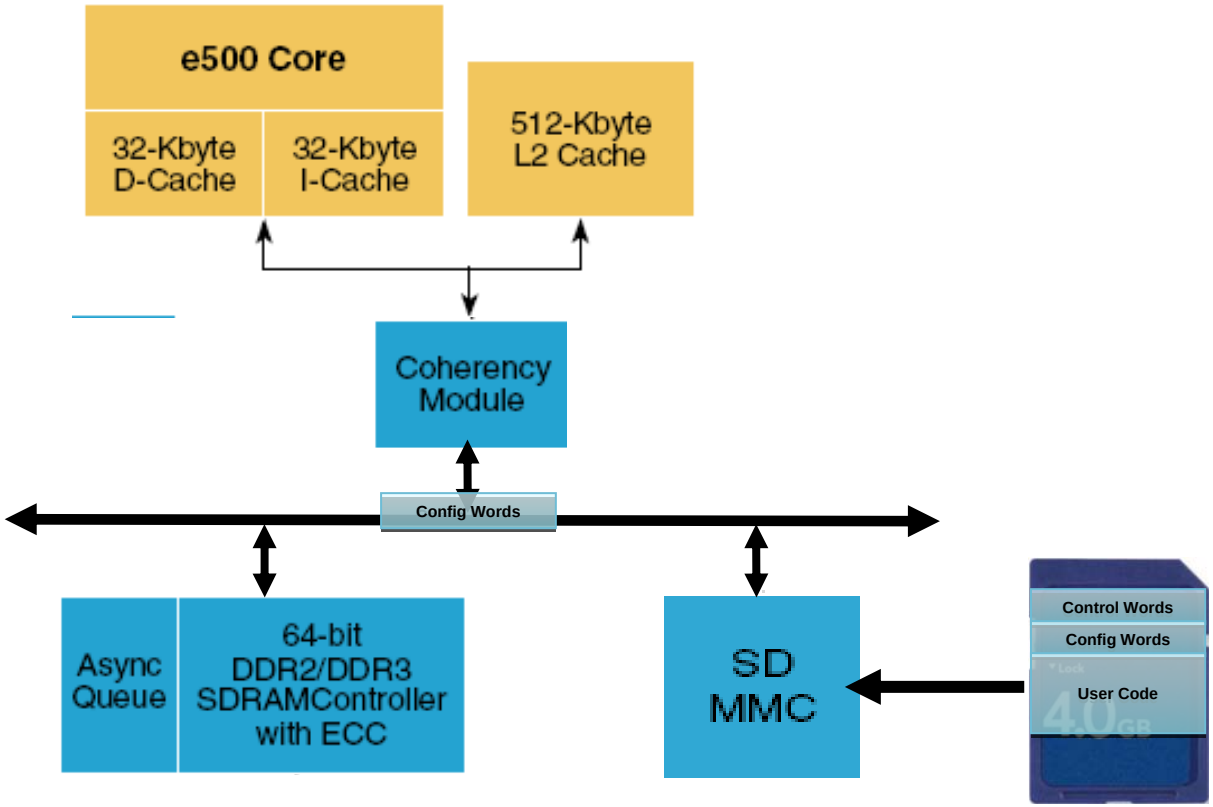
- Unix Based Utility
  - Name: boot_format
  - Does not support FAT12
  - Configuration Info/Image can be not seen (ls)
  - Usage:
    - `./boot_format <config_file> <image> –sd /dev/<sd*>`
- SD/MMC card Format
  - File System Specification Rev 2.0, May 2006
    - FAT16: <= 2 GB
    - FAT32: > 2 GB
  - Two Partitions
    - FAT: configurations/user code (u-boot.bin)
    - Linux: Kernel/RFS

config_sram.dat

```
40:424f4f54 ===> "BOOT" in ASCII
44:00000000 ===> Reserved
48:00080000 ===> User's Code Length 0x80000=512KB
4c:00000000 ===> Reserved
50:00001000 ===> Source Address Offset from SD Card
54:00000000 ===> Reserved
58:f8f80000 ===> Target Address (L2 in this case)
5c:00000000 ===> Reserved
60:f8fff000 ===> Execution Starting Address
64:00000000 ===> Reserved
68:00000006 ===> Number of config addr/data pairs

80:ff720100 ===> Addr Mode - L2SRBAR0
84:f8f80000 ===> Map L2 as SRAM with Base 0xf80000
88:ff720e44 ===> Addr Mode - L2ERRDIS
8c:0000000c ===> Disable ECC error detect
90:ff720000 ===> Addr Mode - L2CTL
94:80010000 ===> Enable L2, Entire 512KB is SRAM
98:ff72e40c ===> Addr Mode - DCR (eSDHC DMA Control Reg)
9c:00000040 ===> Read Safe (can read more byte than intended)
a0:40000001 ===> Data Mode - Delay VAL[a4]*8CCB clks
a4:00000100 ===> 0x100 hex factor
a8:80000001 ===> Data Mode - End Configuration
ac:80000001 ===> End Configuration
```

Boot From a SD/MMC card



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Demo

- P2020RDB-PB
- NOR Boot
- Boot from SD


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