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LNA Design Trade-Offs in the Working World

Tim Das, Sr. MMIC Applications Engineer

Thanks to Jeff Ho, and J. Staudinger
AGENDA: LNA Design Trade-Offs in the Working World

► Prelude
  • Noise Figure Measurement
  • Noise Parameters
  • NF Specification

► Device-Level Considerations
  • Transistors: FET vs. BJT
  • Viable Process Technologies
  • Device Sizing
  • Package Parasites

► Board-Level Considerations
  • Circuit Topologies
  • Biasing Setting
  • Instability
  • Feedback
  • Input and Output Matching
  • Linearity

► Design Example based on Freescale GaAs pHEMT LNA
Prelude: Noise Figure Measurement & Specification
Noise Figure Measurement

Measurement Uncertainty

- Analysis of measurement uncertainties can motivate setup changes for improved measurement repeatability.

- A useful NF uncertainty calculator is available from Agilent.

- Refer to the vast library of excellent NF Application Notes from Agilent.
## Noise Parameters

- Characterize any two-port network at a given frequency, temperature, and bias.

<table>
<thead>
<tr>
<th>F&lt;sub&gt;MIN&lt;/sub&gt;</th>
<th>minimum noise factor occurs at Y&lt;sub&gt;OPT&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>R&lt;sub&gt;N&lt;/sub&gt;</td>
<td>F sensitivity to Y&lt;sub&gt;IN&lt;/sub&gt; deviating from Y&lt;sub&gt;OPT&lt;/sub&gt;</td>
</tr>
<tr>
<td>Y&lt;sub&gt;OPT&lt;/sub&gt; = G&lt;sub&gt;OPT&lt;/sub&gt; + jB&lt;sub&gt;OPT&lt;/sub&gt;</td>
<td>Signal source admittance for F = F&lt;sub&gt;MIN&lt;/sub&gt;</td>
</tr>
<tr>
<td>Y&lt;sub&gt;IN&lt;/sub&gt; = G&lt;sub&gt;IN&lt;/sub&gt; + jB&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input admittance looking into LNA</td>
</tr>
</tbody>
</table>

\[
F(Y_{IN}) = \frac{SNR_{INPUT}}{SNR_{OUTPUT}} = F_{MIN} + \frac{R_{N}}{G_{IN}} |Y_{IN} - Y_{OPT}|^2
\]

- Derived from noise circles
Noise Figure Specification

▸ Fixture/Board Losses in NF Measurement

- Noise Figure measurement necessarily includes test fixture losses

- These losses on LNA input can be significant for sub-1dB NF measurement
## Comparing NF specifications

- LNA manufacturers choose to specify:

<table>
<thead>
<tr>
<th>Option 1</th>
<th>Option 2</th>
<th>Option 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NF as measured</strong></td>
<td><strong>NF with ( Y_{IN} = Y_{OPT} )</strong></td>
<td><strong>NF with fixture/board losses de-embedded</strong></td>
</tr>
<tr>
<td>Reproducible by customer</td>
<td>( NF_{OPT} )</td>
<td>Isolates LNA contribution</td>
</tr>
<tr>
<td>Performance can be easily compared to other LNAs</td>
<td>Not easily comparable with other LNAs</td>
<td>Comparisons should be mindful of subtracted losses</td>
</tr>
</tbody>
</table>

- Be careful when input matching network losses are de-embedded from NF.
- All comparisons between devices/designs should share the same reference plane (\( Z_o = 50\Omega \))
RF Performance is dependant on many variables

- Device-Level Variables
  - Device Geometry
  - Process Technology
  - Layout & Grounding
  - Package Parasitics
- Board-Level Variables
  - Frequency
  - Feedback
  - Input Matching
  - Temperature
  - Layout & Grounding
  - EM Shielding
  - Stability
  - Power Dissipation
  - Biasing & Power Dissipation
  - Output Matching
  - Supply Decoupling
LNA Design Trade-Offs

Multi-dimensional Balancing Act!

- Noise Figure
- Gain
- Linearity
- Power Consumption
- Port Matching
- Stability
- Size
- Manufacturability
- Ruggedness
- B.O.M. cost
LNA Design Trade-Offs: Device-Level Considerations
### Transistors: FET vs. BJT

<table>
<thead>
<tr>
<th>FET (pHEMT)</th>
<th>BJT (HBT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Higher gate resistance and thermal noise.</td>
<td>Shot noise</td>
</tr>
<tr>
<td>• Noise performance strongly dependant on gate geometry.</td>
<td></td>
</tr>
<tr>
<td>Optimal NF bias close to max gain bias.</td>
<td>• Optimal bias for NF is considerably lower than max gain bias.</td>
</tr>
<tr>
<td>• A trade-off is required.</td>
<td></td>
</tr>
<tr>
<td>Lower $R_e[\text{Y}_{\text{OPT}}]$</td>
<td>Higher $R_e[\text{Y}_{\text{OPT}}]$</td>
</tr>
<tr>
<td>ESD protection to avoid gate rupture</td>
<td>Ballast resistor is required for thermal run-away.</td>
</tr>
<tr>
<td>Prone to low frequency oscillation due to very high low frequency gain.</td>
<td>Higher transconductance</td>
</tr>
</tbody>
</table>
## Viable Process Technologies for L & S-Band Applications

<table>
<thead>
<tr>
<th>Low-Noise Amplifiers</th>
<th>GaAs pHEMT</th>
<th>GaAs HBT</th>
<th>SiGe BiCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Typical Noise Figure</strong></td>
<td>≥ 0.5 dB</td>
<td>≥ 1.4 dB</td>
<td>≥ 0.9 dB</td>
</tr>
<tr>
<td><strong>Typical Gain</strong></td>
<td>12 – 21 dB</td>
<td>8 - 13 dB</td>
<td>10 – 17 dB</td>
</tr>
<tr>
<td><strong>Typical oIP3</strong></td>
<td>≤ 41 dBm</td>
<td>≤ 30 dBm</td>
<td>≤ 31 dBm</td>
</tr>
<tr>
<td><strong>Breakdown Voltage (BV&lt;sub&gt;CEO&lt;/sub&gt;)</strong></td>
<td>~15 V</td>
<td>~16.5 V</td>
<td>~4 V</td>
</tr>
<tr>
<td><strong>f&lt;sub&gt;T&lt;/sub&gt; / f&lt;sub&gt;MAX&lt;/sub&gt;</strong></td>
<td>Similar</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Typ. Inductor Q-factor</strong></td>
<td>~15</td>
<td>~15</td>
<td>5 - 10</td>
</tr>
<tr>
<td><strong>Strengths</strong></td>
<td>High P1dB, high IP3, and very low noise</td>
<td>Moderate performance at lower cost</td>
<td>Higher integration, lower cost, ESD immunity</td>
</tr>
</tbody>
</table>

**Typical Strengths**:
- **High P1dB, high IP3, and very low noise** for GaAs pHEMT.
- **Moderate performance at lower cost** for GaAs HBT.
- **Higher integration, lower cost, ESD immunity** for SiGe BiCMOS.
Gain vs. Noise Figure

"Mid-Band" Single-Stage Low-Noise Amplifiers (1400MHz to 2200MHz)

- **GaAs pHEMT**
- **SiGe BiCMOS**
- **GaAs HBT**
- **Freescale**
  - MML20211H
  - GaAs pHEMT

**Best Performers**

**Worst Performers**

**Typical Noise Figure @ 2000MHz, [dB]**

**Gain @ 2000MHz, [dB]**

- GaAs HBT: RF2314 (3v), RF2314 (5v), RF2878
- GaAs pHEMT: SPF-50432 (5v), SPF-51222 (5v), RF3861, FPD2250SOT89E, FPD750SOT89E, FPM21500QFN, FPM2750QFN, RF3863, HMC374, HMC382LP3, HMC669LP3 (5v), HMC818LP4E (5v), HMC758LP3 (5v), ADL5521 (5v), ADL5523 (5v), MGA-30889, MGA-53543, MGA-53589, MGA-85563, MGA-87563

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Viable Process Technologies

Output IP3 vs. Noise Figure

"Mid-Band" Single-Stage Low-Noise Amplifiers (1400MHz to 2200MHz)

Typical Noise Figure @ 2000MHz, [dB]

Output IP3 @ 2000MHz, [dBm]

Best Performers

GaAs HBT
SiGe BiCMOS
GaAs pHEMT
Freescale
MML20211H
GaAs pHEMT

Worst Performers

SiGe BiCMOS
SKY65047-360LF
MAX2641
SGA-8343(Z)
MBC13720
MBC13916
MC13853
BGA2001
BGA2003
BGA2012
BGA622L7
BGA711L7
BGA735N16
BGA736L16
LNAs better suited to high IP3, low NF applications

LNAs better suited to low power, battery powered applications
Device-Level Considerations

► Device Sizing

- Sizing a device for 50Ω matching provides good wideband performance.

- Shrinking FET size reduces power consumption, at the expense of Gain and IP3 performance.

- Base/Gate resistance increases as device size shrinks which would directly impact NF performance.

- Theoretically, there exists an optimal transistor size which moves $Y_{\text{OPT}}$ and $Y_{\text{IN}}$ closer together, while minimizing $R_N$.
Device-Level Considerations

- NF performance is strongly affected by FET gate dimensions

  - Narrower and shorter gate fingers improve $F_{\text{MIN}}$, by lowering gate resistance, and improving high-frequency gain and stability.

  - Wider gate width or multiple gate fingers increases transistor transconductance ($g_m$)
Cascode Amplifiers: Device Sizing

- The CS transistor size and bias point should be optimized for lowest NF.

- Size CG for AM/PM conversion characteristic opposite to that of the CS-stage. AM/PM cancellation improves linearity performance.

- Size CG for P1dB requirement
Device-Level Considerations

Package Parasitics

- Account for bond-wire parasitics and variation
  - Bond-wire parasitics on LNA input has profound effect on LNA performance.
  - Self-inductance can be used constructively for input matching and source/emitter degen *if* well controlled.
- Pad & Package capacitance has significant impact on input impedance matching, transistor $g_m$, and NF.
# Circuit Topologies

## Typical Characteristics for L & S-Band LNAs

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Common-Source (CS)</th>
<th>Common-Gate (CG)</th>
<th>Cascode</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_{\text{MIN}}$</td>
<td>Best</td>
<td>Better</td>
<td>Good</td>
</tr>
<tr>
<td>$R_N$</td>
<td>Higher</td>
<td>Lower</td>
<td>Middle</td>
</tr>
<tr>
<td>Gain</td>
<td>Moderate</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>Narrow</td>
<td>Very Wide</td>
<td>Wide</td>
</tr>
<tr>
<td>Stability</td>
<td>Compensation often required</td>
<td>RF decoupling of gate important</td>
<td>Good</td>
</tr>
<tr>
<td>Reverse Isolation</td>
<td>Lower</td>
<td>Moderate</td>
<td>Best</td>
</tr>
</tbody>
</table>
## Typical Characteristics for L & S-Band LNAs

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Common-Source (CS)</th>
<th>Common-Gate (CG)</th>
<th>Cascode</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Port Matching</strong></td>
<td>High Q input matching network feedback helps move $Y_{IN}$ closer to $Y_{OPT}$</td>
<td>Low Q input matching network</td>
<td>Low Q input matching network</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output VSWR not good</td>
<td>Output VSWR not good</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Must also consider inter-stage noise matching</td>
</tr>
<tr>
<td><strong>Sensitivities</strong></td>
<td>More sensitive</td>
<td>More robust</td>
<td>More robust</td>
</tr>
<tr>
<td>to process, voltage,</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>temperature variations</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
LNA Design Trade-Offs: Board-Level Considerations
Board-Level Considerations

**Bias Setting**

- Trade-off optimal NF and Gain with drain current setting

---

**Gain and NF vs. Drain Current**

MML09211H LNA measured @ 900 MHz
Vs supply = 5.0V, Temp = 25°C

NF for SiGe BiCMOS increases more rapidly than GaAs pHEMT as collector/drain current is increased.
**Board-Level Considerations**

**Bias Setting**

- Added Dimension: Trade-off NF, Gain and IP3 performance

Here the bias point for Max IP3 and Max Gain are close.

GaAs pHEMT allows for a better trade-off between high linearity and low NF than SiGe BiCMOS.

However, low power battery powered applications cannot afford high drain/collector currents.
Board-Level Considerations

► Bias Setting

- **Integrated Active-Bias**
  - Temperature compensated bias current
    - Gain variation over temperature is reduced
  - Reject supply variations
    - Decouple low frequency (< 40MHz) interference on supply lines.
  - Absorbs process variations
Board-Level Considerations

Stability

- Use stability circles (for source and load) to verify legitimacy of chosen $Z_{IN}$ and $Z_{OUT}$.

- **Always** check stability of your design (well beyond band-of-interest)
  - Small-signal stability ($K$, $B_1$ or $\mu$ factors)
  - Large-signal stability
Board-Level Considerations

Circuit Instability

- Address most common causes

  - Insufficient RF decoupling between supply lines of amplifier stages
  - Parasitic inductance in GND connections.
  - Excess in-band and/or out-of-band gain
  - Insufficiently decoupled supply lines
  - EM coupling
Circuit Stability

- Methods of Compensation
  - RF Feedback
  - Filtering to knock down excessive out-of-band gain
  - Resistive Damping
    - Shunt resistance across LNA output
      preferred over
    - Shunt resistance across LNA input (your last resort)
    - Directly impacts NF, gain, and dynamic range
Feedback

- C-S LNA: Source/Emitter Degeneration
  - Small inductance on the source/emitter appears as real portion on $Y_{IN}$.
  - Improve stability and linearity at the expense of gain, especially at higher frequencies.
  - Can move $Y_{IN}$ closer to $Y_{OPT}$ closer together on the Smith chart.

The ideal value for source degen inductance can be sought empirically using a laser trimmable structure.
Feedback

- C-G Shunt Feedback
  - Improve linearity and stability, at the expense of gain especially at higher frequencies

- Cascode Shunt RC Feedback
  - Improve stability, gain flatness, and bandwidth, at the expense of gain
  - Moves match for Max Gain closer to $Y_{OPT}$
  - Large $R_{FB}$ values improves input VSWR without significant impact on NF ($>1$ kΩ)
Input Matching

- Without feedback and/or optimal transistor sizing, $Y_{OPT}$ and conjugate matching points usually do not coincide.
- Minimize the number of components needed on the LNA input.
- High Q networks are sensitive to variations in process, voltage, temperature, and component value.
Source/Emitter Degeneration

- $Y_{IN}$ moves closer to $Y_{OPT}$

**Input Conjugate Match and Noise Circles**

- $L_s = 0.6 \text{ nH}$
- $Y_{OPT}$ Noise Circles
- cir_pts (0.000 to 51.000)
- freq (700.0MHz to 1.000GHz)

**Y_{CM}: Optimal Conjugate Match**

- $L = 0.2$ to $0.6 \text{ nH}$
Board-Level Considerations

Input Matching

Source degen moves $Y_{\text{OPT}}$ closer to $Y_{\text{CM}}$

Then input matching network can provide VSWR ~ 1 AND good NF
Output Matching

- Optimal IP3, Max Gain, and conjugate matching points do not coincide.

- Gain and IP3 circles are measured using load-pull techniques

- Find trade-off between gain, IP3, and ORL with output matching network.
LNA Design Trade-Offs: Design Example
MML09211H – Ultra Low Noise Amplifier

• Frequency performance: 400 – 1400 MHz
• 0.5 dB Noise Figure @ 900 MHz (In Fixture)
• High Isolation
• IIP3 = 12 dBm

• Noise Figure includes connector, board and matching loss
Design LNA for 900MHz GSM base-station receiver

Lets try to improve upon the “state of the art” MMIC solution with Freescale’s MML09211H GaAs pHEMT LNA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>@ 900MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF</td>
<td>0.64 dB</td>
</tr>
<tr>
<td>Gain</td>
<td>18.8 dB</td>
</tr>
<tr>
<td>Output IP3</td>
<td>32.0 dBm</td>
</tr>
<tr>
<td>IRL / ORL</td>
<td>&gt; 15 dB</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>232 mW</td>
</tr>
</tbody>
</table>

Starting point:

- Start with datasheet nominal operating conditions
- Start with conjugate matches on input and output
The designer might first consider the need for feedback.

MML09211H primary feedback is integrated on-chip: No worries!

Let's jump to finding the optimal bias point.

$I_D$ set to 10 - 15% of $I_{DMAX}$ should come close to hitting the design targets.
Find optimal input match: Trade-off between Gain and NF

Let's set input match for optimal NF performance

\[ Y_{IN} = Y_{OPT} \]
\[ NF = 0.52 \text{ dB} \]
\[ IRL = 17.6 \text{ dB} \]
\[ \text{Gain} = 20.7 \text{ dB} \]

\[ f = 900 \text{MHz} \]
Next, determine how much Gain can be improved without too much NF degradation.

\[ f = 900\text{MHz} \]

Gain = 21.1 dB

\[ \text{NF} = 0.52\text{ dB} \]
\[ \text{IRL} = 19.4\text{ dB} \]

We’ve found an acceptable trade-off: implement matching network to this impedance and apply to LNA input.
Find optimal output match: balance gain vs. IP3 trade-off

Consider Scenario 1: Set output match for optimal Gain and ORL

- Gain = 23.2 dB
- oIP3 = 30.2 dBm
- ORL = 21.2 dB

\( f = 900 \text{MHz} \)
► Consider Scenario 2: Use load-pull techniques to determine the output match for optimal IP3 performance.

\[ f = 900 \text{MHz} \]

Gain = 18.9 dB, 
\( o_{IP3} = 36.2 \text{ dBm} \)

ORL = 9.4 dB

Even higher \( o_{IP3} \) performance is attainable at the expense of ORL and Gain.
Consider Scenario 3: Let's look for a trade-off between scenarios 1 & 2

\[ f = 900\text{MHz} \]

Gain = 22.9 dB,  
oIP3 = 33.3 dBm  
ORL = 14.0 dB

Scenario 3 finds a suitable trade-off for output matching

- Implement matching network to this impedance and apply to LNA output
MML09211H Design Example

► Implement both the input and output matching networks

► Is actual performance a little off target?

► If so, fine tune component values and placement.
- Check Stability of solution

If either stab_fact is >1 or stab_meas >0, the circuit is unconditionally stable.

We also check Large-Signal Stability: no unexplained spurs or humps anywhere on output spectrum

Unconditionally Stable!
MML09211H Design Example

► Measured Noise Figure (in test fixture, in shielded room, with no losses de-embedded)

MML09211H: Noise Figure vs. Frequency

![Graph showing Noise Figure vs. Frequency for MML09211H](image-url)
Actual Measured Performance (no losses de-embedded)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MML09211H solution @ 900MHz</th>
<th>Improvement over “state of the art” solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF</td>
<td>0.50</td>
<td>-0.14 dB</td>
</tr>
<tr>
<td>Gain</td>
<td>21.2 dB</td>
<td>+2.4 dB</td>
</tr>
<tr>
<td>Output IP3</td>
<td>32.0 dBm</td>
<td>0 dB</td>
</tr>
<tr>
<td>IRL / ORL</td>
<td>23 dB / 18 dB</td>
<td>&gt; 15 dB</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>330 mW</td>
<td>+98 mW</td>
</tr>
</tbody>
</table>
## 900MHz Receiver LNA Solutions

<table>
<thead>
<tr>
<th>LNA Type</th>
<th>Performance</th>
<th>Key Features</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MML09211H</strong></td>
<td>0.5 dB NF, 21 dB Gain</td>
<td>OIP3: 32 dBm, Gain: 21 dB, NF: 0.5 dB, Freq: 400 – 1400 MHz, DFN 2X2 package, Idd: 65 mA</td>
</tr>
<tr>
<td><strong>MMG15241H</strong></td>
<td>1.5 dB NF, 20 dB Gain</td>
<td>OIP3: 38 dB, Gain: 20 dB, NF: 1.5, Freq: 500 – 2800 MHz, SOT-89 package, Idd: 85 mA</td>
</tr>
<tr>
<td><strong>MML09212H</strong></td>
<td>0.7 dB NF, 35 dB Gain</td>
<td>OIP3: 38 dB, Gain: 35 dB, NF: 0.7, High gain and low NF, Idd: 140 mA</td>
</tr>
</tbody>
</table>

*1st stage LNA*
## 2100MHz Receiver LNA Solutions

<table>
<thead>
<tr>
<th>LNA Model</th>
<th>Performance</th>
<th>Key Features</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MML20211H</strong></td>
<td>OIP3: 32 dBm, Gain: 21 dB, NF: 0.5 dB</td>
<td>0.8 dB NF, 21 dB Gain</td>
</tr>
<tr>
<td><strong>MMG15241H</strong></td>
<td>OIP3: 38 dB, Gain: 16 dB, NF: 1.5</td>
<td>1.5 dB NF, 20 dB Gain</td>
</tr>
<tr>
<td><strong>MML20242H</strong></td>
<td>OIP3: 38 dB, Gain: 32 dB, NF: 0.8</td>
<td>0.8 dB NF, 32 dB Gain</td>
</tr>
</tbody>
</table>

## Key Features

- **MML20211H**
  - Freq: 400 – 1400MHz
  - DFN 2X2 package
  - Idd: 65 mA

- **MMG15241H**
  - Freq: 500 – 2800 MHz
  - SOT-89 package
  - Idd: 85 mA

- **MML20242H**
  - Freq: 1400 – 2800 MHz
  - High gain and low NF
  - Idd: 140 mA

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1\(^{st}\) stage LNA

2\(^{nd}\) stage LNA

1\(^{st}\) stage LNA

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Freescale GaAs LNA Roadmap

- **MML09211H**, NF=0.5 dB, Gain=21 dB, IIP3=11 dBm, Idd=60 mA, DFN2x2
- **MML04211H**, NF=0.5 dB, Gain=20 dB, IIP3=12 dBm, Idd=60 mA, DFN2x2
- **MML04212H**, NF=0.65 dB, Gain=35 dB, IIP3=7 dBm, Idd=140 mA, QFN3x3
- **MML09212H**, NF=0.65 dB, Gain=35 dB, IIP3=7 dBm, Idd=140 mA, QFN3x3
- **MML20211H**, NF=0.8 dB, Gain=18 dB, IIP3=16 dBm, Idd=65 mA, DFN2x2
- **MML20242H**, NF=0.9 dB, Gain=32 dB, IIP3=7 dBm, Idd=140 mA, QFN3x3
- **MMG15241H**, NF=1.6 dB, Gain=15 dB, OIP3=39 dBm, Idd=85 mA, SOT-89
- **MMG09271H**, NF=1.8 dB, Gain=20 dB, OIP3=43 dBm, Idd=175 mA, QFN3X3
- **MMG09271H**, NF=1.8 dB, Gain=20 dB, OIP3=43 dBm, Idd=175 mA, QFN3X3
- **MMG20271H**, NF=1.8 dB, Gain=15 dB, OIP3=43 dBm, Idd=175 mA, QFN3X3

- Noise Figure listed includes connectors and board losses

2009 | 2010 | 2011
Valuable Reference Materials

- CMOS Low-Noise Amplifier Design Optimization Techniques
  T-K Nguyen, C-H Kim, G-J Ihm, M-S Yang, S-G Lee
  IEEE Transactions on Microwave Theory and Techniques, Vol. 52, No. 5, 05/2004

- A Comparative Study on the Various Monolithic LNA Circuit Topologies for RF and Microwave Applications
  B.K. Ko, K. Lee

- Successful LNA Design Involves Performance Trade-Offs
  T. Baker, Freescale Semiconductor
  www.rfdesign.com

- An Introduction to Low-Noise Amplifier Design
  S. Mercer, RF Design, July 1998, pgs 44-56

- RF & Microwave Circuit Design for Wireless Ap…(Hardcover)

- Agilent’s Noise Figure Uncertainty tool

- Agilent’s library of noise figure application notes
  www.freescale.com/rfmmic