Module Introduction

Purpose
- This training module covers 68K/ColdFire Peripherals, including the ADC and timers

Objectives
- Explain the features of the ColdFire Analog-to-Digital Converter (ADC).
- Describe the timer systems and features available in the General Purpose Timer (GPT) module, DMA Timers, Timer Modules, and including time clock selection.
- Understand the output and input compare functions.
- Explain the features of the Pulse Width Modulation (PWM) module and the Programmable Interrupt Timer (PIT) module.

Content
- 22 pages
- 5 questions

Learning Time
- 30 minutes

This module introduces you to some of the ColdFire peripherals.

In this module, we will discuss the features of the Analog to Digital Converter (ADC), the timer system and features of the General Purpose Timer (GPT), output and input compare functions, DMA Timers, Timer Modules, and the Pulse Width Modulation (PWM) module and the Programmable Interrupt Timer (PIT) module.
Fast Analog to Digital Converter

**FEATURES**

- The Fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 12-bit ADCs.
  - Maximum ADC clock frequency of 5.0 MHz
  - Sampling rate up to 444k samples per second (2.25 µs conversion time max.)

- The ADC can be configured to perform a single scan and halt, perform a scan whenever triggered, or perform a programmed scan sequence repeatedly until manually stopped.

- The ADC can be configured for either *sequential* or *simultaneous* conversion.

- Optional interrupts can be generated at the end of the scan sequence if a channel is out of range or at several different zero crossing conditions.

This ADC, which is found on the MCF5211/12/13 devices, is a flexible converter that boasts many features.

It can be configured as one 8-channel A/D converter or as two 4-channel A/D converters.

The A/D runs at a frequency of up to 5.0 MHz. This allows for a conversion rate of 444k samples per second (worst case scenario). If in simultaneous and loop modes, the conversions occur more quickly, at a rate of 1.66 million samples per second.

Measures 10.5 **Effective Number of Bits (ENOB)** of accuracy (which is quite good for a 12-bit A/D). Offers power saving modes which allow automatic shutdown/startup of all or part of the ADC. This power saving setting is in the power management module.
The Queued Analog to Digital Converter Module (QADC) in the MCF5282 is a 10-bit, uni-polar successive approximation A/D converter. This A/D is on the MCF5280/1/2 and MCF5214/6 devices. The interface to the module consists of eight multi-function input/output pins, two reference voltage pins, and two power pins. There is built-in multiplexing and channel decode logic which can be enabled and used to reduce the number of analog inputs to the device. When multiplexing is deselected, up to eight channels can be individually fed in and read.

The channel select and device enable outputs of the device supports four 1-of-4 external multiplexers. Using the on-chip multiplexing support, up to 18 A/D channels can be read.

The internal sample and hold circuitry supports a sample time which is user programmable.

A sophisticated multi-level queuing system provides a high degree of flexibility in setting the order and frequency in which conversions take place. There is also built-in flexibility for initiating and terminating queue conversion operations. This control is supported with multiple interrupt capability.

Finally, the results can be read in one of three different selectable formats.
The block diagram for the QADC shows that eight pins are used for analog input.

Four of these pins are in the bidirectional Port QA and the other four pins are from the bidirectional Port QB. Each of these eight pins have other functionality related to the QADC module, aside from their ability to be set as multiplexed or non-multiplexed analog input or digital I/O.

Two of these functions are external trigger input and external multiplexing control.

The QADC also has a set of its own power pins as well as a set of high/low voltage reference pins.

The digital control block consists of a number of components including; control logic, the QADC clock, a periodic/interval timer, control and status registers, conversion command word and result table RAM. The control logic is used for conversion activities while the PIT is used for timed conversions. The control and status registers are used for mode selections and user control of the module. Control in this module allows for the setup of multiple queues of conversions and how each queue is triggered and terminated.

The analog subsystem consists of multiplexing circuitry and an analog-to-digital converter. A state machine in this subsystem controls conversion sequencing while a successive approximation register and end-of-conversion signal generation control the timing.
The MCF5249 Analog to Digital Converter is based on the sigma-delta concept with 12-bit resolution.

The analog portion must be external, such as an op amp or comparator.

It supports four muxed inputs.

Also, the AD out provides the reference voltage in PDM format, though an external R-C integrator circuit is required. The external circuitry for MCF5249 ADC, which is necessary for the ADC to work, is specific to the ADC on the MCF5249.
Now, let's check your understanding of what you have learned about the analog-to-digital converters.

**Correct.** MCF5211/2/3 devices have 12 bit ADCs and have up to 8 A/D inputs. The MCF5249 device is based on the sigma-delta concept. The MCF5280/1/2 queuing capability and up to 8 A/D inputs. (Note that the same ADC is used on the MCF5214/6 devices.)
Next, we will look at the features of the General Purpose Timers (GPT) of ColdFire. The MCF5282 has two 4-channel general purpose timer modules. Each channel consists of a 16-bit programmable counter driven by a seven-stage programmable prescaler. Each of the four timer channels per module can be configured to perform input capture or output compare. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can capture output waveforms and timer software delays. Additionally, one of the channels, channel three, can be configured as a pulse accumulator. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator. The pulse accumulator shares GPT channel three when in event mode.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. Additionally, two channels can work together for pulse modulation capability with variable pulse widths from microseconds to seconds. This capability can be made interactive for dynamically changing duty cycles or frequency control or it can operate continuously and without user intervention.

Clocking options include the prescaled system clock or external clock source via SYNCA or SYNCB.
DMA Timers

- 32-bit DMA Timers
  - Four independent timers with 32-bit free-running counters
  - 1 Input Capture unit and 1 Output Compare unit per timer
  - Selectable active-low pulse or pin toggle on counter compare
  - Optional free-running counter reset on compare
  - Interrupt or DMA transfer on capture or compare event

The MCF5282 has four Direct Memory Access (DMA) timer modules (DTIM0-DTIM3).

All four 32-bit free running timers provide input capture and reference compare capabilities, 15-ns resolution at 66 Mhz, programmable sources for the clock input including external clock, and a max timeout period of ~74 hours at 66Mhz.

The timers also provide a programmable mode for the output pin on reference compare, active-low pulse or pin toggle.

In addition, the modules can operate in free run or restart modes.

The DMA timers are also capable of generating an interrupt or DMA transfer on a capture event or reference compare.
The ColdFire family features independent 16-bit or 32-bit timers with programmable sources for the clock input, including an option for an external clock source. This module covers the 16-bit timers.

Each timer has an input capture and output compare function with programmable modes for the input pin, T in, and the output pin, Tout.

The timer can operate in a free running mode where the timer continues to run eventually overflowing back to zero and counting back up.

In the next few pages, we will present these two functions and auto restart.
Now let’s take a look at timer clock selection. The timer clock is designed to come from a variety of sources.

More specifically, the timer clock can be selected to come from the system clock, the system clock divided by sixteen, or the external timer input pin, T in.

This clock is then fed through an 8-bit prescaler. A prescaler value of zero will divide the clock by one where as a prescaler value of FF divides the clock by 256.

The 16-bit up counter register can be read at any time. However, a write to this register will reset the counter to zero. Another way to reset the counter is to clear the RST bit in the timer mode register. This will not only reset the counter to zero, it will also stop the timer from counting until this bit is set. The highest timer resolution is one system clock.

For example, the ColdFire 5206e running at a system clock of 54 MHz can result in a timer resolution of 18.5 nanoseconds and a maximum period of five seconds.
Question

In the ColdFire General Purpose (GP) timers, which of the following channels can be configured as a pulse accumulator? Click the correct answer and then click Done.

A. 1  
B. 2  
C. 3  
D. 4  
E. 5

Consider this question about the ColdFire General Purpose timer.

Correct!
Channel three in the ColdFire General Purpose (GP) timer can be configured as a pulse accumulator.  Note: General Purpose timers are only used in the 528x and later devices.
Let’s move on to the timer output compare function.

This function provides a mechanism to output a signal at a specific time.

It is very useful for generating pulse trains, one time pulse generation or single shot operation. It is also useful for generating periodic interrupts that are used to handle background tasks, such as scanning a keyboard, polling I/O, or checking status flags.

The output compare logic contains a 16-bit reference register that compares each timer clock to the 16-bit running counter.

If there is a match, the Tout pin will either toggle or produce an active low pulse for one system clock depending on the state of the OM bit in the timer mode register. The REF status bit is set and a timer interrupt occurs if enabled. At this point the 16-bit running counter will either continue counting up or reset to zero and start counting depending on whether you have the timer setup for free run or restart mode. Note that the new parts, such as the 528x, function slightly differently. They have the ability to set or clear the output pin which is more flexible than the active low pulse.

In order to use the timer in free run mode, the software will need to read the contents of the 16-bit running counter, add a value that represents a time that you want the event and/or interrupt to occur, and then write this value into the 16-bit reference register. When there is a match, the event, Tout, will occur and, if enabled, an interrupt will be generated.

In some cases, the function of the output pin, Tout, is not used. For example, to generate a periodic interrupt you need to set the timer to restart mode and load the 16-bit reference register with the time interval when you want the interrupt to occur. There is very little CPU overhead for this timer function, because once the timer is initialized it will run on its own.
We have examined the output compare function, now let’s take a look at the input capture function.

The input capture function provides a mechanism to capture the time at which an external event occurs.

It is very useful for measuring input pulses or timing an external event.

The timer has a 16-bit capture register that latches to the counter value when the corresponding input capture edge detector senses a defined transition of “T in”.

The capture edge [(CE)] bits (CE0-CE1) in the time mode register selects the type of transition triggering the capture. The capture choices are based on a rising edge, falling edge, any edge, or to inhibit the T in pin. Again these bits are named differently in the 528x and later parts, might need to differentiate.

Upon a capture event, the status bit CAP will be set and, if enabled, an interrupt will occur. Accurate time measurements of external events can be measured utilizing input capture. This can occur because it captures or time stamps when the event occurs within one timer clock tick without CPU intervention. The CPU only needs to service the timer before the second event occurs. CPU latency up to this point is irrelevant.

The Tin pin may also be used as an external edge programmable interrupt pin. You only need to set the Tin pin to capture the edge you want and to generate an interrupt when the edge occurs. The contents of the 16-bit capture register is usually ignored.
Consider this question about the output compare function.

Correct!
The output compare function generates pulse trains, one time pulse generation, or single shot operations. It also generates periodic interrupts that are used to handle background tasks, such as scanning a keyboard, polling I/O, or checking status flags. Finally, it contains a 16-bit reference register that compares each timer clock to the 16-bit running counter.
The Pulse Width Modulation (PWM) module shown here is found on the MCF5272. It generates a synchronous series of pulses having a programmable duty cycle. With a suitable low-pass filter, the PWM can be used as a digital-to-analog converter.

The PWM has the following features: three output compare pins, a double-buffered width register, variable-divide prescale, three independent PWM modules, and a byte-wide width register provides programmable control of duty cycle.
Let's look at the PWM module in more detail. The PWM is a simple free-running counter combined with a pulse width register and a comparator such that the output is cleared whenever the counter value exceeds the width register value. When the counter overflows, or "wraps around," its value becomes less than or equal to the value of the width register, and the output is set.

The width register is double-buffered so that a new value can be loaded for the next cycle without affecting the current cycle.

At the beginning of each period, the value of the width register is loaded into the width buffer, which feeds the comparator. This value is used for comparison during the next cycle.

The prescalar contains a variable divider that can reduce the incoming clock frequency by certain values between 1 and 32768.
The MCF5213 has an 8-bit, 8-channel PWM module, providing a total of eight independent PWM modules. Each channel has a programmable period and duty cycle as well as a dedicated counter.

Dedicated period and duty registers exist for each channel and are double buffered so that if they change while the channel is enabled, the change will not take effect until a certain condition exists.

Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The PWM outputs have programmable polarity, and they can be programmed as left aligned outputs or center aligned outputs.

There are four available clocks—clock A, B, SA (scaled A), and SB (scaled B)—all based on the internal bus clock. Clock A and B can be programmed to run at 1, 1/2, and so forth down to, 1/128 times the internal bus clock. Clock SA and SB use clock A and B respectively as an input and divides it further with a reloadable counter. The rates available for clock SA and SB are programmable to run at clock A and B divided by 2, 4, and so forth up to, 512. Each PWM channel has the capability of selecting one of two clocks: either the prescaled clock (clock A or B) or the scaled clock (clock SA or SB).

For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can thus be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.
Consider this question about the PWM module.

Correct!
That is the width buffer. At the beginning of each period, the value of the width register is loaded into the width buffer, which feeds the comparator.
Another module in the MCF5282 is the programmable interrupt timer (PIT). PITs are also provided in the MCF521x, MCF528x, MCF7275/4, MCF523x, MCF5271/0 devices. There are four PITs, each of which generates interrupts at precise, regular intervals.

Each PIT module is based on a 16-bit free-running down counter.

When the count reaches $0000$, a timeout flag is set, which can trigger an interrupt if the PIT interrupt is enabled. The PIT timeout period is defined as the time it takes for the free-running down counter to reach zero.

The formula for this timeout period is shown here. It is: 
$$ \text{timeout period} = \text{PRE}[3:0] \times (\text{PM}[15:0] + 1) \times \frac{\text{fsys}}{2}.$$ 

The counter is initialized to whatever is programmed into the 16-bit modulus register, thereby giving the user full control over the timeout period. This timeout value, given in terms of system clock cycles, is a function of the prescaler and the modulus value, giving a maximum PIT timeout of two to the 31 system clock cycles. The Count register may be read at any time to check its current value.

A common application of the PIT is to bring the device out of a low-power state at regular intervals. However, the PITs are disabled in STOP mode, thus they cannot be used to wake the part up from STOP mode.
The programmable interrupt timer (PIT) is a 16-bit timer that provides precise interrupts at regular intervals with minimal processor intervention. The timer can either count down from the value written in the modulus register, or it can be a free-running down-counter. This device has four programmable interrupt timers, PIT1-PIT4.
Question

True or false? The PIT counter can be either pre-loaded with a user-programmed value in the modulus register, or it can function as a free-running counter. Click the correct answer and then click Done.

A) True
B) False

Consider this question about the ColdFire family of products.

Correct!
The PIT counter can be either pre-loaded with a user-programmed value in the modulus register, or it can function as a free-running counter.
In this module, you learned about the Fast ADC which is an easy to use 12 Bit ADC with a high accuracy.

The QADC is a 10 Bit ADC with the ability to queue up to 16 conversions for a faster conversion time.

The multiple timer modules offer a flexible and extensive way to time events, generate interrupts, and in the case of the DMA timers, generate DMA requests. They offer a varying range of resolution for added flexibility and operate with little processor intervention.

The PWM module on the MCF5272 generates a synchronous series of pulses having programmable duty cycle. The PWM module on the MCF5213 generates a synchronous series of pulses having programmable period and duty cycle with added support for programmable clock sources.