Enabling flexible multi-standard base-station designs

MAPLE Hardware Accelerator and SC3850 DSP Core

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MSC8156 multicore digital signal processor (DSP) product using the SC3850 DSP cores and MAPLE-B accelerators

MAPLE-B accelerators
  • Programmable accelerators concept
  • Programming model
  • Accelerated functions and standards compliance

SC3850 DSP built on StarCore® technology
  • Architecture overview
  • Performance
  • L1 and L2 cache sub-system

Summary
MSC8156E 45 nm Six-Core DSP

- Six SC3850 Cores Subsystems (up to 6 GHz/48 GMACs) each with:
  - SC3850 DSP core at up to 1 GHz (8 GMACs 16b or 8b)
  - 512 KB unified L2 cache / M2 memory
  - 32 KB I-cache, 32 KB D-cache, WBB, WTB, MMU, PIC
- Internal/External Memories/Caches
  - 1056 KB M3 shared memory (SRAM)
  - Two DDR 2/3 64-bit SDRAM interfaces at up to 800 MHz
- CLASS – Chip-Level Arbitration and Switching Fabric
  - Non-Blocking, fully pipelined, low latency
  - Full fabric 12 masters to eight slaves, up to 512 Gbps throughput
- MAPLE-B – Baseband Accelerator
  - Turbo/Viterbi decoder up to 200/115 Mbps
  - supporting: 3G-LTE, 802.16, 3G, CDMA2K standards
  - FFT and DFT accelerators up to 280 and 175 Msps
  - Multi-standard CRC check and insertion
- Security Engine (Talitos 3.1)
  - Data and code protection (AES, SHA, Kasumi, SNOW3G)
- High Speed Interconnects
  - Dual 4x/1x Serial RapidIO® at 1.25/2.5/3.125 Gbaud
  - PCI Express® 4x/1x
- Dual RISC QUICCEngine™ Technology Supporting
  - Dual SGMI/RGMII Gigabit Ethernet ports
  - Eth. L1 Protocols, Talitos control and Serial RapidIO offload
- TDM Highway
  - 1024 ch., 400Mbps, divided into four ports of 256
- DMA Engine
  - 16 bi-directional channels w/ external req/ack
- Eight Hardware Semaphores
- Other Peripheral Interfaces
  - SPI, UART, I²C, 32 GPIO, 16 Timers, 96 KB boot ROM, JTAG/SAP, 8 WDT
- Technology
  - 45 nm SOI, 1V core, 2.5, 1.8/1.5V I/O
  - FCBPGA (29x29) 1mm pitch, RoHS

Now Sampling
Multi-Accelerator-Platform for Baseband

MAPLE-B
MAPLE-B Accelerator Overview

► Software friendly buffer descriptor based handshake and task assignment with minimal overhead on DSP cores for control

► Highly flexible and programmable Turbo and Viterbi decoder supporting various configurable decoding parameters
  • High throughput Turbo decoding for low latency and advanced antenna systems
  • Low latency multi-standard Viterbi decoding for data/control channels
  • Multi-standard capable: UMTS, CDMA2K, WiMAX and Long Term Evolution (LTE)
  • Flexible rate de-matching schemes for multiple standards, accelerating HARQ functionality

► Flexible and advanced FFT/DFT acceleration:
  • FFT/iFFT for sizes 128, 256, 512, 1024, 2048 points
  • DFT/iDFT for LTE sizes

► High speed CRC calculation/check accelerator for:
  • LTE code and transport block in UL and DL
  • WiMAX PHY Burst CRC in UL and DL
MAPLE-B Block Diagram

PSIF : Programmable System Interface
TVPE: Turbo/Viterbi Processing Engine
FFTPE: FFT Processing Engine
DFTPE: DFT Processing Engine

BD’s write/read and debug by DSP core/host
Data write/read by MAPLE
64b 450 MHz
2x 64b 450 MHz

Interrupts
PSIF config

Arbitration and switching

PSIF
MAG2DRAM
System DMA Engine
Local DMA/ CRC PE x2
IRAM 16kB
RISC 0 Core
RISC 1 Core
IRAM 16kB
PIC
CE Slave

Routing and Config
I/O Data Buffer
Twiddles Memory
SBIF

Arbitration and switching

DRAM
DATA SRAM
16kB
DATA SRAM
16kB

SIF
TVPE
SIF

EXT MEM
CD; NII, HO MEM
EXTL
CDL
NIIL HOL

VRE DRE0 DRE1 DRE2 DRE3
CTL

I/O Data Buffer
Routing and Config
Radix 2 Cells
Radix 4 Cells
Radix 8 Cells
Routing and Config
Radix 2 Cells
Radix 3 Cells
Radix 4 Cells
Radix 5 Cells

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MAPLE-B Block Diagram

Programmable System Interface Based on RISC Engines:

- Flexibility and standards adaption
- Buffer descriptors parsing and system handshake
- DMA capabilities, and high system BW support
- Low level task control and split
- CRC acceleration

PSIF: Programmable System Interface
TVPE: Turbo/Viterbi Processing Engine
FFTPE: FFT Processing Engine
DFTPE: DFT Processing Engine

SDRAM 16kB
SRAM 16kB
SRAM 16kB

Routing and Config
I/O Data
Buffer
Routing and Config
Routing and Config
Twiddles
Memory
Twiddles
Memory
SBIF
SBIF

CDL
CD, NII, HO MEM

EXTL
EXT MEM

VRE DRE0 DRE1 DRE2 DRE3

CTL

BD’s write/read and debug by DSP core/host
Data write/read by MAPLE

Interrupts
PSIF config

64b 450 MHz
2x 64b 450 MHz

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- CRC acceleration

Turbo-Viterbi Processing Element:
- SIMD parallelism
- Novel heuristics and Radix 4 architecture
- >10x the throughput of existent industry/competitor solutions
- Multi-standard capable:
  - binary/duo,
  - tail-bit/trellis termination,
  - configurable interleaver

PSIF: Programmable System Interface
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  - binary/duo,
  - tail-bit/trellis termination,
  - configurable interleaver

FFT/IFFT and DFT/iDFT Processing Elements:
- High throughput engines
- Multi-Radix implementation
- Novel precision handling techniques
- Power, area, performance optimized vs. software implementations

PSIF : Programmable System Interface
TVPE : Turbo/Viterbi Processing Engine
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MAPLE-B Block Diagram

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BD’s write/read and debug by DSP core/host
Data write/read by MAPLE

64b 450 MHz
2x 64b 450 MHz

Interrupts
PSIF config

Arbitration and switching
PSIF overview

- RISC based programmable system interface
- Hardware scheduler
- Firmware based buffer descriptors parsing and arbitration
- DMA and DMA control for input/output data via two master interfaces
- Direct access for BD’s placement by DSP cores or other hosts via fast slave interface
- Local DMA for CRC acceleration and future extensions
- Programmable interrupt controller
- Standard SRAM* interface to PE’s (TVPE, DFTPE, FFTPE)
- Low level control and configuration of PE’s
- Emulate system behavior of “Yet Another Slave DSP Core”
MAPLE-B Programming Model Overview

► Buffer Descriptor (BD) based programming model:
  • Up to eight high-priority BD rings and eight low-priority BD rings per each processing element for multiple master support – multicore awareness
  • MAPLE-B round robin with priority arbitration between jobs
  • 12 KB MAPLE-B internal memory dedicated for BD rings in internal memory
  • TaskID for every job in BD for debug/tracking purposes

► Minimal overhead for DSP core
  • MAPLE-B reads input data using its embedded DMA from any system memory location: M2/L2/M3/DDR
  • MAPLE-B writes results to any system memory location: M2/L2/M3/DDR
  • Interrupts and/or BD polling command done indication to DSP cores
  • Supports direct Serial RapidIO® door-bell generation for job completion indication to external host sharing or controlling certain MAPLE BD rings
Ring Descriptors and Buffer Descriptor

- Located inside MAPLE
- Multiple priorities
- Small handling fee for RISC processors
Ring Descriptors and Buffer Descriptor

Up to 12 KB Total
FFTPE highlights

- High throughput, low power FFT/iFFT transform processing element
- Build from Radix2, Radix4 and Radix8 elements
- Single, 64-bit PSIF interface for control and data
- Support 128, 256, 512, 1024 and 2048 points transforms
- 32-bit (16I, 16Q) input and output data
- Internal twiddles ROM memory
- Advanced scaling methods including:
  - User defined down scaling per stage of 0-4 bits
  - Adaptive scaling (block-floating emulation) with overall scaling option
- Guard bands and DC carrier insertion for iFFT optimization
- Job (BD) repeat option for reduced configuration and increased throughput with adjacent I/O data structures
DFTPE highlights

- High throughput, low power FFT/iFFT, DFT/iDFT transform processing element
- Build from Radix2, Radix3, Radix4 and Radix5 elements
- Single, 64-bit PSIF interface for control and data
- Support 128, 256, 512, 1024 points FFT/iFFT transforms
- Support 3G LTE standard DFT/iDFT transforms from 12 to 1200 and 1536 points
- 32-bit (16I, 16Q) input and output data
- Internal twiddles ROM memory
- Advanced scaling methods including:
  - User defined down scaling per stage of 0-4 bits
  - Adaptive scaling (block-floating emulation) with overall scaling option
- Guard bands and DC carrier insertion for iFFT optimization
- Job (BD) repeat option for reduced configuration and increased throughput with adjacent I/O data structures
TVPE highlights

- High throughput, low power Turbo or Viterbi decoding
- Multi-standard, multi-algorithm support via:
  - Binary and duo binary decoder
  - Tail-bit and zero tail trellis termination support
  - MaxLogMap and HybridLinearLogMap
  - Multi-iteration Viterbi decoding WAVA*
- Dual, 64 bit PSIF interface for control and data
- Radix4, NII-X architecture
- 8-bit soft LLR inputs and soft/hard outputs
- Rate-de-matching support for LTE, WCDMA, WiMAX
- Periodic de-puncturing for CDMA2K and Viterbi
- Various Input data structures to support trade-off between DSP core pre-processing MIPS and Turbo decoding throughput
- Support for APQ and CRC early stopping criterias
### WiMAX Systems

<table>
<thead>
<tr>
<th>Feature</th>
<th>MAPLE-B (MSC8156)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Turbo decoding</strong></td>
<td>&gt; 195 Mbps (6 iterations)</td>
</tr>
<tr>
<td>Optional support for sub-block de-interleaving</td>
<td></td>
</tr>
<tr>
<td><strong>Viterbi decoding</strong></td>
<td>&gt; 100 Mbps (tail-biting multi-iteration)</td>
</tr>
<tr>
<td>Optional support for periodic de-puncturing</td>
<td></td>
</tr>
<tr>
<td><strong>FFT/IFFT</strong></td>
<td>&gt; 350 Msps using 2 units (FFTPE, DFTPE)</td>
</tr>
<tr>
<td>Optional support for guard bands insertion</td>
<td></td>
</tr>
<tr>
<td><strong>CRC</strong></td>
<td>&gt; 10 Gbps , CRC16 (PDU)</td>
</tr>
<tr>
<td>insertion for DL and check for UL</td>
<td></td>
</tr>
</tbody>
</table>

### 3GLTE FDD/TDD Systems

<table>
<thead>
<tr>
<th>Feature</th>
<th>MAPLE-B (MSC8156)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Turbo decoding</strong></td>
<td>&gt; 200 Mbps (6 iterations)</td>
</tr>
<tr>
<td>Optional support for sub-block de-interleaving</td>
<td></td>
</tr>
<tr>
<td><strong>Viterbi decoding</strong></td>
<td>&gt; 100 Mbps (tail-biting multi-iteration)</td>
</tr>
<tr>
<td>Optional support for periodic de-puncturing</td>
<td></td>
</tr>
<tr>
<td><strong>FFT/IFFT/DFT/IDFT</strong></td>
<td>&gt; 280 Msps FFT using FFTPE</td>
</tr>
<tr>
<td>Optional support for guard bands insertion</td>
<td>&gt; 175 Msps DFT using DFTPE</td>
</tr>
<tr>
<td><strong>CRC</strong></td>
<td>&gt; 10 Gbps , CRC24A, CRC24B</td>
</tr>
<tr>
<td>insertion for downlink and check for uplink</td>
<td></td>
</tr>
</tbody>
</table>

### UMTS – WCDMA, HSPA+

<table>
<thead>
<tr>
<th>Feature</th>
<th>MAPLE-B (MSC8156)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Turbo decoding</strong></td>
<td>&gt; 165 Mbps (6 iterations)</td>
</tr>
<tr>
<td><strong>Viterbi decoding</strong></td>
<td>&gt; 115 Mbps (zero tail, K=9)</td>
</tr>
<tr>
<td>Optional support for periodic de-puncturing</td>
<td></td>
</tr>
<tr>
<td><strong>FFT/IFFT</strong></td>
<td>&gt; 350 Msps FFT using FFTPE and DFTPE</td>
</tr>
<tr>
<td><strong>CRC</strong></td>
<td>&gt; 10 Gbps , CRC24</td>
</tr>
<tr>
<td>insertion for DL and check for UL</td>
<td></td>
</tr>
</tbody>
</table>
3G LTE PDSCH/DLSCH Acceleration using MAPLE-B

Example
Advanced programming model

- Buffer descriptors based job assignment
- Multiple buffer descriptor rings for multicore system
- System optimization via:
  - Multi job assignment, advanced alignment
  - Flexible interrupt assignment to any DSP core
  - Embedded DMA with direct access to L2 cache or M2/M3/DDR
  - Full off-load of accelerators programming and control

High capacity processing elements (Coprocessors)

- Optimized for low latency, high throughput system performance
- Local to DSP FFT and DFT acceleration for:
  - OFDMA/SC-FDMA processing
  - Ranging/RACH acceleration
  - Frequency domain processing acceleration for HSPA
- 6144-bit LTE code block: ~40 usec decoding latency
SC3850 DSP Core and Subsystem
StarCore® Architecture Roadmap

- Enhanced control code support
- Dual MAC

- MMU support
- Additional ASI
- Enhanced video
- Dynamic branch prediction
- Additional SIMD instructions

- Memory protection
- Prediction

- Up to 6-Issue VLIW Architecture
- VLES
- SIMD

MSC8101/3, MSC8122/26/12/13, Wireless subscriber

V2

8144/E/EC

V7 products...

V6 SC3850 products...

V5 815x SC3400 products...

V3 MXC (2.5G, 3G, 3.5G)

MSC8101/3, MSC8122/26/12/13, Wireless subscriber

V2 SC1000 products...

SC140e products...

SC3400 products...

SC3850 products...
# StarCore® Feature Evolution

<table>
<thead>
<tr>
<th></th>
<th>SC140 (V2)</th>
<th>SC140e (V3)</th>
<th>SC3400 (V5)</th>
<th>SC3850 (V6)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Shared features</strong></td>
<td>6 issue, statically scheduled VLES model: 4 DALU + 2 AGU</td>
<td>128-bit instruction fetch, 2x64 data ports (3 memory accesses per cycle)</td>
<td>Backward binary compatibility between all family members (16-bit basic inst. set)</td>
<td></td>
</tr>
<tr>
<td><strong>Pipeline Stages</strong></td>
<td>5 (600 MHz @90G)</td>
<td>5 (250 MHz @90LP)</td>
<td>12 (1 Ghz @90SOI)</td>
<td>12 (1 Ghz @45SOI)</td>
</tr>
<tr>
<td><strong>Instructions</strong></td>
<td>Baseline</td>
<td>Minor additions</td>
<td>Video, SIMD2</td>
<td>Control ISA, Dual MPY Cache instructions</td>
</tr>
<tr>
<td><strong>Precise exceptions</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Privilege levels</strong></td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Micro-arch. Features</strong></td>
<td>1 VLES speculation</td>
<td>1 VLES speculation</td>
<td><strong>BTB</strong>, 4 VLES spec., 1 COF deep</td>
<td><strong>BTB</strong>, 4 VLES spec., nested COF</td>
</tr>
<tr>
<td><strong>Platform</strong></td>
<td>M1 + L1 Icache</td>
<td>MMU, L1 I/D cache</td>
<td>L1, MMU, M2</td>
<td>L1, MMU, L2/M2</td>
</tr>
</tbody>
</table>
SC3850 DSP Core Key Architectural Features

► Statically scheduled VLIW
  • VLES model – Variable Length Execution Set
  • 6-issue: 4 DALU + 2 AGU + loop dispatched per cycle

► Very high numerical throughput
  • Two 16x16 multipliers per Data ALU, eight total
  • Support for extended precision and complex multiplication
  • Four zero-overhead hardware loops
  • Application-specific instructions: FFT, complex algebra and more
  • 2x64-bit load/stores per cycle; Multivariable access to/from multiple registers with pack/unpack
  • Compact instructions perform multiple intrinsic functions (e.g. MAC, complex multiply, scale/saturate/round as part of the store)

► Very good support for control code
  • Dynamic branch prediction (BTB), speculative execution
  • Fully predicated instruction set

► Good OS support
  • Precise exceptions for MMU support, including during hardware loops
  • Dual stack pointer management in hardware
The StarCore core consists of the following main units:

- Data arithmetic logic unit (DALU) that contains four instances of an arithmetic logic unit (ALU) and a data register file
- Address generation unit (AGU) that contains two address arithmetic units (AAU) and an address register file
- Program control unit (PCU)
Dual Multiply ISA

Single MAC operation (SC140/SC3400)

\[ \text{mac } Da,Db,Dn \]
\[ Dn + (Da.H \times Db.H) \rightarrow Dn \]

Dual MAC – SIMD2 MAC (SC3850)

\[ \text{mac2 } Da,Db,Dn \]
\[ Dn.WH + (Da.H \times Db.H) \rightarrow Dn.WH \]
\[ Dn.WL + (Da.L \times Db.L) \rightarrow Dn.WL \]

Dual MAC – double throughput MAC (SC3850)

\[ \text{dmac } Da,Db,Dn \]
\[ Dn + (Da.H \times Db.H) + (Da.L \times Db.L) \rightarrow Dn \]
SC3850 DSP Core Data Processing Throughput

- DALU calculations are based on 40-bit registers
- The two multipliers of each ALU can be used in various ways:
  - SIMD2 or dot-product multiplication
  - Complex multiplication
  - Extended precision multiplication (16x32, 32x32)

<table>
<thead>
<tr>
<th>Operation</th>
<th>Precision</th>
<th>Operations per cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Multiply</td>
<td>16x16</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>16x32</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>32x32</td>
<td>2</td>
</tr>
<tr>
<td>Complex Multiply</td>
<td>16x16</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>16x32</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Kernel</th>
<th>SC3850</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real block FIR 16x16</td>
<td>NT/8</td>
</tr>
<tr>
<td>Complex FIR 16x16</td>
<td>NT/2</td>
</tr>
<tr>
<td>Dot Product 16x16</td>
<td>N/4</td>
</tr>
</tbody>
</table>

N: samples
T: Taps
SC3850 DSP Sub-System Features – Caches

► Caches optimized to give best performance reducing TTM

► L1 caches
  • Instructions and data caches both: 32 KB, 8 way
    ▪ Data cache supports write back allocate and write through policies
  • Advanced automatic pre-fetching:
    ▪ Line pre-fetch with critical word first and next line pre-fetch
  • Software-controlled pre-fetching with cache control instructions

► L2/M2 memory system
  • 512 KB, configurable as L2 cache or M2 SRAM in 64 KB banks
  • M2 SRAM accessible by DMA
  • L2 cache: 8-ways, unified program and data
  • Programmable cache way partitioning according to address ranges
  • Low latency to the core (10-12 cycles)
  • Software-triggered DMA like pre-fetch channels operate in the background
  • DMA based “stashing” to DDRz
L2 cache software pre-fetch (SWPF), L1 DFETCH and PFETCH

- L2 SWPF of code2 and/or data2
- PFETCH (code2) and/or DFETCH (data2)
- Task1(code1,data1) Execution

- L2 SWPF of code3 and/or data3
- PFETCH (code3) and/or DFETCH (data3)
- Task2(code2,data2) Execution

- L2 SWPF of code3 and/or data3
- PFETCH (code3) and/or DFETCH (data3)
- Task3(code3,data3) Execution

Legend:
- Inline fetch into L1 caches
- Background fetch into L2 caches
- In reality: Smaller and more frequent

Fetch “SW Pipeline”

Task1(code1,data1) Execution
Task2(code2,data2) Execution
Task3(code3,data3) Execution

time
Cache vs. DMA Model in SC3850 DSP Subsystem

**DMA SW Model**
- All in M2
- Highest performance
- High effort
- Generate higher bus load
- Expert mode – higher TTM

**Mixed Model**
- L2 is partly M2

**Scheduled Cache SW model**
- 100% L2 + SWPF
- Critical code/data in M2
- Consider using L2 cache partitioning
- High performance
- Moderate effort

**Cache SW model**
- 100% L2
- All in DDR/M3
- Good performance
- Low effort

Effort
SC3850 DSP Sub-System Features – Benefits of the MMU

► Memory protection, translation and precise exceptions
► Simpler, abstract software model - not SoC specific
► Good support for multicore devices
  • Code written once, unaware of the core it will actually run on
  • Specific memory allocated per channel instance, on a specific core
► Easier debug, faster time to market
  • MMU errors quickly catch when a task accesses out of bounds
  • Virtual addressing allows simpler code re-use
► Better MTBF (Mean Time Between Errors)
  Channels are isolated from each other and from system code
  • System code and privileged registers protected in supervisor level
  • An errant task will not bring down the whole system
  • Precise exceptions serviced before the error executes, allowing recovery in some cases
SC3850 DSP Sub-System Features – Debug and Profile

**Debug:**
- Rich brakepoint capabilities
- Cache aware debug
- PC trace with task information
- Remote debug capability

**Profile:**
- Performance optimization using detailed core stall information
- Measuring RTOS and system overhead
- Profiling at a function level
- Constraint violation monitors
CodeWarrior™ Developer Studio is a highly integrated toolchain providing the most comprehensive support of Freescale DSPs built on StarCore® technology.

► Complete build and debug environment united in Eclipse IDE
► Robust platform for development
► Performance optimized StarCore DSP compiler
► Multicore capabilities in every component
  • SmartDSP OS, IDE, SA, debugger, simulator
CodeWarrior™ Development Studio for StarCore® v10.0
A complete development environment under Eclipse

► Eclipse IDE
  • Configuration Wizards
  • Plug-in architecture
  • Third party community

► StarCore Build Tools
  • v23 performance C/C++ compiler
  • New linker
    - Redesigned for usability
    - Available for beta testing
    - Old linker still included as default
      - New linker will become default in beta release

► Simulation
  • Functional and cycle accurate

► SmartDSP OS
  • Enhanced performance and networking
  • High speed data io via SmartDSP HEAT

► StarCore Debugger
  • Multicore and multi-DSP
  • MSC8144 and MSC8156 targets

► Trace and Profile
  • Trace data offload via Ethernet using SmartDSP HEAT technology
Summary

► SC3850 cores and sub-systems are optimized for baseband processing using advanced core architecture and high performance and flexible multi-level cache system

► MAPLE-B provides innovative hardware acceleration platform for baseband processing

► SC3850 DSP cores coupled with MAPLE-B acceleration in MSC8156 DSP processor provide unique combination of processing power and flexibility for current and future multi-standard base station designs
Thank you for attending this presentation. We’ll now take a few moments for the audience’s questions and then we’ll begin the question and answer session.