White Paper

Semiconductor Packaging Technologies
System-in-Package, Package-on-Package and Redistributed Chip Packaging: Progressing Toward 3G Radio-in-Package
Overview

As electronic devices do more in less space, so do their enabling technologies. Semiconductor packaging is no exception. Freescale has developed and shipped millions of integrated circuits as technologies have advanced in sophistication and shrunk in size. Now Freescale is introducing a new technology, redistributed chip packaging (RCP), which promises to increase speeds and reduce package sizes used in high-interconnect semiconductor devices such as those found in smartphones and multimedia players. This will enable manufacturers to create the small, sleek multifunction devices that their customers want—in a smaller, more cost-effective and highly integrated solution.

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1 Packaging Technology Overview

Packaging is the final step in the complex process of turning silicon into a useful semiconductor device. As such, it has a significant effect on the appearance and function of end-user devices, from computers to cell phones to embedded processors. As in most electronics, the trend is to make semiconductor devices smaller yet more powerful. This evolution can be traced through three types of packaging technologies: system-in-package (SiP), package-on-package (PoP) and a new Freescale packaging innovation called redistributed chip packaging (RCP).

All of these packaging technologies provide benefits not only to end device manufacturers, but also to consumers. Manufacturers gain the benefit of high levels of integration so that they can use increasingly sophisticated electronics without adding bulk. This integration also saves board space, so that more functionality—from cameras to multimedia players to 3G communications—can be packed into converged mobile devices, creating true form factor freedom. Consumers also see the benefit of smaller mobile devices with more features, such as smartphones, PDAs and portable media players.

While short-term packaging needs will be met by incremental improvements of current generations of technology, future packaging needs will require new technology to meet evolving engineering and market demands. Freescale’s approach to the evolution of packaging is driven by system cost and miniaturization. Each step along the path from SiP to PoP to RCP represents improvements in these two areas. Right now, each of these packages fit unique niches. For example, if size is most important, then stacked die will yield smaller packages. Moving into PoP may actually increase board space, but improves cost structure. RCP, with its potential to dramatically improve cost-effective systems to the size of a postage stamp, represents the best of both worlds.

1.1 SiP and PoP

System in package, as the name implies, is a technology that allows the placement of several integrated circuits in one package, providing a complete set of device electronics in a small area. This technique saves board space by integrating devices that were once spread farther apart on the circuit board. In 2000, Freescale produced the world’s first SiP module that stacked a baseband processor die with memory die in a single package.

Freescale’s approach to PoP packaging makes it a very flexible choice. The baseband and memory or other silicon are assembled, tested and yielded independently. Figure 1.1 illustrates how the top chip in this kind of package can be any ASIC, such as memory, an applications processor, a Bluetooth™ module or a camera module. Customers can change...
memory configuration as needed—even at the last minute. Because PoP is a Joint Electron Device Engineering Council (JEDEC) standard, Freescale can optimize designs for the bottom package for any component that meets those standards.

1.2 Standards-Based and Scalable

PoP enables standardization of I/O pin out configurations for easier implementation. Application-level integration, done during application assembly, is part of the set of services Freescale offers our customers. Software modifications are driven by customers’ applications, not by memory selection.

Scalability is another PoP advantage. Because PoP body sizes must conform to the JEDEC standard, customers can maintain control of memory procurement, enabling multiple suppliers, supplier qualifications and certifications and minimal inventory vulnerability. Customers can choose from various types, densities and combinations of memory such as Flash, PSRAM, SDRAM or DDR.

In terms of cost, the standards-based PoP approach limits exposure to memory market fluctuations, design choices and demand plans. PoP enables faster transitions to lower-cost memory and system solutions, including faster implementations of die shrinks, faster qualification cycles and the ability to add and maintain multiple sources. Memory and baseband are tested separately, creating higher final test yields. Because known good die (KGD) and its rigorous testing costs are not required, memory suppliers can save money. Another cost savings comes through standardized test equipment that can be used on a range of JDEC-compatible packages.

Although PoP is preferable in many cases, there are cost and complexity choices that may lead a customer to choose SiP. Freescale provides both packaging approaches for our customers.

1.3 Wire Bonding

SiP and PoP packages both use wire bonding for the die-package interface. Freescale has a history of innovation in wire bond technology. For example, Freescale was the first company to implement bond and probe over passivation and the first to implement bond over active for low-k (<90 nm) dielectrics. Both these die design techniques place active circuitry in previously unused areas beneath bond pads. Wire bonded devices that have high I/O counts also have high bond pad counts, which meant that a significant portion of the die could not be used for circuitry. Being able to use more space on the die allows smaller, denser die with higher levels of functionality. For 65-nanometer CMOS (complementary metal oxide semiconductor) manufacturing, for example, Freescale has enabled ultra-fine 40 - 38 micron wire bonding pitch.

Space efficiency and I/O density continued to increase with fine pitch dual in-line wire bond techniques (pioneered by Freescale) and the shrinking of bond pad pitch from 47 to 38 microns, for increased function and accessibility in a given die size.

2 RCP: The End of Wire Bond

While wire bonding is an important packaging technology, it has limitations. The wires take up valuable board space, no matter how tightly they can be compacted. Flip chip is a step in the direction of eliminating wire bonding. In the flip chip process, a die is connected face-down to a board or substrate using ball grid array (BGA) or other conductive bumps. This approach eliminates wire bonds, increases speeds and reduces size.

Freescale’s RCP technology takes flip chip a step further by eliminating package substrates altogether. This improves and increases die-package interconnect in a way that simply cannot be accomplished using today’s laminate substrates. Laminate substrate technology is paced by via escape and the routing trace width and pitch, both required to connect the wire bonds to the package interface pins. In this way the package I/O density is limited for a given body size. RCP allows the bond fingers to be effectively pulled into the die, creating a smaller package with higher I/O density.
Table 2.1 shows how the three technologies compare in terms of benchmarks.

<table>
<thead>
<tr>
<th></th>
<th>SI0</th>
<th>PoP</th>
<th>RCP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package/system cost</td>
<td>★</td>
<td>★</td>
<td>★</td>
</tr>
<tr>
<td>Package reliability</td>
<td>O</td>
<td>△</td>
<td>Data not available</td>
</tr>
<tr>
<td>Package footprint</td>
<td>O</td>
<td>△</td>
<td>★</td>
</tr>
<tr>
<td>PCB footprint</td>
<td>O</td>
<td>△</td>
<td>★</td>
</tr>
<tr>
<td>Integration density</td>
<td>O</td>
<td>△</td>
<td>★</td>
</tr>
<tr>
<td>Customer surface mount technology (SMT) assembly</td>
<td>O</td>
<td>△</td>
<td>★</td>
</tr>
<tr>
<td>Electrical performance</td>
<td>O</td>
<td>△</td>
<td>★</td>
</tr>
<tr>
<td>Thermal performance</td>
<td>△</td>
<td>△</td>
<td>★</td>
</tr>
<tr>
<td>Flexibility</td>
<td>★</td>
<td>O</td>
<td>★</td>
</tr>
<tr>
<td>Requires memory known good die (KGD)</td>
<td>Yes</td>
<td>Yes, for top package</td>
<td>No</td>
</tr>
</tbody>
</table>

- ★ Best
- △ OK
- O Good
- × Not good

2.1 Eliminating Substrates
RCP is an interconnect buildup technology, which means that the package is built around the die. Other packaging interconnection techniques insert a die directly onto a substrate using flip chip or wire bond techniques. The substrate performs the routing between the die and the rest of the electronics. RCP, on the other hand, eliminates the substrate altogether.

RCP technology reduces the size of high-pitch packages; it can reduce a given package by up to 50 percent. By eliminating the substrate and enabling large area batch processing, RCP lowers packaging costs, allowing it to compete with commodity BGA packaging solutions. RCP enables high-density pad array designs and provides significant design flexibility with improved noise, power distribution and thermal characteristics.

2.2 The Right Choice for Low K
Freescale’s CMOS manufacturing process enables superior conductivity with copper interconnects and ultra-low-k dielectric materials to further enable high performance. RCP is ideally suited for the low-k materials used in CMOS.

Low-k allows a dielectric material to be thinner, which is necessary as transistors are placed closer and closer together on smaller dies. In many packaging technologies, the plastic molding can shrink around the die as the plastic cures, placing stress on the dielectric material and, in some cases, actually changing the die’s functional behavior. As manufacturing processes shrink from 90 to 65 to 45 nanometers, these packaging concerns will become critical. RCP eliminates the cost associated with formulating exotic low-stress molding compounds and polyimide passivation processes; the dielectric material used in the buildup process places no stress on the surface of the die and therefore is inherently compatible with low-k.
3 Benefits of RCP

As an emerging technology, RCP may displace current packaging solutions in many applications. In some applications there will be cost and manufacturability tradeoffs that make SiP, PoP, WL-CSP, flip chip or other packages a better choice. In addition to offering RCP, Freescale plans to continue to support the wide infrastructure of wire bonded and other packaging technologies that we have enabled by shipping millions of ICs over the years.

As I/O and interconnect density increases, the benefits of RCP rise exponentially. The only limitations on the use of RCP are I/O density, BGA array pitch, and the die size. This means that RCP packages can be made very small and very integrated, enabling innovations such as Freescale’s radio in package (RiP). RiP could, for example, replace the electronics in an entire cell phone with one package. This could produce new form factors such as a self-contained headset phone that does not need to connect to a handset.

As illustrated in Figure 3.1, the RCP system integration process for RiP takes memory, RF and PA modules, baseband or applications processor and power management components and integrates them into a single package solution and format. All “sub-assemblies” are fully tested using traditional, non-integrated methodologies and using conventional lowest cost test (ATE) platforms.

Figure 3.1 RCP System Integration for RiP

3.1 Enabling the MXC Platform

RCP also enables Freescale’s Mobile eXtreme Convergence (MXC) platform. The MXC platforms feature a single core modem, a shared memory subsystem, radio frequency (RF), power amplifier (PA) and power management (PM) functions—and RCP enables the option of putting an entire 2.75G platform in a package format the size of a U.S. quarter coin (Figure 3.2). Communications baseband and applications processing technologies are integrated into the chip with a shared memory system and shared peripherals to reduce complexity, part count, size and overall system costs while enhancing multimedia and communications processing performance using conventional surface mount technology (SMT) component placement techniques.
Similarly, RCP is flexible enough to integrate even more complex systems solutions such as 3G platforms. By using the unique integration capabilities of RCP technology, the reduction of external peripheral components can be significant. In the design shown in Figure 3.3, the peripheral component reduction exceeded 60% when compared to the traditional motherboard and discrete component design. This design contains the baseband processor, power management, WCDMA transceiver, quad-band GSM transceiver and the memory. Further demonstration of the capabilities of the RCP technology is realized in this application by using memory packaged in standard, off-the-shelf MCP BGA packaging. This enables customers to source memory from their preferred suppliers, as well as alter the memory sizes to meet their specific application requirements.

![GSM-EDGE Radio-in-Package](image1)

![3G Radio-in-Package](image2)

In the MXC platform, RCP enables high levels of integration, extremely dense routing, and support for multiple technologies. RCP’s superior electrical qualities reduce the need for external peripheral components, which in turn reduces total component count and cost and board space.

RCP technology has the potential to make ICs smaller and more cost-effective, and enable a tremendous amount of system integration. With this new technology, Freescale continues its tradition of providing the flexibility to cut costs, innovate and differentiate, allowing manufacturers to have true form factor freedom and put sleek new technologies in consumers’ hands.
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