New Compact Model for Induced Gate Current Noise

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Abstract
Accurate compact modeling of induced gate noise is a prerequisite for RF CMOS circuit design. Existing models underestimate the induced gate noise for short-channel devices. In this paper, a new model is introduced, based on an improved Klaassen-Prins approach, which accurately accounts for velocity saturation. The model accurately describes noise without fitting any additional parameters.

Introduction
Accurate compact modeling of noise is a prerequisite for RF CMOS circuit design. At the RF-frequencies used, besides the drain current thermal noise also the induced gate noise plays an important role. Over the years, several compact models for induced gate noise have been introduced [1–4]. Nevertheless, all of these models are based on the same Van der Ziel model [1], which is only valid in saturation. In addition, the Van der Ziel model is based on the Klaassen-Prins (KP) equation [5], which does not accurately account for velocity saturation [6]. As a result, the above models are inaccurate for short-channel devices, and more accurate modeling for induced gate noise is needed.

In a previous study [7,8], we modeled the induced gate noise by using channel segmentation, which automatically results in an accurate description of RF-noise. This accuracy is, however, obtained at the expense of simulation speed. In this paper, we introduce new compact equations for drain and induced gate noise based on surface potential $\psi_s$ and, as a result, valid in all operation regions. In contrast to existing models, the new model is based on a new improved Klaassen-Prins approach, which accurately accounts for velocity saturation and is therefore valid even for short-channel devices. Finally, the new compact model is verified on measurements from the 0.18$\mu$m and 0.12$\mu$m technology node.

$\psi_s$-Based Noise Modeling in KP-Approach
First, we investigate the accuracy of the conventional Klaassen-Prins approach [5], see Fig. 1. The drain current $I_D$ is calculated from (1), where an accurate velocity saturation expression (2) has been incorporated ($\mu = 2$) [9,10]. A thermal current noise source $i_v$ (3) and the resulting channel noise voltage $v$ are introduced in (1) to calculate the terminal noise current $i_D$, see (4a). Note that the noise in the velocity saturation term is neglected in the conventional KP-approach. Due to the capacitive coupling between channel and gate, the noise voltage $v$ will also induce a gate noise current $i_g$ given by (7). Using (4a) and (7), we can derive eqs (8)–(11) for the drain noise $S_{i_D}$, the induced gate noise $S_{i_g}$, and the correlation coefficient $c$, where $g_k$ and $L_c$ denote the channel conductance (5a) and channel length (6a), respectively. Eqs (8)–(11) can be approximated by the well-known Van der Ziel model (12) [1], which forms the basis of, e.g., the BSIM4-model [11], by limiting the result to the saturation region, using a threshold-voltage-based model, and neglecting the impact of velocity saturation.

In contrast, we derive explicit equations for the induced gate noise (9)–(11) in the framework of our $\psi_s$-based compact model, MOS Model 11 (MM11) [12], making the equations valid in all operation regions. This approach is an extension of our previous drain noise model [10]. In order to verify this new model, we compare it to a channel segmentation model which automatically includes an accurate description of induced gate noise [7,8]. As a first step, we simulate an ideal MOSFET without velocity saturation, see Fig. 2. In contrast to the Van der Ziel model, our $\psi_s$-based model gives an accurate description in all operation regions. Next, we simulate the same MOSFET, this time including velocity saturation, see Fig. 3. Again, our model (solid lines) can be interpreted as a more accurate version of the Van der Ziel model. The description of drain noise is accurate enough, keeping our previous results [10] still valid. However, the description of the induced gate noise and the correlation deviates considerably from the expected behaviour, due to the fact that the conventional KP-approach (4a) does not correctly account for the impact of velocity saturation.

Correct Incorporation of Velocity Saturation in Noise Model
Next, we derive an improved KP-approach given by (4b), where fluctuations in the velocity saturation term are also taken into account, compare (4a) and (4b). Using (4b), it can be shown that the same expressions (8)–(11) can be used for $S_{i_D}$, $S_{i_g}$ and $c$, where the corrected conductance $g_k$ and the corrected channel length $L_c$ are given by (5b) and (6b), respectively, which reduce to the conventional eqs (5a) and (6a) in the absence of velocity saturation. Under the appropriate linearizations, the improved approach can be solved in the $\psi_s$-framework. The improved model is also shown in Fig. 3 (dashed lines). In general, it gives an accurate description of all noise currents including induced gate noise.

The above noise model has been implemented in MM11, where the impact of series resistance and short-channel effects (CLM, DIBL, etc.) have been incorporated as well. To be able to use the compact model for RF-applications, we furthermore extend the model with a gate resistor and a bulk resistance network [7,8].
Experimental Results

Noise measurements were performed on 0.18μm and 0.12μm RF CMOS technologies. Compact model parameters were extracted from DC-measurements, and gate and bulk resistance values were determined from Y-parameter measurements. In Fig. 4, noise results are shown for a L = 0.5μm MOSFET. The new model based on the improved KP-approach is in excellent agreement with the data without any additional noise parameter fitting. The Van der Ziel model, on the other hand, leads to a considerable error in the gate noise. Noise results for various channel lengths L are shown in Fig. 5. Our new model gives accurate results over all bias conditions and channel lengths. Using the Van der Ziel model leads to an underestimation of gate noise (up to 40%), particularly for intermediate L where velocity saturation is important. For short-channel devices, the differences between the two models are obscured due to the dominant impact of gate resistance, see Fig. 6. In future CMOS technologies where metal gates will be used, however, the gate resistance will be less dominant and the induced gate noise may dominate S_{g_{n}} even for short-channel devices.

Conclusions

Existing models, such as BSIM4, are based on the Van der Ziel model and underestimate the induced gate noise for short-channel devices. A new induced gate noise model has been developed suitable for compact MOS models. It is based on ψ_n-formulations and thus valid in all operation regions, but it can also be derived for V_T-based models. In contrast to existing models, the model is based on an improved Klaassen-Prins approach, which accurately accounts for velocity saturation. This approach hardly affects drain noise, but considerably changes the induced gate noise. Our model accurately describes noise data for all investigated devices without introduction of model parameters to fit the data.

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References

Figure 2: (a) Drain current spectral density $S_{id}$, (b) gate current spectral density $S_{ig}$, and (c) imaginary part of correlation coefficient $c$ as a function of gate bias $V_{GS}$ for an ideal (short-channel) MOSFET without velocity saturation (i.e., $v_{sat} \to \infty$). Symbols represent simulations with segmentation model, solid lines represent new ($\psi_s$-based) noise model and dotted lines represent Van der Ziel model (12). (NMOS, $W/L = 2\,\mu$m/0.1\,mm, $t_{ox} = 1.7$nm, $V_{DS} = 1$V, $f = 5.2$GHz)

Figure 3: (a) Drain current spectral density $S_{id}$, (b) gate current spectral density $S_{ig}$, and (c) imaginary part of correlation coefficient $c$ as a function of gate bias $V_{GS}$ for an ideal (short-channel) MOSFET with velocity saturation (i.e., $v_{sat} = 10^5$ms). Symbols represent simulations with segmentation model, solid lines represent model based on the conventional KP-approach (4a), dashed lines represent model based on the improved KP-approach (4b), and dotted lines represent Van der Ziel model (12). (NMOS, $W/L = 2\,\mu$m/0.1\,mm, $t_{ox} = 1.7$nm, $V_{DS} = 1$V, $f = 5.2$GHz)
Figure 4: (a) Drain and gate current noise versus gate-source bias and (b) versus drain-source bias, and (c) correlation coefficient \( c \) versus gate-source bias for an \( L = 0.5 \mu m \) n-channel device in 0.18\( \mu m \) CMOS technology. Symbols denote measurements, dashed lines denote the Van der Ziel model (12), and solid lines denote the new model based on the improved KP-approach (4b)–(6b). The new model gives an accurate description of all noise results, whereas the Van der Ziel model leads to a considerable underestimation of induced gate noise (up to 40%). The measured real part of \( c \) is slightly negative due to non-quasi-static effects, which are not taken into account in this model.

Figure 5: (a) Drain current noise and (b) gate current noise versus gate-source bias for \( n \)-channel devices with different channel length \( L \). Symbols denote measurements, dashed lines denote Van der Ziel model (12), and solid lines denote new model based on the improved KP-approach (4b)–(6b). The new model gives accurate results for all channel lengths. (\( f = 5 \)GHz and \( V_{DS} = 1.0 \)V for \( L \leq 0.18 \mu m \), \( f = 2.5 \)GHz and \( V_{DS} = 1.8 \)V for \( L \geq 0.5 \mu m \)).

Figure 6: Contributions to the modeled gate current noise for \( L = 0.13 \mu m \) n-channel device, see Fig. 5 (\( f = 5 \)GHz, \( V_{GS} = 0.85 \)V, \( V_{DS} = 1.0 \)V). Noise from the gate resistance dominates, and can only be partly reduced by changing the MOSFET layout [7,8].