1 MOS Model 11, level 1100
1.1 Introduction

General Remarks

MOS Model 11 (MM11, level 1100) is a new compact MOSFET model, intended for digital, analogue and RF circuit simulation in modern and future CMOS technologies. MM11 is the successor of MOS Model 9, it was especially developed to give not only an accurate description of currents and charges and their first-order derivatives (i.e. transconductance, conductance, capacitances), but also of the higher-order derivatives, resulting in an accurate description of electrical distortion behaviour [1]. The latter is especially important for analog and RF circuit design. The model furthermore gives an accurate description of the noise behaviour of MOSFETs.

MOS Model 11 gives a complete description of all transistor-action related quantities: nodal currents, nodal charges and noise-power spectral densities. The equations describing these quantities are based on surface-potential formulations, resulting in equations valid over all operation regions (i.e. accumulation, depletion and inversion). Although in general the surface potential is implicitly related to the terminal voltages and has to be calculated iteratively, in MM11 it has been approximated by an explicit expression [2]. Additionally, in order for the model to be valid for modern and future MOS devices, several important physical effects have been included in the model: mobility reduction, bias-dependent series-resistance, velocity saturation, drain-induced barrier lowering, static feedback, channel length modulation, self-heating, weak-avalanche (or impact ionization), gate current due to tunnelling, poldepletion, quantum-mechanical effects on charges and bias-dependent overlap capacitances.

MOS Model 11 only provides a model for the intrinsic transistor and the gate/source- and gate/drain overlap regions. Junction charges, junction leakage currents and interconnect capacitances are not included. They are covered by separate models, which are not part of this documentation.

MOS Model 11, level 1100 has been superseded by level 1101 and level 1102.

Structural Elements of Model 11

The structure of MOS Model 11 is the same as the structure of MOS Model 9. The model is separable into a number of relatively independent parts, namely:

- Model embedding

It is convenient to use one single model for both n- and p-channel devices. For this reason, any p-channel device and its bias conditions are mapped onto those of an equivalent n-channel transistor. This mapping comprises a number of sign changes. Also, the model describes a symmetrical device, i.e. the source and drain nodes can be interchanged without changing the electrical properties. The assignment of source and drain to the channel nodes is based on the
voltages of these nodes: for an n-channel transistor the node at the highest potential is called drain. In a circuit simulator the nodes are denoted by their network numbers, based on the circuit configuration. Again, a transformation is necessary involving a number of sign changes, including the directional noise-current sources.

• Preprocessing

The complete set of all the parameters, as they occur in the equations for the various electrical quantities, is denoted as the set of actual parameters, usually called the "miniset". Each of these actual parameters can be determined by purely electrical measurements. Since most of these parameters scale with geometry and temperature the process as a whole is characterized by an enlarged set of parameters, which is denoted as the set of reference and scaling parameters, usually called the "maxiset". This set of parameters contains most of the actual parameters for a reference device, a large set of sensitivity coefficients and the reference conditions. From this, the actual parameters for an arbitrary transistor under non-reference conditions are obtained by applying a set of transformation rules to the reference parameters. The transformation rules describe the dependencies of the actual parameters on the length, width, and temperature. This procedure is called preprocessing, as it is normally done only once, prior to the actual electrical simulation.

• Clipping

For very uncommon geometries or temperatures, the preprocessing rules may generate parameters that are outside a physically realistic range or that may create difficulties in the numerical evaluation of the model, for example division by zero. In order to prevent this, all parameters are limited to a pre-specified range directly after the preprocessing. This procedure is called clipping.

• Current equations

These are all expressions needed to obtain the DC nodal currents as a function of the bias conditions. They are segmentable in equations for the channel current, the gate tunnelling current and the avalanche current.

Charge equations

These are all the equations that are used to calculate both the intrinsic and extrinsic charge quantities, which are assigned to the nodes.

• Noise equations

The total noise output of a transistor consists of a thermal- and a flicker noise part, which create fluctuations in the channel current. Owing to the capacitive coupling between gate and
channel region, current fluctuations in the gate current are induced as well, which is referred to as induced gate noise.
1.2 Physics

1.2.1 Comments and Physical Background

In this section some physical background on the current, charge and noise description of MOS Model 11 will be given. For the full details of the physical background of the drain-source channel current equations the reader is referred to [1], [2], [4] - [6]. The gate current, charge and noise equations have been newly developed and their physical background will be discussed in a future report. All equations referred to are to be found in section 1.2.2

Comments on Current Equations

Conventional MOS models such as MOS Model 9 and BSIM4 are threshold-voltage-based models, which make use of approximate expressions of the drain-source channel current $I_{DS}$ in the weak-inversion region (i.e. subthreshold) and in the strong-inversion region (i.e. well above threshold). These approximate equations are tied together using a mathematical smoothing function, resulting in neither a physical nor an accurate description of $I_{DS}$ in the moderate inversion region (i.e. around threshold). With the constant downscaling of supply voltage the moderate inversion region becomes more and more important, and an accurate description of this region is thus essential.

A more accurate type of model is the surface-potential-based model, where the channel current $I_{DS}$ is split up in a drift ($I_{drift}$) and a diffusion ($I_{diff}$) component, which are a function of the gate bias $V_{GB}$ and the surface potential at the source ($\psi_{s0}$) and the drain ($\psi_{sL}$) side. In this way $I_{DS}$ can be accurately described using one equation for all operating regions (i.e. weak, moderate and strong-inversion). MOS Model 11 is a surface-potential-based model.

Surface Potential

The surface potential $\psi_s$ is defined as the electrostatic potential at the gate oxide/substrate interface with respect to the neutral bulk (due to the band bending, see Figure 1a). For an n-MOS transistor with uniform doping concentration it can be calculated from the following implicit relation:
where \( V \) is the quasi-Fermi potential, which ranges from \( V_{SB} \) at the source side to \( V_{DB} \) at the drain side. The parameter \( m_0 \) has been added to model the non-ideal subthreshold behaviour of short-channel transistors\(^1\), and \( \psi_p \) is the potential drop in the polysilicon gate material due to the poly-depletion effect. The latter is given by\(^2\):

\[
\psi_p = \begin{cases} 
0 & V_{GB} \leq V_{FB} \\
\left(V_{GB} - V_{FB} - \psi_s + k_p^2 \cdot \frac{k_p}{2}\right)^2 & V_{GB} > V_{FB}
\end{cases}
\]

In Figure 1b the surface potential is shown as a function of gate bias for a typical n-type MOS device. The surface potential \( \psi_s \) is implicitly related to the gate bias \( V_{GB} \) and the quasi-Fermi potential \( V \), and cannot be calculated analytically. It can only be calculated using an iterative solution, which in general is computation-time consuming. In MOS Model 11 an explicit approximation of the surface potential is used, which has partly been treated in [2]. In the inversion region \( V_{GB} > V_{FB} \) the surface potential is approximated by \( \psi_{s_{inv}} \) given by eqs. 1.18 - 1.20 and 1.27 - 1.32, where variable \( \Delta_{acc} \) is used to describe the influence of majority carriers. In the accumulation region \( V_{GB} < V_{FB} \) the surface potential is approximated by \( \psi_{s_{acc}} \) given by eqs. 1.33 - 1.35. The total surface potential \( \psi_s \) is simply given by \( \psi_{s_{inv}} + \psi_{s_{acc}} \).

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1. Parameter \( m_0 = 0 \) for the ideal long-channel case.

2. For \( V_{GB} < V_{FB} \) an accumulation layer is formed in both the substrate silicon and the gate polysilicon, in this case \( \psi_p \) is slightly negative and weakly dependent on \( V_{GB} \). This effect has been neglected.
Figure 1: Upper figure: The energy band diagram of an n-type MOS transistor in inversion $V_{GB} > V_{FB}$, where $\psi_s$ is the surface potential, $\psi_p$ is the potential drop in the gate due to the poly-depletion effect, $V$ is the quasi-Fermi potential and $\phi_F$ is the intrinsic Fermi-potential ($\phi_B = 2 \cdot \phi_F$). Lower figure: The surface potential as a function of gate bias for different values of quasi-Fermi potential $V$ ($m_0 = 0$).
A surface-potential-based model automatically incorporates the pinch-off condition at the drain side, and as a result it gives a description of both the linear (or ohmic) region and the saturation region for the ideal long-channel case. In this case the saturation voltage $V_{DSAT}$ (i.e. the drain-source voltage above which saturation occurs) corresponds to eq. (1.21). For short-channel devices, however, no real pinch-off occurs and the saturation voltage is affected by velocity saturation and series-resistance. In this case the saturation voltage $V_{DSAT}$ is calculated using eqs. (1.21)-(1.25). The transition from linear to saturation region is no longer automatically described by the surface-potential-based model. This has been solved in the same way as in [7] by introducing an effective drain-source bias $V_{DSx}$ which changes smoothly from $V_{DS}$ in the linear region to $V_{DSAT}$ in the saturation region, see eq. (1.26).

A surface-potential-based model makes no use of threshold voltage $V_T$. Circuit designers, however, are used to think in terms of threshold voltage, and as a consequence it would be useful to have a description of $V_T$ in the framework of a surface-potential-model. It has been found that an accurate expression of threshold voltage is simply given by:

$$V_T = V_{FB} + \left(1 + \frac{k_0^2}{k_p^2}\right) \cdot (V_{SB} + \Phi_B + 2 \cdot \Phi_T) - V_{SB} + k_0 \cdot \sqrt{V_{SB} + \Phi_B + 2 \cdot \Phi_T}$$

The threshold voltage and other important parameters for circuit design are part of the operating point output as given in Section 1.9.

**Channel Current**

Neglecting the influence of gate and bulk current, the channel current can be written as: $I_{DS} = I_{drift} + I_{diff}$ where ideally the drift component $I_{drift}$ can be approximated by (for $V_{GB} > V_{FB}$):

$$I_{drift} = \beta \cdot \left[ \frac{2 \cdot \left[ V_{GB} - V_{FB} - \frac{\psi_{sl} + \psi_{sb}}{2} \right]}{1 + \frac{4}{k_p} \cdot \left[ V_{GB} - V_{FB} - \frac{\psi_{sl} + \psi_{sb}}{2} \right]} \cdot \left(\frac{\psi_{sl} + \psi_{sb}}{2}\right) \cdot (\psi_{sl} - \psi_{sb}) \right]$$
and the diffusion component \( I_{\text{diff}} \) can be approximated by (for \( V_{GB} > V_{FB} \)):

\[
I_{\text{diff}} = \beta \cdot \phi_T \cdot (Q_{\text{inv}_L} - Q_{\text{inv}_R}) \cdot \frac{t_{ox}}{\varepsilon_{ox}}
\]

In the latter equation \( Q_{\text{inv}_L} \) and \( Q_{\text{inv}_R} \) denote the inversion-layer charge density at the source and drain side, respectively, which are given by eqs. (1.54)-(1.56) (where \( Q_{\text{inv}} = -\varepsilon_{ox}/t_{ox} \cdot V_{\text{inv}} \)).

In the non-ideal case the channel current is affected by several physical effects, such as drain-induced barrier lowering, static feedback, mobility reduction, series-resistance, velocity saturation, channel length modulation and self-heating, which have to be taken into account in the channel current expression:

- In threshold-voltage-based models drain-induced barrier lowering and static feedback are traditionally implemented as a decrease in threshold voltage with drain bias. Here these effects have been implemented as an increase in effective gate bias \( \Delta V_G \) given by eqs. (1.11)-(1.17). An effective drain-source voltage \( V_{DS_{eff}} \) has been used to preserve non-singular behaviour in the higher-order derivatives of \( I_{DS} \) at \( V_{DS_{eff}} = 0 \) V.

- The effects of mobility reduction and series-resistance on channel current have been described in [5], and have consequently been implemented using eqs. (1.47) and (1.51), respectively.

- The effect of velocity saturation has been modelled along the same lines as was done in [6] with the exception of the electrical field distribution. In [6] the influence of the electron velocity saturation expression:

\[
v = \frac{\mu \cdot E_{||}}{\sqrt{1 + (\mu / v_{sat} \cdot E_{||})^2}}
\]

was approximated assuming that the lateral electric field \( E_{||} \) in the denominator is constant and equal to \( (\psi_{s_L} - \psi_{s_R})/L \). Here, we assume that \( E_{||} \) (in the denominator) increases linearly along the channel (from 0 at the source to \( 2 \cdot (\psi_{s_L} - \psi_{s_R})/L \) at the drain), and obtain a more accurate expression for velocity saturation, which has been implemented using eq. (1.49).
The effect of channel length modulation and self-heating on channel current have been described in [6], and have consequently been implemented using eqs. (1.50) and (1.52), respectively.

All the above effects can be incorporated into the channel current expression using eq. (1.53) and eq. (1.59).

![Diagram of MOS transistor with current components labeled](image)

Figure 2: Upper figure: The different gate current components in a MOS transistor. One can distinguish the intrinsic components, i.e. the gate-to-channel current $I_{GC} = I_{GS} + I_{GD}$ and the gate-to-bulk current $I_{GB}$, and the extrinsic, i.e. the gate/source and gate/drain overlap components $I_{Gox}$.

Lower figure: Measured and modelled gate current as a function of gate bias $V_{GS}$ at $V_{DS} = V_{SB} = 0$ V, the different gate current components are also shown. NMOS-transistor, $W/L = 10/0.6 \mu m$ and $t_{ox} = 2$ nm.
Weak-Avalanche Current

At high drain bias, owing to the weak-avalanche effect (or impact ionization), a current $I_{avl}$ will flow between drain and bulk\(^1\). The description of the weak-avalanche current has been taken from MOS Model 9 [3], and is given by eq. (1.60). With the down-scaling of supply voltage for modern CMOS technologies, weak-avalanche becomes less and less important.

Gate Tunnelling Current

With CMOS technology scaling the gate oxide thickness is reduced and, due to the direct-tunnelling of carriers through the oxide, the gate current is no longer negligible, and has to be taken into account. Several gate current components can be distinguished, three components ($I_{GS}$, $I_{GD}$ and $I_{GB}$) due to the intrinsic MOS channel, and two components ($I_{Govq}$ and $I_{Govl}$) due to gate/source and gate/drain overlap region, see Figure 2(a).

For an n-type MOS transistor operating in inversion, the intrinsic gate current density $J_G$ consists of electrons tunnelling from the inversion layer to the gate, the so-called conductance band tunnelling, which in general can be written as [8] (for $V_{GB} > V_{FB}$):

$$J_G \propto -V_{ox} \cdot Q_{inv} \cdot P_{tun} \{ V_{ox} - \chi_B \cdot B \}$$

where $V_{ox}$ is the oxide voltage given by $V_{ox} = V_{GB} - V_{FB} - \psi_p - \psi_s$. The carrier tunnelling probability $P_{tun}$ is a function of the oxide voltage $V_{ox}$, the oxide energy barrier $\chi_B$ as observed by the inversion-layer carriers, and a parameter $B$. This probability is given by eq. (1.61), where both direct-tunnelling for $V_{ox} < \chi_B$ and Fowler-Nordheim tunnelling for $V_{ox} > \chi_B$ have been taken into account.

Owing to quantum-mechanical energy quantization in the potential well at the SiO$_2$-surface, the electrons in the inversion layer are not situated at the bottom of the conduction band, but in the lowest energy subband which lies $\Delta \chi_B$ above the conduction band. Assuming that only the lowest energy subband is occupied by electrons, the value of $\Delta \chi_B$ can be given by eq. (1.78) [9]. As a result the oxide barrier $\chi_{B,eff}$ has to be lowered by an amount of $\Delta \chi_B$, see eq. (1.79).

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\(^1\)In reality part of the generated avalanche current will also flow from drain to source [1], this has been neglected.
In inversion the total intrinsic gate current consists of electrons tunnelling from inversion layer to gate, the so-called gate-to-channel current $I_{GC}$. These electrons are supplied by both source ($I_{GS}$) and drain ($I_{GD}$). The gate-to-channel current $I_{GC}$ can be calculated from:

$$I_{GC} = W \int_{0}^{L} J_{G} \cdot dx$$

where $x$ is the coordinate along the channel. Using a first-order perturbation approximation, i.e. assuming the gate current is small enough so that it does not change the distribution of surface potential along the channel, $I_{GC}$ can be calculated by eqs. (1.78)-(1.88). In the same way the partitioning of $I_{GC}$ into $I_{GS}$ and $I_{GD}$ can be calculated using:

$$I_{GS} = W \int_{0}^{L} \left(1 - \frac{x}{L}\right) J_{G} \cdot dx$$

$$I_{GD} = W \int_{0}^{L} \frac{dx}{L} J_{G} \cdot dx$$

which results in expressions for $I_{GS}$ and $I_{GD}$ as given by eqs. (1.89)-(1.91). The gate-to-channel current $I_{GC}$ can be seen in Figure 2(b) as a function of gate bias for a typical n-MOS transistor at $V_{DS} = 0$ (i.e. $I_{GS} = I_{GD} = 1/2 \cdot I_{GC}$).

For an n-type MOS transistor operating in accumulation, an accumulation layer of holes is formed in the p-type substrate and an accumulation layer of electrons is formed in the n⁺-type polysilicon gate. Since the oxide energy barrier for electrons $\chi_{B_n}$ is considerably lower than that for holes $\chi_{B_p}$, the gate current will mainly consist of electrons tunnelling from the gate to the bulk silicon, where they are swept to the bulk terminal. In this case the (intrinsic) gate current density $J_{G}$ can be written as [8] (for $V_{GB} < V_{FB}$):

$$J_{G} \propto -V_{ox} \cdot Q_{acc} \cdot P_{tan}\{\frac{-V_{ox}}{\chi_{B_n}};B\}$$

where $Q_{acc}$ is the accumulation charge density in the gate given by $\frac{\epsilon_{ox}}{t_{ox}} \cdot V_{ox}$. In order to limit calculation time the quantum-mechanical oxide barrier lowering in this case is neglected, and the resulting expression for $I_{GB}$ is given by eqs. (1.76)-(1.77). The gate-to-
bulk current $I_{GB}$ can be seen in Figure 2 (b) as a function of gate bias for a typical n-MOS transistor at $V_{DS} = 0$.

Apart from the intrinsic components $I_{GC}$ and $I_{GB}$, considerable gate current can be generated in the gate/source- and gate/drain-overlap regions. Concentrating on the gate/source-overlap region, in order to calculate the overlap gate current, the overlap region is treated as an n$^+$-gate/oxide/n$^+$-bulk MOS capacitance where the source acts as bulk. Although the impurity doping concentration in the n$^+$-source extension region is non-uniform in both lateral and transversal direction, it is assumed that an effective flat-band voltage $V_{FBov}$ and body-factor $k_{ov}$ can be defined for this structure. Furthermore, assuming that only accumulation and depletion occur in the n$^+$-source region, a surface potential $\psi_{sov}$ can be calculated using:

$$
\left( \frac{V_{GS} - V_{FBov} - \psi_{pov} - \psi_{sov}}{k_{ov}} \right)^2 = -\psi_{sov} + \phi_T \cdot \left[ \exp \left( \frac{\psi_{sov}}{\phi_T} \right) - 1 \right]
$$

where the potential drop in the polysilicon gate material due to the poly-depletion effect $\psi_{pov}$ is given by:

$$
\psi_{pov} = \begin{cases} 
0 & V_{GS} \leq V_{GBov} \\
\sqrt{\left( V_{GS} - V_{FBov} - \psi_{sov} - \frac{k_p}{4} - \frac{k_p}{2} \right)^2} & V_{GS} > V_{FBov}
\end{cases}
$$

Again the surface potential $\psi_{pov}$ can be explicitly approximated, this is done by using eqs. (1.62)-(1.68).

For $V_{GS} > V_{FBov}$ a negatively charged accumulation layer is formed in the overlapped n$^+$-source extension and a positively charged depletion layer is formed in the overlapping gate.

1. In the following derivation, the same can be done for the gate/drain-overlap region by replacing the source by the drain.

2. Since the source extension has a very high doping concentration, an inversion layer in the gate/source overlap will only be formed at very negative gate-source bias values. This effect has been neglected.
In this case the overlap gate current will mostly consist of electrons tunnelling from the 
source accumulation layer to the gate, it is given by:

\[ I_{Gov} \propto -V_{ov} \cdot Q_{ov} \cdot P_{tun} \{ V_{ov} \cdot \chi_B \cdot B \} \]

where \( V_{ov} \) is the oxide voltage for the gate/source-overlap \( = V_{GS} - V_{FBov} - \psi_{pov} - \psi_{sov} \),
given by eqs. (1.69)-(1.71), and \( Q_{ov} \) is the total charge density in the n^+-source region
\( = e_{ox} / t_{ox} \cdot V_{ov} \). For \( V_{GS} < V_{FBov} \) the situation is reversed, a positively charged depletion
layer is formed in the overlapped n^+-source extension and a negatively charged accumulation
layer is formed in the overlapping gate. In this case the overlap gate current will mostly con-
sist of electrons tunnelling from the gate accumulation layer to the source, it is given by:

\[ I_{Gov} \propto V_{ov} \cdot Q_{ov} \cdot P_{tun} \{ -V_{ov} \cdot \chi_B \cdot B \} \]

The overlap gate current components can now be given by eqs. (1.72)-(1.75). In Figure 2 (b)
the gate overlap current \( I_{Gov} \) is shown as a function of gate bias for a typical n-MOS transistor
at \( V_{DS} = 0 \) (i.e. \( I_{Gov} = I_{Gov0} \)). For n-type and p-type MOS transistors the gate current
behaviour is different due to the type of carriers that constitute the different gate current com-
ponents\(^1\). The difference is summarized in Table 1.

---
\(^1\) It is assumed here that the gate current is only determined by conductance band tunnelling.
For high values of gate bias (i.e. \( q \cdot V_{ox} > E_g \)) electrons in the bulk valence band may also
tunnel through the oxide to the gate conduction band. This mechanism is referred to as
valence band tunnelling, and it has not been taken into account in MOS Model 11.
Table 1: The type of carriers that contribute to the gate tunnelling current in the various operation regions for the intrinsic MOSFET, the gate/drain- and gate/source-overlap regions. The type of carriers determine the value of oxide energy barrier $\chi_B$ that has to be used ($\chi_{B_N}$ for electrons, $\chi_{B_P}$ for holes). In the last row the direction of gate current is indicated.

<table>
<thead>
<tr>
<th>Type</th>
<th>Intrinsic MOSFET</th>
<th>Overlap Regions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Accumulation</td>
<td>Inversion</td>
</tr>
<tr>
<td>NMOS</td>
<td>electrons</td>
<td>electrons</td>
</tr>
<tr>
<td>PMOS</td>
<td>electrons</td>
<td>holes</td>
</tr>
<tr>
<td></td>
<td>$I_{GB}$</td>
<td>$I_{GS}/I_{GD}$</td>
</tr>
</tbody>
</table>

Comments on Charge Equations

In a typical MOS structure we can distinguish intrinsic and extrinsic charges. The latter are due to the gate/source and gate/drain overlap regions. The drain/source junctions also contribute to the capacitance behaviour of a MOSFET, but this is not taken into account in MOS Model 11; it is described by a separate junction diode model.

Intrinsic Charges

In the intrinsic MOS transistor charges can be attributed to the four terminals. The bulk charge $Q_B$, which is determined by either the depletion charge (for $V_{GB} > V_{FB}$) or the accumulation charge (for $V_{GB} < V_{FB}$), can be calculated from:

$$Q_B = W \cdot \int_0^L (Q_{tot} - Q_{inv}) \cdot dx$$

where $Q_{tot}$ is the total charge density in the silicon bulk ($Q_{tot} = -\varepsilon_{ox}/t_{ox} \cdot V_{ox}$). The total inversion-layer charge $Q_{inv}$ is split up in a source $Q_S$ and a drain $Q_D$ charge, they can be calculated using the Ward-Dutton charge partitioning scheme [10]:

$$Q_S = W \cdot \int_0^L \left(1 - \frac{x}{L}\right) \cdot Q_{inv} \cdot dx$$

$$Q_D = W \cdot \int_0^L \frac{x}{L} \cdot Q_{inv} \cdot dx$$
Since charge neutrality holds for the complete transistor, the gate charge is simply given by:

\[ Q_G = -Q_S - Q_D - Q_B \]

The above equations have been solved, and the charges are given by eqs. (1.94)-(1.100). In these equations \( C_{ox,eff} \) is the effective oxide capacitance, which is smaller than the ideal oxide capacitance \( C_{ox} \) due to quantum-mechanical effects: Quantum-mechanically, the inversion/accumulation charge concentration is not maximum at the Si-SiO\(_2\)-interface (as it would be in the classical case), but reaches a maximum at a distance \( \Delta z \) from the interface [9]. This quantum-mechanical effect can be taken into account by an effective oxide thickness \( t_{ox} + \varepsilon_{ox}/\varepsilon_{si} \cdot \Delta z \), where \( \Delta z \) is dependent on the effective electric field \( E_{eff} \) [9], [11] \( (E_{eff} = -\varepsilon_{ox}/\varepsilon_{si} \cdot V_{eff}/t_{ox}) \). The effective oxide thickness results in an effective oxide capacitance \( C_{ox,eff} \), see eq. (1.94).

It should be noted that the above charge model is quasi-static. A phase-shift between drain channel current and gate voltage is not taken into account. This implies that for a few applications at high frequencies approaching the cut-off frequency, errors have to be expected due to non-quasi-static effects. Nevertheless non-quasi-effects can be taken into account using a segmentation model as described in [12].

**Extrinsic Charges**

The gate/source- and gate/drain-overlap regions act as bias-dependent capacitances. In order to take this bias-dependence into account the overlap regions are treated as an \( n^+ \)-gate/oxide/\( n^- \)-bulk MOS capacitance along the same lines as was done for the overlap gate current, see the section: Comments on Current Equations. The charge in the overlap regions can simply be given by eqs. (1.92)-(1.93). The quantum-mechanical effect on oxide thickness has been neglected here in order to reduce calculation time.

**Comments on Noise Equations**

In a MOS transistor generally three different types of noise can be observed: \( 1/f \) noise, thermal noise and induced gate noise. The gate tunnel current and the bulk avalanche current will also exhibit noisy behaviour (due to shot noise), however this has been neglected in MOS Model 11.

**1/f -Noise**

At low frequencies flicker (or \( 1/f \)) noise becomes dominant in MOSFETs. In the past this type of noise has been interpreted either in terms of trapping and detrapping of charge carri-
ers in the gate oxide or in terms of mobility fluctuations. Over the past years, a general model for $1/f$-noise which combines both of the above physical origins [13], [14], has found wide acceptance in the field of MOS modelling. The model assumes that the carrier number in the channel fluctuates due to trapping/detrapping in the gate oxide, and that these number fluctuations also affect the carrier mobility resulting in (correlated) mobility fluctuations.

The same model is part of MOS Model 9 [15], and has been used to calculate the $1/f$-noise for MOS Model 11. The calculations have been performed in such a way that the resulting expression for spectral density is valid for all operation regions (i.e. both in subthreshold and above threshold), it is given by eqs. (1.105)-(1.108).

### Thermal Noise

Since the MOSFET channel can be considered as a non linear resistor, the channel current is subject to thermal noise. Let thermal noise current sources be parallel connected to each infinitesimal short element of the channel, it can be shown that the noise spectral density, which is defined by [16]:

$$\langle \Delta i_{th}^2 \rangle = \int_0^\infty s_{th}(f) df$$

is given by a generalized Nyquist relation:

$$S_{th} = \frac{N_T}{L^2} \cdot \int_0^L g(x) dx$$

where $N_T$ is equal to $4 \cdot k_B \cdot T$ and $g(x)$ is the local specific channel conductance:

$$g(x) = -\mu(x) \cdot W \cdot Q_{inv}(x)$$

Here the mobility $\mu(x)$ is position dependent mainly due to the effect of velocity saturation. Elaborating the latter integral via a transform of the $x$ variable into the quasi-Fermi potential $V(x)$, we obtain the spectral density given by eqs. (1.102)-(1.104). Again continuity of the noise model is assured along all modes of operation. The above thermal noise model has been found to accurately describe experimental results for various CMOS technologies without having to invoke carrier heating effects [17].
Figure 3: Noise current sources in the electrical scheme of the MOS transistor

**Induced Gate Noise**

Owing to capacitive coupling between gate and channel, the fluctuating channel current induces noise in the gate terminal at high frequencies. Unfortunately the calculation of this component from first principles is too complicated to provide a result applicable to circuit simulation. It is more practical to derive the desired result from an equivalent circuit presentation given in Figure 3. Owing to the mentioned capacitive coupling, a part of the channel is present as a resistance in series with the gate input capacitance. In saturation this resistance is approximately equal to:

\[ R_i = \frac{1}{3} \cdot g_m \]

It can be easily shown that the latter resistance produces an input noise current with a spectral density given by eq. (1.109). In addition, since \( \Delta i_{th} \) and \( \Delta i_{ig} \) have the same physical source, both spectral densities are correlated. This is expressed by eqs. (1.110) and (1.111). The induced gate noise \( S_{ig} \) is a so-called non-quasi static (NQS) effect. Since the use of the channel current noise description in an NQS segmentation model [12] would automatically result in a correct description of induced gate noise, \( S_{ig} \) can be made equal to zero by using parameter GATENOISE, see eq. (1.109).
1.2.2 Basic Equations

The equations listed in the following sections, are the basic equations of MOS model 11 without any adaptation necessary for numerical reasons. As such they form the base for parameter extraction. In the following, a function is denoted by \( F\{\text{variable, ...}\} \), where \( F \) denotes the function name and the function variables are enclosed by braces \{\}. 

**Internal Parameters**

\( P_D = 1 + (k_0/k_p)^2 \) \hspace{1cm} (1.1)

\( V_{\text{limit}} = 4 \cdot \phi_T \) \hspace{1cm} (1.2)

\[ \theta_{\text{R}}^{\text{eff}} = \frac{1}{2} \cdot \theta_{\text{R}} \cdot \left( 1 + \frac{\theta_{\text{R}}^{\text{1}}}{1/2 + \theta_{\text{R}}^{\text{2}}} \right) \] \hspace{1cm} (1.3)

\[ Acc = \left. \frac{\partial \psi_s}{\partial V_{\text{GB}}} \right|_{V_{\text{GB}} = V_{\text{FB}}} = \frac{1}{1 + k_0/(\sqrt{2} \cdot \phi_T)} \] \hspace{1cm} (1.4)

\[ N_{\phi_T} = (2.6)^2/k_0 \] \hspace{1cm} (1.5)

\[ Acc_{\text{ov}} = \left. \frac{\partial \psi_{\text{sov}}}{\partial V_{\text{GB}}} \right|_{V_{\text{GB}} = V_{\text{FB}}^{\text{ov}}} = \frac{1}{1 + k_{\text{ov}}/(\sqrt{2} \cdot \phi_T)} \] \hspace{1cm} (1.6)

\[ QM_\psi = \begin{cases} QM_N \cdot (\varepsilon_{\text{ox}}/t_{\text{ox}})^{2/3} & \text{for NMOS} \\ QM_P \cdot (\varepsilon_{\text{ox}}/t_{\text{ox}})^{2/3} & \text{for PMOS} \end{cases} \] \hspace{1cm} (1.7)
Basic Current Equations

Drain induced barrier lowering and Static Feedback:

\[ V_{GB_{eff}} = \begin{cases} 0 & V_{GS} + V_{SB} - V_{FB} \leq 0 \\ V_{GS} + V_{SB} - V_{FB} & V_{GS} + V_{SB} - V_{FB} > 0 \end{cases} \]  

(1.11)

\[ \psi_{sat0} = \left( \frac{\sqrt{P_D \cdot V_{GB_{eff}} + k_0^2 / 4 - k_0 / 2}}{P_D} \right)^2 \]  

(1.12)

\[ D_{dibl} = \sigma_{dibl} \cdot \sqrt{V_{SB} + \phi_B} \]  

(1.13)

\[ D_{sf} = \begin{cases} 0 & \psi_{sat0} - V_{SB} - \phi_B \leq 0 \\ \sigma_{sf} \cdot \sqrt{\psi_{sat0} - V_{SB} - \phi_B} & \psi_{sat0} - V_{SB} - \phi_B > 0 \end{cases} \]  

(1.14)

\[ D = \begin{cases} D_{dibl} & D_{sf} \leq D_{dibl} \\ D_{sf} & D_{sf} > D_{dibl} \end{cases} \]  

(1.15)
\[ V_{DS_{eff}} = \frac{V_{DS}^4}{(V_{limit}^2 + V_{DS}^2)^{3/2}} \]  

(1.16)

\[ \Delta V_G = D \cdot V_{DS_{eff}} \]  

(1.17)

Redefinition of \( V_{GB_{eff}} \), equation (1.11)

\[ V_{GB_{eff}} = \begin{cases} 0 & V_{GS} + V_{SB} + \Delta V_G - V_{FB} \leq 0 \\ V_{GS} + V_{SB} + \Delta V_G - V_{FB} & V_{GS} + V_{SB} + \Delta V_G - V_{FB} > 0 \end{cases} \]  

(1.18)

\[ \Delta_{acc} = \phi_T \cdot \left[ \exp\left(\frac{V_{GB_{eff}}}{\phi_T}\right) - 1 \right] \]  

(1.19)

\[ \psi_{sat_1} = \left( \frac{P_D \cdot (V_{GB_{eff}} + \Delta_{acc}) + k_0^2/4 - k_0/2}{P_D} \right)^2 - \Delta_{acc} \]  

(1.20)

**Drain Saturation Voltage:**

\[ V_{DSAT_{long}} = \begin{cases} 0 & \psi_{sat_1} - V_{SB} - \phi_B \leq 0 \\ \psi_{sat_1} - V_{SB} - \phi_B & \psi_{sat_1} - V_{SB} - \phi_B > 0 \end{cases} \]  

(1.21)

\[ T_{sat} = \begin{cases} \theta_{sat} & \text{for NMOS} \\ \frac{\theta_{sat}}{(1 + \theta_{sat}^2 \cdot V_{DSAT_{long}}^2)^{1/4}} & \text{for PMOS} \end{cases} \]  

(1.22)
\[ \Delta_{SAT} = \frac{T_{\text{sat}} - \theta_{R_{\text{eff}}}}{\sqrt{\frac{2}{V_{DSAT_{\text{long}}}} + T_{\text{sat}}^2 + \theta_{R_{\text{eff}}}}} \]  
\[ (1.23) \]

\[ V_{DSAT_{\text{short}}} = V_{DSAT_{\text{long}}} \cdot \left( 1 - \frac{9}{10} \cdot \frac{\Delta_{SAT}}{1 + \sqrt{1 - \Delta_{SAT}^2}} \right) \]  
\[ (1.24) \]

\[ V_{DSAT} = \begin{cases} V_{\text{limit}} & \text{if } V_{DSAT_{\text{short}}} \leq V_{\text{limit}} \\ V_{DSAT_{\text{short}}} & \text{if } V_{DSAT_{\text{short}}} > V_{\text{limit}} \end{cases} \]  
\[ (1.25) \]

\[ V_{DS} = \frac{V_{DS} \cdot V_{DSAT}}{[V_{DS}^{2m} + V_{DSAT}^{2m}]^{1/(2m)}} \]  
\[ (1.26) \]

**Surface Potential:**

\[ f_1(\psi) = \begin{cases} \psi_{sat1} & \psi_{sat1} \leq \psi \\ \psi & \psi_{sat1} > \psi \end{cases} \]  
\[ (1.27) \]

\[ f_2(\psi) = f_1(\psi) + \frac{\psi_{sat1} - f_1(\psi)}{\sqrt{\frac{[\psi_{sat1} - f_1(\psi)]^2}{1 + \frac{N_{\phi_T} \cdot \phi_T^2}{k_p^2}}} \]  
\[ (1.28) \]

\[ f_3(\psi) = \frac{2 \cdot [V_{GB_{\text{eff}}} - f_2(\psi)]}{1 + \sqrt{1 + 4/k_p^2 \cdot [V_{GB_{\text{eff}}} - f_2(\psi)]}} \]  
\[ (1.29) \]
\[ \psi_{s_{\text{inv}}} \{ \psi \} = f_1 \{ \psi \} + \phi_T \cdot [1 + m_0] \cdot \ln \left[ \frac{f_3 \{ \psi \}^2 - f_1 \{ \psi \} - \Delta_{\text{acc}} + \phi_T}{\phi_T} \right] \]  

(1.30)

\[ \psi_{s_0}^* = \psi_{s_{\text{inv}}} \cdot \{ V_{SB} + \phi_B \} \]  

(1.31)

\[ \psi_{s_L}^* = \psi_{s_{\text{inv}}} \cdot \{ V_{DS} + V_{SB} + \phi_B \} \]  

(1.32)

**Surface Potential in Accumulation:**

\[ f_1 = \begin{cases} 
Acc \cdot (V_{GS} + V_{SB} + \Delta V_G - V_{FB}) & V_{GS} + V_{SB} + \Delta V_G - V_{FB} \leq 0 \\
0 & V_{GS} + V_{SB} + \Delta V_G - V_{FB} > 0 
\end{cases} \]  

(1.33)

\[ f_2 = \frac{f_1}{\sqrt{1 + \frac{f_1^2}{N_{\phi_T} \cdot \phi_T^2}}} \]  

(1.34)

\[ \psi_{s_{\text{acc}}} = -\phi_T \cdot \ln \left[ \frac{\left\{ \frac{f_1 \cdot Acc - f_2}{k_0} \right\}^2 - f_2 + \phi_T}{\phi_T} \right] \]  

(1.35)
Auxiliary Variables:

\[ \Delta \psi = \psi_{s_L}^* - \psi_{s_0}^* \]  \hspace{1cm} (1.36)

\[ \overline{\psi}_{inv} = \frac{\psi_{s_L}^* + \psi_{s_0}^*}{2} \]  \hspace{1cm} (1.37)

\[ V_{GT}\{\psi_{s_{inv}}^*\} = \frac{2 \cdot [V_{GB_{eff}} - \psi_{s_{inv}}]}{1 + \sqrt{1 + 4/k_p^2 \cdot [V_{GB_{eff}} - \psi_{s_{inv}}]}} - k_0 \cdot \sqrt{\psi_{s_{inv}} + \Delta acc} \]  \hspace{1cm} (1.38)

\[ \overline{V}_{GT} = V_{GT}\{\overline{\psi}_{inv}\} \]  \hspace{1cm} (1.39)

\[ V_{GT_0} = V_{GT}\{\psi_{s_0}^*\} \]  \hspace{1cm} (1.40)

\[ V_{GT_L} = V_{GT}\{\psi_{s_L}^*\} \]  \hspace{1cm} (1.41)

\[ V_{ox} = \frac{2 \cdot [V_{GS} + V_{SB} + \Delta V_G - V_{FB} - \overline{\psi}_{inv} - \psi_{acc}]}{1 + \sqrt{1 + 4/k_p^2 \cdot [V_{GB_{eff}} - \overline{\psi}_{inv}]}} \]  \hspace{1cm} (1.42)

\[ \partial V_{ox} = \frac{2}{1 + \sqrt{1 + 4/k_p^2 \cdot [V_{GB_{eff}} - \overline{\psi}_{inv}]}} \]  \hspace{1cm} (1.43)
\[ V_{eff} = \bar{V}_{G_T} + \eta_{mob} \cdot (V_{ox} - \bar{V}_{G_T}) \]  \hspace{1cm} (1.44)

\[ \xi = \phi_T \cdot \frac{\partial \bar{V}_{G_T}}{\partial \psi_{inv}} = \phi_T \cdot \left[ \frac{1}{1 + 4/k_p^2 \cdot [V_{GB_{eff}} - \psi_{inv}]} + \frac{k_0}{2 \cdot \sqrt{\psi_{inv} + \Delta acc}} \right] \]  \hspace{1cm} (1.45)

\[ \bar{V}_{G_T}^* = \frac{V_{GT_0} + V_{GT}}{2} + \xi \]  \hspace{1cm} (1.46)

**Second-Order Effects**

**Mobility Degradation:**

\[ G_{mob} = \frac{\mu_0}{\mu} = \begin{cases} 
1 + [(\theta_{ph} \cdot V_{eff})^{v/3} + (\theta_{sr} \cdot V_{eff})^{2v}]^{1/v} & \text{for NMOS} \\
1 + [(\theta_{ph} \cdot V_{eff})^{v/3} + (\theta_{sr} \cdot V_{eff})^{v}]^{1/v} & \text{for PMOS} 
\end{cases} \]  \hspace{1cm} (1.47)

**Velocity Saturation:**

\[ x = \begin{cases} 
\frac{2 \cdot \theta_{sat} \cdot \Delta \psi}{\sqrt{G_{mob}}} & \text{for NMOS} \\
\frac{2 \cdot \theta_{sat} \cdot \Delta \psi}{\sqrt{G_{mob}}} \cdot \left(1 + \theta_{sat}^2 \cdot \Delta \psi^2\right)^{1/4} & \text{for PMOS} 
\end{cases} \]  \hspace{1cm} (1.48)

\[ G_{vsat} = \frac{G_{mob}}{2} \cdot \left[ \sqrt{1 + x^2} + \frac{\ln(x + \sqrt{1 + x^2})}{x} \right] \]  \hspace{1cm} (1.49)
Channel Length Modulation:

\[ G_{DL} = 1 - \frac{\Delta L}{L} = 1 - \alpha \cdot \ln \left( \frac{V_{DS} - V_{DS_s} + \sqrt{(V_{DS} - V_{DS_s})^2 + V_p^2}}{V_p} \right) \quad (1.50) \]

Series Resistance and Self-Heating:

\[ G_R = \theta_R \cdot \left( 1 + \frac{\theta_{R1}}{\theta_{R2} + \bar{V}_{G_T}} \right) \cdot \bar{V}_{G_T} \quad (1.51) \]

\[ G_{Th} = \theta_{Th} \cdot V_{DS} \cdot \Delta \psi \cdot \bar{V}_{G_T} \quad (1.52) \]

\[ G_{tot} = G_{Th} + \frac{[G_{DL} \cdot G_{vsat} + G_R]}{2} \cdot \left[ 1 + \frac{4 \cdot G_R / G_{vsat}}{\left( G_{DL} \cdot G_{vsat} + G_R \right)^2 (G_{vsat} - G_{mob})} \right] \quad (1.53) \]

Inversion-Layer Charge

\[ Q_{inv} = -\varepsilon_{ox} / t_{ox} \cdot V_{inv} \quad : \]

\[ V_{inv} \{ \psi_{s_{inv}}, \psi \} = \frac{k_0 \cdot \phi_T \cdot \exp \left[ \frac{\psi_{s_{inv}} - \psi}{(1 + m_0) \cdot \phi_T} \right]}{\sqrt{\psi_{s_{inv}} + \Delta acc + \phi_T \cdot \exp \left[ \frac{\psi_{s_{inv}} - \psi}{(1 + m_0) \cdot \phi_T} \right] + \sqrt{\psi_{s_{inv}} + \Delta acc}}} \quad (1.54) \]
\[ V_{inv0} = V_{inv} \left\{ \psi_s^*, V_{SB} + \psi_B \right\} \quad (1.55) \]

\[ V_{invL} = V_{inv} \left\{ \psi_s^*, V_{DSx} + V_{SB} + \psi_B \right\} \quad (1.56) \]

**Drain Current**

\[ I_{drift} = \beta \cdot \bar{V}_{G_T} \cdot \Delta \psi \quad (1.57) \]

\[ I_{diff} = \beta \cdot \phi_T \cdot (V_{inv0} - V_{invL}) \quad (1.58) \]

\[ I_{DS} = \frac{I_{drift} + I_{diff}}{G_{tot}} \quad (1.59) \]

**Weak-Avalanche**

\[ I_{avl} = \begin{cases} 
0 & V_{DS} \leq a_3 \cdot V_{DSAT} \\
 a_1 \cdot I_{DS} \cdot \exp \left( -\frac{a_2}{V_{DS} - a_3 \cdot V_{DSAT}} \right) & V_{DS} > a_3 \cdot V_{DSAT} 
\end{cases} \quad (1.60) \]

**Gate Current Equations**

The tunnelling probability is given by:

\[ P_{tun}\{V_{ox}, \chi_B; B\} = \begin{cases} 
\exp \left( -B \cdot \left[ 1 - \left( \frac{V_{ox}}{\chi_B} \right)^{3/2} \right] \right) & V_{ox} < \chi_B \\
\exp \left( -B / V_{ox} \right) & V_{ox} \geq \chi_B 
\end{cases} \quad (1.61) \]
Source/Drain Gate Overlap Current:

First calculate the oxide voltage $V_{ov}$ at both Source and Drain overlap:

$$V_{GX_{eff}}\{V_{GX}\} = \begin{cases} V_{GX} - V_{FBov} & V_{GX} - V_{FBov} \leq 0 \\ 0 & V_{GX} - V_{FBov} > 0 \end{cases}$$ (1.62)

$$\Delta_{ov}\{V_{GX}\} = \phi_T \cdot \left[ \exp\left( \frac{Acc_{ov} \cdot V_{GX_{eff}}\{V_{GX}\}}{\phi_T} \right) - 1 \right]$$ (1.63)

$$\psi_{sat_{ov}}\{V_{GX}\} = \left[ -\frac{k_{ov}^2}{4} - V_{G_{eff}}\{V_{GX}\} + \Delta_{ov}\{V_{GX}\} - \frac{k_{ov}}{2} \right]^2 \Delta_{ov}\{V_{GX}\}$$ (1.64)

$$f_1\{V_{GX}\} = \begin{cases} 0 & V_{GX} - V_{FBov} \leq 0 \\ Acc_{ov} \cdot [V_{GX} - V_{FBov}] & V_{GX} - V_{FBov} > 0 \end{cases}$$ (1.65)

$$f_2\{V_{GX}\} = \frac{f_1\{V_{GX}\}}{\sqrt{1 + \frac{[f_1\{V_{GX}\}]^2}{N \phi_T \cdot \phi_T^2}}}$$ (1.66)

$$f_3\{V_{GX}\} = \frac{2 \cdot \left[ \frac{f_1\{V_{GX}\}}{Acc_{ov}} - f_2\{V_{GX}\} \right]}{1 + \left[ 1 + 4/k_p^2 \cdot \left( \frac{f_1\{V_{GX}\}}{Acc_{ov}} - f_2\{V_{GX}\} \right) \right]}$$ (1.67)
Next calculate the gate tunnelling current in both Source and Drain overlap:

\[ P_{ov}\{V_{ov}\} = P_{tun}\{V_{ov} : \chi_{B_{inv}} : B_{inv} \} \]  

(1.72)

\[ I_{Gov}\{V_{GX} , V_{ov}\} = I_{GOV} \cdot V_{GX} \cdot V_{ov} \cdot [P_{ov}\{V_{ov}\} - P_{ov}\{-V_{ov}\}] \]  

(1.73)

\[ I_{Govv} = I_{Gov}\{V_{GS} , V_{ovv}\} \]  

(1.74)

\[ I_{Govl} = I_{Gov}\{V_{GS} - V_{DS} , V_{ovl}\} \]  

(1.75)

**Intrinsic Gate Current**

The gate tunnelling current in accumulation:

\[ P_{acc} = P_{tun}\{-V_{ov} : \chi_{B_{acc}} : B_{acc} \} \]  

(1.76)
The tunnelling current in inversion, including quantum-mechanical barrier lowering $\Delta \chi_B$:

$$\Delta \chi_B = Q M \psi \cdot \left( \frac{\bar{V}_{G_T}}{3} + V_{ox} - \bar{V}_{G_T} \right)^{2/3}$$  \hspace{1cm} (1.78)

$$\chi_{B_{\text{eff}}} = \chi_{B_{\text{inv}}} - \Delta \chi_B$$  \hspace{1cm} (1.79)

$$B_{\text{eff}} = B_{\text{inv}} \cdot \left( \frac{\chi_{B_{\text{eff}}}}{\chi_{B_{\text{inv}}}} \right)^{3/2}$$  \hspace{1cm} (1.80)

$$P_{\text{inv}} = P_{\text{tun}} \{ V_{ox} \cdot \chi_{B_{\text{eff}}} \cdot B_{\text{eff}} \}$$  \hspace{1cm} (1.81)

$$B_{\text{inv}}^* = \frac{3}{8} \cdot \chi_{B_{\text{eff}}}^{-2} \cdot B_{\text{eff}} \cdot \partial V_{ox}$$  \hspace{1cm} (1.82)

$$\xi^* = \frac{\xi}{\phi_T \cdot \bar{V}_{G_T}}$$  \hspace{1cm} (1.83)

$$\partial V_{ox}^* = \frac{\partial V_{ox}}{V_{ox}}$$  \hspace{1cm} (1.84)

$$P_{GC} = 1 + \frac{\left[ (B_{inv}^*)^2 + 4 \cdot B_{inv}^* \cdot \xi^* + 2 \cdot B_{inv}^* \cdot \partial V_{ox}^* + 2 \cdot \xi^* + 2 \cdot 4 \cdot \partial V_{ox}^* \cdot \xi^* \right] \cdot \Delta \psi^2}{24}$$  \hspace{1cm} (1.85)
The total intrinsic gate current \( I_{GC} \):

\[
I_{GC} = I_{GC} \cdot \bar{V}_{inv} \cdot P_{GC}
\]

(1.88)

Bias-Dependent Overlap Capacitance:

\[
P_{GS} = [B_{inv}^{*} + \partial V_{ox}^{*}] \cdot \frac{\Delta \psi}{12} + [(B_{inv}^{*})^{2} \cdot (B_{inv}^{*} + 5 \cdot \xi^{*} + 3 \cdot \partial V_{ox}^{*}) + 2 \cdot \xi^{*2} \cdot (B_{inv}^{*} - \xi^{*} + \partial V_{ox}^{*}) + 10 \cdot B_{inv}^{*} \cdot \xi^{*} \cdot \partial V_{ox}^{*}] \cdot \frac{\Delta \psi^{3}}{480}
\]

(1.89)

\[
I_{GS} = \frac{1}{2} \cdot I_{GC} + \left( P_{GS} \cdot \bar{V}_{inv} + \frac{V_{inv_{0}} - V_{inv_{L}}}{12} \right) \cdot \bar{I}_{GC} + I_{Gov_{0}}
\]

(1.90)

\[
I_{GD} = I_{GC} - I_{GS} + I_{Gov_{0}} + I_{Gov_{L}}
\]

(1.91)

Basic Charge Equations

Bias-Dependent Overlap Capacitance:

\[
Q_{ov_{0}} = C_{GSO} \cdot V_{ov_{0}}
\]

(1.92)

\[
Q_{ov_{L}} = C_{GDO} \cdot V_{ov_{L}}
\]

(1.93)
Intrinsic Charges:

\[ C_{\text{ox eff}} = \frac{C_{\text{ox}}}{1 + QM_{t_{\text{ox}}} \cdot \left[ \frac{V_{\text{eff}}}{\eta_{\text{mob}}} \right]^{-1/3}} \]  \hspace{1cm} (1.94)

\[ \Delta V_{G_T} = \frac{V_{G_{T0}} - V_{G_{T_{L}}}}{2 \cdot \left( 1 + \theta_{R} \cdot \frac{V_{G_T}^*}{G_{\text{tot}}} \right)} \]  \hspace{1cm} (1.95)

\[ F_{j} = \frac{\Delta V_{G_T}}{V_{G_T}^*} \]  \hspace{1cm} (1.96)

\[ Q_{S} = -\frac{C_{\text{ox eff}}}{2} \cdot \left[ V_{G_T}^* + \frac{\Delta V_{G_T}}{3} \cdot \left( F_{j} - \frac{F_{j}^{2}}{5} + 1 \right) - \xi \right] \]  \hspace{1cm} (1.97)

\[ Q_{D} = -\frac{C_{\text{ox eff}}}{2} \cdot \left[ V_{G_T}^* + \frac{\Delta V_{G_T}}{3} \cdot \left( F_{j} + \frac{F_{j}^{2}}{5} - 1 \right) - \xi \right] \]  \hspace{1cm} (1.98)

\[ Q_{B} = -C_{\text{ox eff}} \cdot \left[ V_{\text{ox}} - V_{G_T}^* + \xi \right] \]  \hspace{1cm} (1.99)

\[ Q_{G} = -[Q_{S} + Q_{D} + Q_{B}] \]  \hspace{1cm} (1.100)
Noise Equations

In these equations $f$ represents the operation frequency of the transistor.

\[ g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \]  
(1.101)

\[ T_{sat} = \begin{cases} 
\frac{\theta^2_{sat}}{\sqrt{1 + \theta^2_{sat} \cdot \Delta \psi^2}} & \text{for NMOS} \\
\frac{\theta^2_{sat}}{\sqrt{1 + \theta^2_{sat} \cdot \Delta \psi^2}} & \text{for PMOS} 
\end{cases} \]  
(1.102)

\[ R_{ideal} = \frac{\beta \cdot G_{vsat}^2}{G_{tot}} \left[ V_{G_T} + \frac{\Delta \psi^2}{12} - \xi \cdot \left( V_{G_T} - \frac{V_{inv_0} + V_{inv_L}}{2} \right) \right] \]  
(1.103)

\[ S_{th} = \frac{N_T}{G_{mob}^2} \cdot (R_{ideal} - T_{sat} \cdot I_{DS} \cdot \Delta \psi) \]  
(1.104)

\[ N_0 = \frac{\varepsilon_{ox}}{q t_{ox}} \cdot V_{inv_0} \]  
(1.105)

\[ N_L = \frac{\varepsilon_{ox}}{q t_{ox}} \cdot V_{inv_L} \]  
(1.106)

\[ N^* = \frac{\varepsilon_{ox}}{q t_{ox}} \cdot \xi \]  
(1.107)
\[ S_{fl} = \frac{q \cdot \phi_T^2 \cdot t_{ox} \cdot \beta \cdot I_{DS}}{f \cdot \varepsilon_{ox} \cdot G_{vsat} \cdot N^*} \cdot \left[(N_{FA} - N^* \cdot N_{FB} + N^{*2} \cdot N_{FC}) \cdot \ln \frac{N_0 + N^*}{N_L + N^*} + \right] \\
(\frac{N_{FB} - N^* \cdot N_{FC}}{(N_0 - N_L) + \frac{N_{FC}}{2} \cdot (N_0^2 - N_L^2)} \right] + \\
\frac{\phi_T \cdot I_{DS}^2}{f} \cdot (1 - G_{\Delta L}) \cdot \left[\frac{N_{FA} + N_{FB} \cdot N_L + N_{FC} \cdot N_{L}^2}{(N_L + N^*)^2} \right] \]

(1.108)

\[ S_{ig} = \begin{cases} \\
\frac{1}{3} \cdot N_T \cdot (2 \cdot \pi \cdot f \cdot C_{ox})^2 / g_m \\
1 + 0.075 \cdot (2 \cdot \pi \cdot f \cdot C_{ox} / g_m)^2 \\
0 \\
\end{cases} \]

GATENOISE = 0 \hspace{1cm} (1.109)

GATENOISE = 1

\[ \rho_{igth} = 0.4 \cdot j \]

(1.110)

\[ S_{igth} = \rho_{igth} \cdot \sqrt{S_{ig} \cdot S_{th}} \]

(1.111)
1.3 Symbols, parameters and constants

The symbolic representation and the recommended programming names of the quantities listed in the following sections, have been chosen in such a way to express their purpose and relations to other quantities and to preclude ambiguity and inconsistency.

1.3.1 Glossary of used symbols

All parameters which refer to the reference transistor and/or the reference temperature have a symbol with the subscript R and a programming name ending with R. All characters 0 (zero) in subscripts of parameters are represented by the capital letter O in the programming name, because often they are distinguishable with great difficulty! Scaling parameters are indicated by $S$ with a subscript where the variables on which the parameter depends, preceed a semicolon whereas the parameter succeeds it, e.g. $S_{T,\theta_{sr}}$.

List of input variables

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Prog. Name</th>
<th>Units</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L$</td>
<td>L</td>
<td>m</td>
<td>Drawn channel length in the lay-out of the actual transistor</td>
</tr>
<tr>
<td>$W$</td>
<td>W</td>
<td>m</td>
<td>Drawn channel width in the lay-out of the actual transistor</td>
</tr>
<tr>
<td>$T_A$</td>
<td>TA</td>
<td>°C</td>
<td>Ambient circuit temperature</td>
</tr>
<tr>
<td>$f$</td>
<td>F</td>
<td>s$^{-1}$</td>
<td>Operation frequency</td>
</tr>
</tbody>
</table>
External Electrical Variables

The definitions of the external electrical variables are illustrated in Figure 4.

### Variable Prog. Name Units Description

<table>
<thead>
<tr>
<th>Variable $V^{e}_{D}$</th>
<th>Prog. Name $VDE$</th>
<th>Units $V$</th>
<th>Description: Potential applied to the drain node</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V^{e}_{G}$</td>
<td>Prog. Name $VGE$</td>
<td>Units $V$</td>
<td>Description: Potential applied to the gate node</td>
</tr>
<tr>
<td>$V^{e}_{S}$</td>
<td>Prog. Name $VSE$</td>
<td>Units $V$</td>
<td>Description: Potential applied to the source node</td>
</tr>
<tr>
<td>$V^{e}_{B}$</td>
<td>Prog. Name $VBE$</td>
<td>Units $V$</td>
<td>Description: Potential applied to the bulk node</td>
</tr>
<tr>
<td>Variable</td>
<td>Prog. Name</td>
<td>Units</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>$I_D^e$</td>
<td>IDE</td>
<td>A</td>
<td>DC current into the drain</td>
</tr>
<tr>
<td>$I_G^e$</td>
<td>IGE</td>
<td>A</td>
<td>DC current into the gate</td>
</tr>
<tr>
<td>$I_S^e$</td>
<td>ISE</td>
<td>A</td>
<td>DC current into the source</td>
</tr>
<tr>
<td>$I_B^e$</td>
<td>IBE</td>
<td>A</td>
<td>DC current into the bulk</td>
</tr>
<tr>
<td>$Q_D^e$</td>
<td>QDE</td>
<td>C</td>
<td>Charge in the device attributed to the drain node</td>
</tr>
<tr>
<td>$Q_G^e$</td>
<td>QGE</td>
<td>C</td>
<td>Charge in the device attributed to the gate node</td>
</tr>
<tr>
<td>$Q_S^e$</td>
<td>QSE</td>
<td>C</td>
<td>Charge in the device attributed to the source node</td>
</tr>
<tr>
<td>$Q_B^e$</td>
<td>QBE</td>
<td>C</td>
<td>Charge in the device attributed to the bulk node</td>
</tr>
<tr>
<td>$S_D^e$</td>
<td>SDE</td>
<td>$A^2/s$</td>
<td>Spectral density of the noise current into the drain</td>
</tr>
<tr>
<td>$S_G^e$</td>
<td>SGE</td>
<td>$A^2/s$</td>
<td>Spectral density of the noise current into the gate</td>
</tr>
<tr>
<td>$S_S^e$</td>
<td>SSE</td>
<td>$A^2/s$</td>
<td>Spectral density of the noise current into the source</td>
</tr>
<tr>
<td>$S_{DG}^e$</td>
<td>SDGE</td>
<td>$A^2/s$</td>
<td>Cross spectral density between the drain and the gate noise currents</td>
</tr>
<tr>
<td>$S_{GS}^e$</td>
<td>SGSE</td>
<td>$A^2/s$</td>
<td>Cross spectral density between the gate and the source noise currents</td>
</tr>
<tr>
<td>$S_{SD}^e$</td>
<td>SSDE</td>
<td>$A^2/s$</td>
<td>Cross spectral density between the source and the drain noise currents</td>
</tr>
</tbody>
</table>
### Internal Electrical Variables

<table>
<thead>
<tr>
<th>Variable</th>
<th>Progr. Name</th>
<th>Units</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>VDS</td>
<td>V</td>
<td>Drain-to-source voltage applied to the equivalent n-MOST</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>VGS</td>
<td>V</td>
<td>Gate-to-source voltage applied to the equivalent n-MOST</td>
</tr>
<tr>
<td>$V_{SB}$</td>
<td>VSB</td>
<td>V</td>
<td>Source-to-bulk voltage applied to the equivalent n-MOST</td>
</tr>
<tr>
<td>$I_{DS}$</td>
<td>IDS</td>
<td>A</td>
<td>DC current through the channel flowing from drain to source</td>
</tr>
<tr>
<td>$I_{AVL}$</td>
<td>IAVL</td>
<td>A</td>
<td>DC current flowing from drain to bulk due to the weak-avalanche effect</td>
</tr>
<tr>
<td>$I_{GS}$</td>
<td>IGS</td>
<td>A</td>
<td>DC current flowing from gate to source due to the direct tunnelling effect</td>
</tr>
<tr>
<td>$I_{GD}$</td>
<td>IGD</td>
<td>A</td>
<td>DC current flowing from gate to drain due to the direct tunnelling effect</td>
</tr>
<tr>
<td>$I_{GB}$</td>
<td>IGB</td>
<td>A</td>
<td>DC current flowing from gate to bulk due to the direct tunnelling effect</td>
</tr>
<tr>
<td>$Q_{D}$</td>
<td>QD</td>
<td>C</td>
<td>Charge in the equivalent n-MOST attributed to the drain node</td>
</tr>
<tr>
<td>$Q_{G}$</td>
<td>QG</td>
<td>C</td>
<td>Charge in the equivalent n-MOST attributed to the gate node</td>
</tr>
<tr>
<td>$Q_{S}$</td>
<td>QS</td>
<td>C</td>
<td>Charge in the equivalent n-MOST attributed to the source node</td>
</tr>
<tr>
<td>$Q_{B}$</td>
<td>QB</td>
<td>C</td>
<td>Charge in the equivalent n-MOST attributed to the bulk node</td>
</tr>
<tr>
<td>$Q_{ov0}$</td>
<td>QOVO</td>
<td>C</td>
<td>Extrinsic charge in the equivalent n-MOST attributed to the gate-source overlap</td>
</tr>
<tr>
<td>$Q_{ovL}$</td>
<td>QOVL</td>
<td>C</td>
<td>Extrinsic charge in the equivalent n-MOST attributed to the gate-drain overlap</td>
</tr>
<tr>
<td>$S_{th}$</td>
<td>STH</td>
<td>$A^2 s$</td>
<td>Spectral density of the thermal-noise current of the channel</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>--------------------------------------</td>
<td>-------</td>
<td></td>
</tr>
<tr>
<td>$S_{fl}$</td>
<td>Spectral density of the flicker-noise current of the channel</td>
<td>$A^2s$</td>
<td></td>
</tr>
<tr>
<td>$S_{ig}$</td>
<td>Spectral density of the noise current induced in the gate</td>
<td>$A^2s$</td>
<td></td>
</tr>
<tr>
<td>$S_{igth}$</td>
<td>Cross spectral density of the noise current induced in the gate and the thermal-noise current of the channel</td>
<td>$A^2s$</td>
<td></td>
</tr>
</tbody>
</table>
1.3.2 Parameters

Parameters of the geometrical model

These parameters correspond to the geometrical model (MN, MP, MOS1100).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Progr. Name</th>
<th>Units</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEVEL</td>
<td>-</td>
<td></td>
<td>Must be 1100</td>
</tr>
<tr>
<td>PARAMCHK</td>
<td>-</td>
<td></td>
<td>Level of clip warning info *)</td>
</tr>
<tr>
<td>$L_{ER}$</td>
<td>LER</td>
<td>m</td>
<td>Effective channel length of the reference transistor</td>
</tr>
<tr>
<td>$W_{ER}$</td>
<td>WER</td>
<td>m</td>
<td>Effective channel width of the reference transistor</td>
</tr>
<tr>
<td>$\Delta L_{PS}$</td>
<td>LVAR</td>
<td>m</td>
<td>Difference between the actual and the programmed poly-silicon gate length</td>
</tr>
<tr>
<td>$\Delta L_{overlap}$</td>
<td>LAP</td>
<td>m</td>
<td>Effective channel length reduction per side due to the lateral diffusion of the source/drain dopant ions</td>
</tr>
<tr>
<td>$\Delta W_{OD}$</td>
<td>WVAR</td>
<td>m</td>
<td>Difference between the actual and the programmed field-oxide opening</td>
</tr>
<tr>
<td>$\Delta W_{narrow}$</td>
<td>WOT</td>
<td>m</td>
<td>Effective reduction of the channel width per side due to the lateral diffusion of the channel-stop dopant ions</td>
</tr>
<tr>
<td>$T_R$</td>
<td>TR</td>
<td>°C</td>
<td>Temperature at which the parameters for the reference transistor have been determined</td>
</tr>
<tr>
<td>$V_{FBR}$</td>
<td>VFBR</td>
<td>V</td>
<td>Flat-band voltage for the reference transistor at the reference temperature</td>
</tr>
<tr>
<td>$S_{T:V_{FBR}}$</td>
<td>STVFB</td>
<td>VK$^{-1}$</td>
<td>Coefficient of the temperature dependence $V_{FB}$</td>
</tr>
<tr>
<td>$k_{0R}$</td>
<td>KOR</td>
<td>V$^{1/2}$</td>
<td>Body-effect factor for the reference transistor</td>
</tr>
<tr>
<td>$S_{L:k_0}$</td>
<td>SLKO</td>
<td>V$^{1/2}$</td>
<td>Coefficient of the length dependence of $k_0$</td>
</tr>
<tr>
<td>$S_{L2:k_0}$</td>
<td>SL2KO</td>
<td>V$^{1/2}$</td>
<td>Second coefficient of the length dependence of $k_0$</td>
</tr>
<tr>
<td>Symbol</td>
<td>Program Name</td>
<td>Units</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>--------------</td>
<td>--------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>$S_{W,k_0}$</td>
<td>SWKO</td>
<td>$V^{1/2}$</td>
<td>Coefficient of the width dependence of $k_0$</td>
</tr>
<tr>
<td>$1/k_p$</td>
<td>KPINV</td>
<td>$V^{-1/2}$</td>
<td>Inverse of body-effect factor of the polysilicon gate</td>
</tr>
<tr>
<td>$\phi_{BR}$</td>
<td>PHIBR</td>
<td>$V$</td>
<td>Surface potential at the onset of strong inversion at the reference temperature</td>
</tr>
<tr>
<td>$S_{L,\phi_B}$</td>
<td>SLPHIB</td>
<td>$V_m$</td>
<td>Coefficient of the length dependence of $\phi_B$</td>
</tr>
<tr>
<td>$S_{L2,\phi_B}$</td>
<td>SL2PHIB</td>
<td>$V_m$</td>
<td>Second coefficient of the length dependence of $\phi_B$</td>
</tr>
<tr>
<td>$S_{W,\phi_B}$</td>
<td>SWPHIB</td>
<td>$V_m$</td>
<td>Coefficient of the width dependence of $\phi_B$</td>
</tr>
<tr>
<td>$\beta_{sq}$</td>
<td>BETSQ</td>
<td>$AV^{-2}$</td>
<td>Gain factor for an infinite square transistor at the reference temperature</td>
</tr>
<tr>
<td>$\eta_\beta$</td>
<td>ETABET</td>
<td>-</td>
<td>Exponent of the temperature dependence of the gain factor</td>
</tr>
<tr>
<td>$f_{\beta,1}$</td>
<td>FBET1</td>
<td>-</td>
<td>Relative mobility decrease due to first lateral profile</td>
</tr>
<tr>
<td>$L_{p,1}$</td>
<td>LP1</td>
<td>$m$</td>
<td>Characteristic length of first lateral profile</td>
</tr>
<tr>
<td>$f_{\beta,2}$</td>
<td>FBET2</td>
<td>-</td>
<td>Relative mobility decrease due to second lateral profile</td>
</tr>
<tr>
<td>$L_{p,2}$</td>
<td>LP2</td>
<td>$m$</td>
<td>Characteristic length of second lateral profile</td>
</tr>
<tr>
<td>$\theta_{srR}$</td>
<td>THESRR</td>
<td>$V^{-1}$</td>
<td>Coefficient of the mobility reduction due to surface roughness scattering for the reference transistor at the reference temperature</td>
</tr>
<tr>
<td>$S_{W,\theta_{sr}}$</td>
<td>SWTHESR</td>
<td>-</td>
<td>Coefficient of the width dependence of $\theta_{sr}$</td>
</tr>
<tr>
<td>$\theta_{phR}$</td>
<td>THEPHR</td>
<td>$V^{-1}$</td>
<td>Coefficient of the mobility reduction due to phonon scattering for the reference transistor at the reference temperature</td>
</tr>
<tr>
<td>$\eta_{ph}$</td>
<td>ETAPH</td>
<td>-</td>
<td>Exponent of the temperature dependence of $\theta_{ph}$ for the reference transistor</td>
</tr>
<tr>
<td>Symbol</td>
<td>Progr. Name</td>
<td>Units</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>$S_{W;\theta_{ph}}$</td>
<td>SWTHEPH</td>
<td>m</td>
<td>Coefficient of the width dependence of $\theta_{ph}$</td>
</tr>
<tr>
<td>$\eta_{mobR}$</td>
<td>ETAMOB</td>
<td>-</td>
<td>Effective field parameter for dependence on depletion/ inversion charge for the reference transistor</td>
</tr>
<tr>
<td>$S_{T;\eta_{mob}}$</td>
<td>STETAMOB</td>
<td>K$^{-1}$</td>
<td>Coefficient of the temperature dependence of $\eta_{mob}$</td>
</tr>
<tr>
<td>$S_{W;\eta_{mob}}$</td>
<td>SWETAMOB</td>
<td>m</td>
<td>Coefficient of the width dependence of $\eta_{mob}$</td>
</tr>
<tr>
<td>$\nu_R$</td>
<td>NUR</td>
<td>-</td>
<td>Exponent of the field dependence of the mobility model minus 1 (i.e. $\nu$-1) at the reference temperature</td>
</tr>
<tr>
<td>$\nu_{EXP}$</td>
<td>NUEXP</td>
<td>-</td>
<td>Exponent of the temperature dependence of parameter $\nu$</td>
</tr>
<tr>
<td>$\theta_{RR}$</td>
<td>THERR</td>
<td>$\nu^{-1}$</td>
<td>Coefficient of the series resistance for the reference transistor at the reference temperature</td>
</tr>
<tr>
<td>$\eta_R$</td>
<td>ETAR</td>
<td>-</td>
<td>Exponent of the temperature dependence of $\theta_R$</td>
</tr>
<tr>
<td>$S_{W;\theta_R}$</td>
<td>SWATHER</td>
<td>m</td>
<td>Coefficient of the width dependence of $\theta_R$</td>
</tr>
<tr>
<td>$\theta_{R1}$</td>
<td>THER1</td>
<td>V</td>
<td>Numerator of the gate voltage dependent part of series resistance for the reference transistor</td>
</tr>
<tr>
<td>$\theta_{R2}$</td>
<td>THER2</td>
<td>V</td>
<td>Denominator of the gate voltage dependent part of series resistance for the reference transistor</td>
</tr>
<tr>
<td>$\theta_{satR}$</td>
<td>THESATR</td>
<td>$\nu^{-1}$</td>
<td>Velocity saturation parameter due to optical/acoustic phonon scattering for the reference transistor at the reference temperature</td>
</tr>
<tr>
<td>$S_{L;\theta_{sat}}$</td>
<td>SLTHESAT</td>
<td>-</td>
<td>Coefficient of the length dependence of $\theta_{sat}$</td>
</tr>
<tr>
<td>$\theta_{satEXP}$</td>
<td>THESATEXP</td>
<td>-</td>
<td>Exponent of the length dependence of $\theta_{sat}$</td>
</tr>
<tr>
<td>Symbol</td>
<td>Prog. Name</td>
<td>Units</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>------------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>$\eta_{sat}$</td>
<td>ETASAT</td>
<td>-</td>
<td>Exponent of the temperature dependence of $\theta_{sat}$</td>
</tr>
<tr>
<td>$S_{W;\theta_{sat}}$</td>
<td>SWTHESAT</td>
<td>-</td>
<td>Coefficient of the width dependence of $\theta_{sat}$</td>
</tr>
<tr>
<td>$\theta_{ThR}$</td>
<td>THETHR</td>
<td>V^{-3}</td>
<td>Coefficient of self-heating for the reference transistor at the reference temperature</td>
</tr>
<tr>
<td>$\theta_{ThEXP}$</td>
<td>THETHEXP</td>
<td>-</td>
<td>Exponent of the length dependence of $\theta_{Th}$</td>
</tr>
<tr>
<td>$S_{W;\theta_{Th}}$</td>
<td>SWTHETH</td>
<td>m</td>
<td>Coefficient of the width dependence of $\theta_{Th}$</td>
</tr>
<tr>
<td>$\sigma_{dibl0}$</td>
<td>SDIBLO</td>
<td>V^{-1/2}</td>
<td>Drain-induced barrier-lowering parameter for the reference transistor</td>
</tr>
<tr>
<td>$\sigma_{diblEXP}$</td>
<td>SDIBLEXP</td>
<td>-</td>
<td>Exponent of the length dependence of $\sigma_{dibl}$</td>
</tr>
<tr>
<td>$m_{0R}$</td>
<td>MOR</td>
<td>-</td>
<td>Parameter for short-channel subthreshold slope for the reference transistor</td>
</tr>
<tr>
<td>$m_{0EXP}$</td>
<td>MOEXP</td>
<td>-</td>
<td>Exponent of the length dependence of $m_0$</td>
</tr>
<tr>
<td>$\sigma_{sfR}$</td>
<td>SSFR</td>
<td>V^{-1/2}</td>
<td>Static feedback parameter for the reference transistor</td>
</tr>
<tr>
<td>$S_{L;\sigma_{sf}}$</td>
<td>SLSSF</td>
<td>m</td>
<td>Coefficient of the length dependence of $\sigma_{sf}$</td>
</tr>
<tr>
<td>$S_{W;\sigma_{sf}}$</td>
<td>SWSSF</td>
<td>m</td>
<td>Coefficient of the width dependence of $\sigma_{sf}$</td>
</tr>
<tr>
<td>$\alpha_{R}$</td>
<td>ALPR</td>
<td>-</td>
<td>Factor of the channel length modulation for the reference transistor</td>
</tr>
<tr>
<td>$S_{L;\alpha}$</td>
<td>SLALP</td>
<td>-</td>
<td>Coefficient of the length dependence of $\alpha$</td>
</tr>
<tr>
<td>$\alpha_{EXP}$</td>
<td>ALPEXP</td>
<td>-</td>
<td>Exponent of the length dependence of $\alpha$</td>
</tr>
<tr>
<td>$S_{W;\alpha}$</td>
<td>SWALP</td>
<td>m</td>
<td>Coefficient of the width dependence of $\alpha$</td>
</tr>
<tr>
<td>$V_P$</td>
<td>VP</td>
<td>V</td>
<td>Characteristic voltage of the channel length modulation</td>
</tr>
<tr>
<td>$L_{min}$</td>
<td>LMIN</td>
<td>m</td>
<td>Minimum effective channel length in technology, used for calculation of smoothing factor $m$</td>
</tr>
<tr>
<td>Symbol</td>
<td>Progr. Name</td>
<td>Units</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>$a_{1R}$</td>
<td>A1R</td>
<td>-</td>
<td>Factor of the weak-avalanche current for the reference transistor at the reference temperature</td>
</tr>
<tr>
<td>$S_{T,a_1}$</td>
<td>STA1</td>
<td>K$^{-1}$</td>
<td>Coefficient of the temperature dependence of $a_1$</td>
</tr>
<tr>
<td>$S_{L,a_1}$</td>
<td>SLA1</td>
<td>m</td>
<td>Coefficient of the length dependence of $a_1$</td>
</tr>
<tr>
<td>$S_{W,a_1}$</td>
<td>SWA1</td>
<td>m</td>
<td>Coefficient of the width dependence of $a_1$</td>
</tr>
<tr>
<td>$a_{2R}$</td>
<td>A2R</td>
<td>V</td>
<td>Exponent of the weak-avalanche current for the reference transistor</td>
</tr>
<tr>
<td>$S_{L,a_2}$</td>
<td>SLA2</td>
<td>Vm</td>
<td>Coefficient of the length dependence of $a_2$</td>
</tr>
<tr>
<td>$S_{W,a_2}$</td>
<td>SWA2</td>
<td>Vm</td>
<td>Coefficient of the width dependence of $a_2$</td>
</tr>
<tr>
<td>$a_{3R}$</td>
<td>A3R</td>
<td>-</td>
<td>Factor of the drain-source voltage above which weak-avalanche occurs, for the reference transistor</td>
</tr>
<tr>
<td>$S_{L,a_3}$</td>
<td>SLA3</td>
<td>m</td>
<td>Coefficient of the length dependence of $a_3$</td>
</tr>
<tr>
<td>$S_{W,a_3}$</td>
<td>SWA3</td>
<td>m</td>
<td>Coefficient of the width dependence of $a_3$</td>
</tr>
<tr>
<td>$I_{GINVR}$</td>
<td>IGINVR</td>
<td>AV$^{-2}$</td>
<td>Gain factor for intrinsic gate tunnelling current in inversion for the reference transistor</td>
</tr>
<tr>
<td>$B_{Inv}$</td>
<td>BINV</td>
<td>V</td>
<td>Probability factor for intrinsic gate tunnelling current in inversion</td>
</tr>
<tr>
<td>$I_{GACCR}$</td>
<td>IGACCR</td>
<td>AV$^{-2}$</td>
<td>Gain factor for intrinsic gate tunnelling current in accumulation for the reference transistor</td>
</tr>
<tr>
<td>$B_{acc}$</td>
<td>BACC</td>
<td>V</td>
<td>Probability factor for intrinsic gate tunnelling current in accumulation</td>
</tr>
<tr>
<td>$V_{FBov}$</td>
<td>VFBOV</td>
<td>V</td>
<td>Flat-band voltage for the Source/Drain overlap extensions</td>
</tr>
<tr>
<td>$k_{ov}$</td>
<td>KOV</td>
<td>V$^{1/2}$</td>
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Remark: The parameters $L$, $W$, and $\Delta T_A$ are used to calculate the electrical parameters of the actual transistor, as specified in the section on parameter preprocessing.

*) See Appendix D for the definition of PARAMCHK

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## Default and clipping values (geometrical model)

The default values and clipping values as used for the parameters of the geometrical MOS model, level 11 (n-channel) are listed below.

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Parameters of the electrical model

These parameter correspond to the electrical model (MNE, MPE, MOS1100e).

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<td>Coefficient of the series resistance for the actual transistor at the actual temperature: $\theta_R = 2 \cdot \beta \cdot R_s$</td>
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*) Level of clip warning info must be 1100.
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### Note

The parameter $t_{\text{ox}}$ is used for calculation of the effective oxide thickness (due to quantum-mechanical effects) and the 1/f noise, not for the calculation of $\beta$ !!!
### Default and clipping values (electrical model)

The default values and clipping values as used for the parameters of the electrical MOS model, level 11 (n-channel) are listed below.

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### 1.3.3 Model constants

The following is a list of constants hardcoded in the model.

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<td>Offset for conversion from Celsius to Kelvin temperature scale (273.15)</td>
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<td>Q</td>
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<td>Elementary unit charge ($1.6021918 \cdot 10^{-19}$)</td>
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<td>Absolute permittivity of the oxide layer ($3.453143800 \cdot 10^{-11}$)</td>
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<td>Constant of quantum-mechanical behavior of electrons ($5.951993.10^{+00}$)</td>
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1.4 Parameter scaling

1.4.1 Geometrical scaling and temperature scaling

Calculation of Transistor Geometry

\[
L_E = L - \Delta L = L + \Delta L_{PS} - 2 \cdot \Delta L_{\text{overlap}}
\]

(1.112)

\[
W_E = W - \Delta W = W + \Delta W_{OD} - 2 \cdot \Delta W_{\text{narrow}}
\]

(1.113)

**WARNING:** \( L_E \) and \( W_E \) after calculation can not be less than \( 1.0 \times 10^{-9} \)! 

---

**Figure 5:** Specification of the dimensions of a MOS transistor
Calculation of Transistor Temperature

\( T_A \) is the ambient or the circuit temperature.

\[
T_{KR} = T_0 + T_R \tag{1.114}
\]

\[
T_{KD} = T_0 + T_A + \Delta T_A \tag{1.115}
\]

Calculation of Threshold-Voltage Parameters

\[
\tilde{V}_{FB} = V_{FBR} \tag{1.116}
\]

\[
K_0 = K_{0R} \cdot \left[ 1 + \left( \frac{1}{L_E} - \frac{1}{L_{ER}} \right) \cdot S_{L:K_0} + \left( \frac{1}{L_E^2} - \frac{1}{L_{ER}^2} \right) \cdot S_{L2:K_0} \right]. \tag{1.117}
\]

\[
\left[ 1 + \left( \frac{1}{W_E} - \frac{1}{W_{ER}} \right) \cdot S_{W:K_0} \right]
\]

\[
\phi_B = \phi_{BR} \cdot \left[ 1 + \left( \frac{1}{L_E} - \frac{1}{L_{ER}} \right) \cdot S_{L:\phi_B} + \left( \frac{1}{L_E^2} - \frac{1}{L_{ER}^2} \right) \cdot S_{L2:\phi_B} \right]. \tag{1.118}
\]

\[
\left[ 1 + \left( \frac{1}{W_E} - \frac{1}{W_{ER}} \right) \cdot S_{W:\phi_B} \right] \tag{1.119}
\]
Calculation of Mobility/Series-Resistance Parameters

\[ G_{P,E} = 1 + \beta_{1} \cdot \frac{L_{P,1}}{L_{E}} \left\{ 1 - \exp \left( \frac{L_{E}}{L_{P,1}} \right) \right\} + \]

\[ f_{\beta,2} \cdot \frac{L_{P,2}}{L_{E}} \left\{ 1 - \exp \left( \frac{L_{E}}{L_{P,2}} \right) \right\} \]  

(1.120)

\[ G_{P,R} = 1 + \beta_{1} \cdot \frac{L_{P,1}}{L_{ER}} \left\{ 1 - \exp \left( \frac{L_{ER}}{L_{P,1}} \right) \right\} + \]

\[ f_{\beta,2} \cdot \frac{L_{P,2}}{L_{ER}} \left\{ 1 - \exp \left( \frac{L_{ER}}{L_{P,2}} \right) \right\} \]  

(1.121)

\[ \tilde{\beta} = \frac{\beta_{sq}}{G_{P,E}} \cdot \frac{W_{E}}{L_{E}} \]  

(1.123)

\[ \tilde{\theta}_{sr} = \theta_{sr} \cdot \left[ 1 + \left( \frac{1}{W_{E}} - \frac{1}{W_{ER}} \right) \cdot S_{W;\theta_{sr}} \right] \]  

(1.124)

\[ \tilde{\theta}_{ph} = \theta_{ph} \cdot \left[ 1 + \left( \frac{1}{W_{E}} - \frac{1}{W_{ER}} \right) \cdot S_{W;\theta_{ph}} \right] \]  

(1.125)

\[ \tilde{\eta}_{mob} = \eta_{mob} \cdot \left[ 1 + \left( \frac{1}{W_{E}} - \frac{1}{W_{ER}} \right) \cdot S_{W;\eta_{mob}} \right] \]  

(1.126)
Calculation of Conductance Parameters

\[
\tilde{\theta}_R = \theta_{RR} \cdot \left[ 1 + \left( \frac{1}{W_E} - \frac{1}{W_{ER}} \right) \cdot S_{W;\theta_R} \right] \cdot \frac{L_{ER}}{L_E} \cdot \frac{G_{P,R}}{G_{P,E}} \quad (1.127)
\]

\[
\tilde{\theta}_{sat} = \theta_{satR} \cdot \left[ 1 + \left( \frac{1}{W_E} - \frac{1}{W_{ER}} \right) \cdot S_{W;\theta_{sat}} \right] \cdot \left[ 1 + S_L \cdot \left\{ \left( \frac{L_{ER}}{L_E} \right)^{\theta_{satEXP}} - 1 \right\} \right] \quad (1.128)
\]

Calculation of Sub-Threshold Parameters

\[
\tilde{\phi}_T = \frac{k_B \cdot T_{KR}}{q} \quad (1.132)
\]

\[
\sigma_{dibl} = \sigma_{dibl0} \cdot \left( \frac{L_{ER}}{L_E} \right)^{\sigma_{diblEXP}} \quad (1.133)
\]
\[ m_0 = m_{0R} \left( \frac{L_{ER}}{L_E} \right)^{m_{EXP}} \]  

(1.134)

**Calculation of Smoothing Parameters**

\[ L_{max} = 10 \cdot 10^{-6} \]  

(1.135)

\[
m = \frac{8 \cdot (L_{max} - L_{min})}{L_{max} - 4 \cdot L_{min} + 3 \cdot \frac{L_{max} \cdot L_{min}}{L_E}}
\]  

(1.136)

(\( m \) is rounded off to the nearest integer)

**Calculation of Weak-Avalanche Parameters**

\[
a_1 = \tilde{a}_1 + \left( \frac{1}{L_E} - \frac{1}{L_{ER}} \right) \cdot S_{L:a_1} + \left( \frac{1}{W_E} - \frac{1}{W_{ER}} \right) \cdot S_{W:a_1}
\]  

(1.137)

\[
a_2 = a_{2R} + \left( \frac{1}{L_E} - \frac{1}{L_{ER}} \right) \cdot S_{L:a_2} + \left( \frac{1}{W_E} - \frac{1}{W_{ER}} \right) \cdot S_{W:a_2}
\]  

(1.138)

\[
a_3 = a_{3R} + \left( \frac{1}{L_E} - \frac{1}{L_{ER}} \right) \cdot S_{L:a_3} + \left( \frac{1}{W_E} - \frac{1}{W_{ER}} \right) \cdot S_{W:a_3}
\]  

(1.139)

**Calculation of Gate Current Parameters**

\[
I_{GINV} = \frac{W_E \cdot L_E}{W_{ER} \cdot L_{ER}} \cdot I_{GINVR}
\]  

(1.140)
Calculation of Charge Parameters

\[ I_{GACC} = \frac{W_E \cdot L_E}{W_{ER} \cdot L_{ER}} \cdot I_{GACCR} \]  
(1.141)

\[ I_{GOV} = \frac{W_E \cdot L_E}{W_{ER} \cdot L_{ER}} \cdot I_{GOVR} \]  
(1.142)

Calculation of Noise Parameters

\[ c_{ox} = \varepsilon_{ox} \cdot \frac{W_E \cdot L_E}{t_{ox}} \]  
(1.143)

\[ C_{GD0} = W_E \cdot C_{ol} \]  
(1.144)

\[ C_{GS0} = W_E \cdot C_{ol} \]  
(1.145)

\[ \tilde{N}_T = N_{TR} \]  
(1.146)

\[ N_{FA} = \frac{W_{ER} \cdot L_{ER}}{W_E \cdot L_E} \cdot N_{FAR} \]  
(1.147)

\[ N_{FB} = \frac{W_{ER} \cdot L_{ER}}{W_E \cdot L_E} \cdot N_{FBR} \]  
(1.148)

\[ N_{FC} = \frac{W_{ER} \cdot L_{ER}}{W_E \cdot L_E} \cdot N_{FCR} \]  
(1.149)
1.4.2 Calculation of Temperature-Dependent Parameters

Calculation of Threshold-voltage Parameters

\[ V_{FB} = \tilde{V}_{FB} + (T_{KD} - T_{KR}) \cdot S_{T;V_{FB}} \] (1.150)

\[ S_{T;\phi_B} = \frac{\phi_{BR} - 1.13 - 2.5 \cdot 10^{-4} \cdot T_{KR}}{300} \] (1.151)

\[ \phi_B = \tilde{\phi}_B + (T_{KD} - T_{KR}) \cdot S_{T;\phi_B} \] (1.152)

Calculation of Mobility/Series-Resistance Parameters

\[ \beta = \tilde{\beta} \cdot \left( \frac{T_{KR}}{T_{KD}} \right)^{\eta_\beta} \] (1.153)

\[ \theta_{sr} = \begin{cases} 
\left( \tilde{\theta}_{sr} \cdot \left( \frac{T_{KR}}{T_{KD}} \right)^{\eta_\beta/2} \right) & \text{for NMOS} \\
\left( \tilde{\theta}_{sr} \cdot \left( \frac{T_{KR}}{T_{KD}} \right)^{\eta_\beta} \right) & \text{for PMOS} 
\end{cases} \] (1.154)

\[ \theta_{ph} = \tilde{\theta}_{phR} \cdot \left( \frac{T_{KD}}{T_{KR}} \right)^{3\eta_{ph} - 3\eta_\beta} \] (1.155)

\[ \eta_{mob} = \tilde{\eta}_{mob} \cdot [1 + (T_{KD} - T_{KR}) \cdot S_{T;\eta_{mob}}] \] (1.156)

\[ v = 1 + v_R \cdot \left( \frac{T_{KR}}{T_{KD}} \right)^{v_{exp}} \] (1.157)
\[ \theta_R = \tilde{\theta}_R \cdot \left( \frac{T_{KR}}{T_{KD}} \right)^{\eta_R} \]  

(1.158)

\[ \theta_{sat} = \tilde{\theta}_{sat} \cdot \left( \frac{T_{KR}}{T_{KD}} \right)^{\eta_{sat}} \]  

(1.159)

**Calculation of Conductance Parameters**

\[ \theta_{Th} = \tilde{\theta}_{Th} \cdot \left( \frac{T_{KR}}{T_{KD}} \right)^{\eta_{\beta}} \]  

(1.160)

**Calculation of Sub-Threshold Parameters**

\[ \phi_T = \frac{T_{KD}}{T_{KR}} \cdot \tilde{\phi}_T \]  

(1.161)

**Calculation of Weak-Avalanche Parameters**

\[ a_1 = \tilde{a}_1 \cdot [1 + (T_{KD} - T_{KR}) \cdot S_{T;a_1}] \]  

(1.162)

**Calculation of Noise Parameters**

\[ N_T = \frac{T_{KD}}{T_{KR}} \cdot \tilde{N}_T \]  

(1.163)
1.4.3 MULT scaling

The $N_{MULT}$ factor determines the number of equivalent parallel devices of a specified model. The $N_{MULT}$ factor has to be applied on the electrical parameters. Hence after the temperature scaling and other parameter processing. Some electrical parameters cannot be specified by the user as parameters but must always be computed from geometrical parameters. They are called electrical quantities here. The parameters: $\beta$, $I_{GINV}$, $I_{GACC}$, $I_{GOV}$, $C_{OX}$, $C_{GDO}$, $C_{GSO}$, $NF$, $NFA$, $NFB$ and $NFC$ are affected by the $N_{MULT}$ factor:

\[
\begin{align*}
\beta &= \beta \cdot N_{MULT} \\
I_{GINV} &= I_{GINV} \cdot N_{MULT} \\
I_{GACC} &= I_{GACC} \cdot N_{MULT} \\
I_{GOV} &= I_{GOV} \cdot N_{MULT} \\
C_{OX} &= C_{OX} \cdot N_{MULT} \\
C_{GDO} &= C_{GDO} \cdot N_{MULT} \\
C_{GSO} &= C_{GSO} \cdot N_{MULT} \\
N_{FA} &= \frac{N_{FA}}{N_{MULT}} \\
N_{FB} &= \frac{N_{FB}}{N_{MULT}} \\
N_{FC} &= \frac{N_{FC}}{N_{MULT}}
\end{align*}
\]

Convention:

No distinction is made between the symbol before and after the $N_{MULT}$ scaling, e.g: the symbol $\beta$ represents the actual parameter after the $N_{MULT}$ processing and temperature scaling. This parameter may be used to put several MOSTs in parallel.
1.5 Model Equations

Although the basic equations, given in section 1.2.2 on page 19, form a complete set of model equations, they are not yet suited for a circuit simulator. Several equations have to be adapted in order to obtain smooth transitions of the characteristics between adjacent regions of operation conditions and to prevent numerical problems during the iteration process for solving the network equations. In the following section a list of numerical adaptations and elucidations is given, followed by the extended set of model equations.

The definition of the hyp function, which provides for a smooth $C_\infty$-continuous clipping, is to be found in the Appendix A Hyp functions.

In the following sections, a function is denoted by $F\{variable, \ldots\}$, where $F$ denotes the function name and the function variables are enclosed by braces {}.

**Internal Parameters**

\[
\begin{align*}
\varepsilon_1 &= 2 \cdot 10^{-2} \quad \text{(1.164)} \\
\varepsilon_2 &= 1 \cdot 10^{-2} \quad \text{(1.165)} \\
\varepsilon_3 &= 4 \cdot 10^{-2} \quad \text{(1.166)} \\
\varepsilon_4 &= 1 \cdot 10^{-1} \quad \text{(1.167)} \\
\varepsilon_5 &= 1 \cdot 10^{-4} \quad \text{(1.168)} \\
P_D &= 1 + \left(\frac{k_0}{k_p}\right)^2 \quad \text{(1.169)} \\
V_{\text{limit}} &= 4 \cdot \phi_T \quad \text{(1.170)}
\end{align*}
\]
\[ \theta_{R_{\text{eff}}} = \frac{1}{2} \theta_R \cdot \left( 1 + \frac{\theta_{R1}}{1/2 + \theta_{R2}} \right) \]  
\[ (1.171) \]

\[ Acc = \left. \frac{\partial \psi_s}{\partial V_{GB}} \right|_{V_{GB} = V_{FB}} = \frac{1}{1 + k_0/(\sqrt{2} \cdot \phi_T)} \]  
\[ (1.172) \]

\[ N_{\phi_T} = \frac{(2.6)^2}{k_0} \]  
\[ (1.173) \]

\[ Acc_{ov} = \left. \frac{\partial \psi_{sov}}{\partial V_{GB}} \right|_{V_{GB} = V_{FBov}} = \frac{1}{1 + k_{ov}/(\sqrt{2} \cdot \phi_T)} \]  
\[ (1.174) \]

\[ QM_\psi = \begin{cases} QM_N \cdot (\varepsilon_{ox}/t_{ox})^{2/3} & \text{for NMOS} \\ QM_P \cdot (\varepsilon_{ox}/t_{ox})^{2/3} & \text{for PMOS} \end{cases} \]  
\[ (1.175) \]

\[ QM_{tox} = \frac{2}{5} \cdot QM_\psi \]  
\[ (1.176) \]

\[ \chi_{B_{\text{inv}}} = \begin{cases} \chi_{B_N} & \text{for NMOS} \\ \chi_{B_P} & \text{for PMOS} \end{cases} \]  
\[ (1.177) \]

\[ \chi_{B_{\text{acc}}} = \chi_{B_N} \]  
\[ (1.178) \]
1.5.1 Extended equations

Extended Current Equations

\[ V_{GB_{eff}} = \text{hyp}_1(V_{GS} + V_{SB} - V_{FB}; \varepsilon_1) \]  
\[ (1.179) \]

\[ V_{SB_i} = \text{hyp}_1(V_{SB} + 0.9 \cdot \phi_B; \varepsilon_2) + 0.1 \cdot \phi_B \]  
\[ (1.180) \]

\[ \psi_{sat_0} = \left( \frac{P_D \cdot V_{GB_{eff}}}{k_0^2/4 - k_0/2} \right)^2 \]  
\[ (1.181) \]

Drain induced barrier lowering and Static Feedback

\[ D_{dibl} = \sigma_{dibl} \cdot \sqrt{V_{SB_i}} \]  
\[ (1.182) \]

\[ D_{sf} = \sigma_{sf} \cdot \sqrt{\text{hyp}_1(\psi_{sat_0} - V_{SB_i}; \varepsilon_3)} \]  
\[ (1.183) \]

\[ D = D_{dibl} + \text{hyp}_1(D_{sf} - D_{dibl}; \sigma_{sf} \cdot \varepsilon_4) \]  
\[ (1.184) \]

\[ V_{DS_{eff}} = \frac{V_{DS}^4}{(V_{limit} + V_{DS}^2)^{3/2}} \]  
\[ (1.185) \]

\[ \Delta V_G = D \cdot V_{DS_{eff}} \]  
\[ (1.186) \]

Redefinition of \( V_{GB_{eff}} \), equation (1.179)

\[ V_{GB_{eff}} = \text{hyp}_1(V_{GS} + V_{SB} + \Delta V_G - V_{FB}; \varepsilon_1) \]  
\[ (1.187) \]
\[ \Delta_{acc} = \phi_T \cdot \left[ \exp \left( -\frac{A \cdot [V_{GB_{eff}} - \varepsilon_1]}{\phi_T} \right) - 1 \right] \] (1.188)

\[ \psi_{sat_1} = \left( \sqrt{\frac{P_D \cdot (V_{GB_{eff}} + \Delta_{acc}) + k_0^2/4 - k_0/2}{P_D}} \right)^2 - \Delta_{acc} \] (1.189)

**Drain Saturation Voltage:**

\[ V_{DSAT_{long}} = \psi_{sat_1} - V_{SB_t} \] (1.190)

\[ T_{sat} = \begin{cases} \theta_{sat} & \text{for NMOS} \\ \frac{\theta_{sat}}{(1 + \theta_{sat}^2 \cdot V_{DSAT_{long}}^2)^{1/4}} & \text{for PMOS} \end{cases} \] (1.191)

\[ \Delta_{SAT} = \frac{T_{sat} - \theta_{Reff}}{\sqrt{\frac{2}{V_{DSAT_{long}}^2 + \varepsilon_4}} + T_{sat}^2 + \theta_{Reff}} \] (1.192)

\[ V_{DSAT_{short}} = V_{DSAT_{long}} \cdot \left( 1 - \frac{9}{10} \cdot \frac{\Delta_{SAT}}{1 + \sqrt{1 - \Delta_{SAT}^2}} \right) \] (1.193)

\[ V_{DSAT} = V_{limit} + hyp_1(V_{DSAT_{short}} - V_{limit}; \varepsilon_3) \] (1.194)

\[ V_{DS} = \frac{V_{DS} \cdot V_{DSAT}}{\left[ V_{DS}^{2m} + V_{DSAT}^{2m} \right]^{1/(2 \cdot m)}} \] (1.195)
\[ V_{DB_t} = \text{hyp}_1(V_{DSx} + V_{SB} + 0.9 \cdot \phi_B; \varepsilon_2) + 0.1 \cdot \phi_B \]  

(1.196)

**Surface Potential:**

\[ f_1\{\psi\} = \psi_{sat} - \text{hyp}_1\{\psi_{sat} - \psi; \varepsilon_1\} \]  

(1.197)

\[ f_2\{\psi\} = f_1\{\psi\} + \frac{\psi_{sat} - f_1\{\psi\}}{\sqrt{1 + \frac{[\psi_{sat} - f_1\{\psi\}]^2}{N\phi_T \cdot \phi_T^2}}} \]  

(1.198)

\[ f_3\{\psi\} = \frac{2 \cdot [V_{GB_{eff}} - f_2\{\psi\}]}{1 + \sqrt{1 + 4/k_p^2 \cdot [V_{GB_{eff}} - f_2\{\psi\}]}} \]  

(1.199)

\[ \psi_{s_{inv}}\{\psi\} = f_1\{\psi\} + \phi_T \cdot [1 + m_0] \cdot \ln \left[ \frac{\left(\frac{f_3\{\psi\}}{k_0}\right)^2 - f_1\{\psi\} - \Delta_{acc} + \phi_T}{\phi_T} \right] \]  

(1.200)

\[ \psi_{s0}^* = \psi_{s_{inv}} \cdot \{V_{SB_t}\} \]  

(1.201)

\[ \psi_{sL}^* = \psi_{s_{inv}} \cdot \{V_{DB_t}\} \]  

(1.202)

**Surface Potential in Accumulation:**

\[ f_1 = \text{Acc} \cdot [V_{GS} + V_{SB} + \Delta V_G - V_{FB} - V_{GB_{eff}}] \]  

(1.203)
$f_2 = \sqrt[2]{\sqrt{\frac{f_1^2}{1 + \frac{f_1^2}{N_{\phi_T} \cdot \phi_T^2}}}}$ (1.204)

$\psi_{s_{acc}} = -\phi_T \cdot \ln \left[ \frac{\left\{ f_1 / (Acc) - f_2 \right\}^2}{k_0} - f_2 + \phi_T \right] \phi_T$ (1.205)

**Auxiliary Variables:**

$\Delta \psi = \psi^*_S - \psi^*_S$ (1.206)

$\bar{\psi}_{inv} = \frac{\psi^*_S + \psi^*_S}{2}$ (1.207)

$V_{GT} \{\psi_{s_{inv}}\} = \frac{2 \cdot [V_{GB_{eff}} - \psi_{s_{inv}}]}{1 + \sqrt{1 + 4k_p^2 \cdot [V_{GB_{eff}} - \psi_{s_{inv}}]}} - k_0 \cdot \sqrt{\text{hyp1} \{\psi_{s_{inv}} + \Delta_{acc} ; \varepsilon_2\}}$ (1.208)

$V_{GT_0} = \text{hyp1} \left\{ V_{GT} \left\{ \psi^*_S \right\} ; \varepsilon_5 \right\}$ (1.209)
\[ V_{GT_L} = \text{hyp}_1 \left\{ V_{G_T} \left\{ \psi_{s_L}^* \right\}; \varepsilon_5 \right\} \]  

(1.210)

\[ \bar{V}_{G_T} = V_{G_T} \{ \psi_{inv} \} \]  

(1.211)

\[ V_{ox} = \frac{2 \cdot [V_{GS} + V_{SB} + \Delta V_G - V_{FB} - \psi_{inv} - \psi_{acc}]}{1 + \sqrt{1 + 4/k_p^2 \cdot [V_{GB_{eff}} - \psi_{inv}]}} \]  

(1.212)

\[ \partial V_{ox} = \frac{2}{1 + \sqrt{1 + 4/k_p^2 \cdot [V_{GB_{eff}} - \psi_{inv}]}} \]  

(1.213)

\[ V_{eff} = \bar{V}_{G_T} + \eta_{mob} \cdot (V_{ox} - \bar{V}_{G_T}) \]  

(1.214)

\[ \xi = \phi_T \cdot \left[ \frac{1}{\sqrt{1 + 4/k_p^2 \cdot [V_{GB_{eff}} - \psi_{inv}]}} + \frac{k_0}{2 \cdot \text{hyp}_1 \{ \psi_{inv} + \Delta_{acc} ; \varepsilon_5 \}} \right] \]  

(1.215)

\[ \bar{V}_{G_T}^* = \frac{V_{GT_0} + V_{GT_L}}{2} + \xi \]  

(1.216)
Second-Order Effects

Mobility Degradation:

\[ V_{\text{eff}, 1} = \text{hyp}_1 (V_{\text{eff}, 2} : \varepsilon_2) \]  

\[ G_{\text{mob}} = \frac{\mu_0}{\mu} = \begin{cases} \frac{1 + \left[ (\theta_{\text{ph}} \cdot V_{\text{eff}, 1})^{v/3} + (\theta_{\text{sr}} \cdot V_{\text{eff}, 1})^{2v} \right]^{1/v}}{1 + \left[ (\theta_{\text{ph}} \cdot V_{\text{eff}, 1})^{v/3} + (\theta_{\text{sr}} \cdot V_{\text{eff}, 1})^{v} \right]^{1/v}} & \text{for NMOS} \\ \end{cases} \]  

\[ G_{\text{mob}} = \begin{cases} \frac{1 + \left[ (\theta_{\text{ph}} \cdot V_{\text{eff}, 1})^{v/3} + (\theta_{\text{sr}} \cdot V_{\text{eff}, 1})^{v} \right]^{1/v}}{1 + \left[ (\theta_{\text{ph}} \cdot V_{\text{eff}, 1})^{v/3} + (\theta_{\text{sr}} \cdot V_{\text{eff}, 1})^{v} \right]^{1/v}} & \text{for PMOS} \\ \end{cases} \]

\[ x = \begin{cases} \frac{2 \cdot \theta_{\text{sat}} \cdot \Delta \psi}{\sqrt{G_{\text{mob}}}} & \text{for NMOS} \\ \frac{2 \cdot \theta_{\text{sat}} \cdot \Delta \psi}{\sqrt{G_{\text{mob}}}} (1 + \theta_{\text{sat}}^2 \cdot \Delta \psi^2)^{1/4} & \text{for PMOS} \\ \end{cases} \]  

Velocity Saturation:

\[ G_{\text{vsat}} = \begin{cases} \frac{G_{\text{mob}}}{2} \cdot \left[ \sqrt{1 + x^2} + 1 - \frac{x^2}{6} \right] & x < 1 \cdot 10^{-4} \\ \frac{G_{\text{mob}}}{2} \cdot \left[ \sqrt{1 + x^2} + \ln \left( x + \sqrt{1 + x^2} \right) \right] & x \geq 1 \cdot 10^{-4} \\ \end{cases} \]

Channel Length Modulation:

\[ G_{\Delta L} = \text{hyp}_1 \left( 1 - \alpha \cdot \ln \left[ \frac{V_{DS} - V_{DS_s} + \sqrt{(V_{DS} - V_{DS_s})^2 + V^2}}{V_P} \right] : \varepsilon_5 \right) \]
Series Resistance and Self-Heating:

\[ G_R = \theta_R \cdot \left( 1 + \frac{\theta_{R1}}{\theta_{R2} + \overline{V}_{G_T}} \right) \cdot \overline{V}_{G_T} \]  \hspace{1cm} (1.222) 

\[ G_{Th} = \theta_{Th} \cdot V_{DS} \cdot \Delta \psi \cdot \overline{V}_{G_T} \]  \hspace{1cm} (1.223) 

\[ G_{tot} = G_{Th} + \frac{[G_{\Delta L} \cdot G_{vSat} + G_R]}{2} \]  \hspace{1cm} (1.224) 

\[ \left[ 1 + \sqrt[4]{\text{hyp}_1 \left( 1 - \frac{4 \cdot G_R / G_{vSat}}{G_{\Delta L} \cdot G_{vSat} + G_R} \cdot \left[ G_{vSat}^2 - G_{mob}^2 ; \epsilon_5 \right] \right)} \right] \]

Inversion-Layer Charge

\( Q_{inv} = -\epsilon_{ox} / t_{ox} \cdot V_{inv} \) : 

\[ \psi_{s_{inv}}^* \{ \psi_{s_{inv}} \} = \text{hyp}_1 (\psi_{s_{inv}} + \Delta_{acc} ; \epsilon_5) \]  \hspace{1cm} (1.225) 

\[ V_{inv} \{ \psi_{s_{inv}} , \psi \} = \frac{k_0 \cdot \phi_T \cdot \exp \left[ \frac{\psi_{s_{inv}} - \psi}{(1 + m_0) \cdot \phi_T} \right]} {\sqrt[4]{\psi_{s_{inv}}^* \{ \psi_{s_{inv}} \} + \phi_T \cdot \exp \left[ \frac{\psi_{s_{inv}} - \psi}{(1 + m_0) \cdot \phi_T} \right] + \sqrt[4]{\psi_{s_{inv}}^* \{ \psi_{s_{inv}} \}}} + \sqrt[4]{\psi_{s_{inv}}^* \{ \psi_{s_{inv}} \} \cdot \phi_T \cdot \exp \left[ \frac{\psi_{s_{inv}} - \psi}{(1 + m_0) \cdot \phi_T} \right] + \sqrt[4]{\psi_{s_{inv}}^* \{ \psi_{s_{inv}} \} \right]} \]  \hspace{1cm} (1.226)
\[ V_{inv_o} = V_{inv} \left\{ \phi_{s_0}^*, V_{SB_i} \right\} \] (1.227)

\[ V_{inv_L} = V_{inv} \left\{ \phi_{s_L}^*, V_{DB_i} \right\} \] (1.228)

**Drain Current**

\[ x_0 = \frac{2}{\phi_T} \left( \psi_{sat_1} + \phi_T - V_{SB_i} \right) \] (1.229)

\[ x_L = \frac{2}{\phi_T} \left( \psi_{sat_1} + \phi_T - V_{DB_i} \right) \] (1.230)

\[ G = \frac{\exp(x_0) + \exp(x_L)}{\exp(x_0) + \exp(x_L) + 1} \] (1.231)

\[ I_{drift} = \begin{cases} 
\beta \cdot \bar{V}_G \cdot \Delta \psi & \text{if } x_0 > 80 \text{ or } x_L > 80 \\
\beta \cdot \bar{V}_G \cdot \Delta \psi \cdot G & \text{if } x_0 \leq 80 \text{ and } x_L \leq 80 
\end{cases} \] (1.232)

\[ I_{diff} = \beta \cdot \phi_T \cdot (V_{inv_o} - V_{inv_L}) \] (1.233)

\[ I_{DS} = \frac{I_{drift} + I_{diff}}{G_{tot}} \] (1.234)
Weak-Avalanche

\[
I_{avl} = \begin{cases} 
0 & V_{DS} \leq a_3 \cdot V_{DSAT} \\
 a_1 \cdot I_{DS} \cdot \exp \left( -\frac{a_2}{V_{DS} - (a_3 \cdot V_{DSAT})} \right) & V_{DS} > a_3 \cdot V_{DSAT} 
\end{cases}
\] (1.235)

Gate Current Equations

The tunnelling probability is given by:

\[
P_{\text{tun}}\{V_{ox}, \chi_B; B\} = \begin{cases} 
\exp \left( -\frac{B}{\chi_B} \cdot \frac{\left( \frac{V_{ox}}{\chi_B} \right)^2 \cdot 3 \cdot \frac{V_{ox}}{\chi_B} + 3}{1 + \left( 1 - \frac{V_{ox}}{\chi_B} \right)^{3/2}} \right) & V_{ox} < \chi_B \\
\exp(-B/V_{ox}) & V_{ox} \geq \chi_B 
\end{cases}
\] (1.236)

Source/Drain Gate Overlap Current:

First calculate the oxide voltage \( V_{ov} \) at both Source and Drain overlap:

\[
V_{G_{\text{eff}}}\{V_{GX}\} = V_{GX} - V_{FBo} - \text{hyp}_1 (V_{GX} - V_{FBo}, \varepsilon_1) 
\] (1.237)

\[
\Delta_{ov}\{V_{GX}\} = \phi_T \cdot \exp \left( \frac{A_{cc_{ov}} \cdot \left[ V_{GX_{eff}}\{V_{GX}\} + \varepsilon_1 \right]}{\phi_T} \right) - 1 
\] (1.238)

\[
\psi_{sat_{ov}}\{V_{GX}\} = -\sqrt{\frac{k_{ov}^2}{4} - V_{G_{\text{eff}}}\{V_{GX}\} + \Delta_{ov}\{V_{GX}\} - \frac{k_{ov}}{2}^2} + \Delta_{ov}\{V_{GX}\} 
\] (1.239)
Next calculate the gate tunnelling current in both Source and Drain overlap:

\[
P_{ov}(V_{ov}) = P_{tun}\{V_{ov}; \chi_{B_{inv}}; B_{inv}\} \tag{1.247}
\]
Intrinsic Gate Current

The gate tunnelling current in accumulation:

\[ I_{Gov}(V_{GX}, V_{ov}) = I_{GOV} \cdot V_{GX} \cdot V_{ov} \cdot \left[ P_{ov}(V_{ov}) - P_{ov}(-V_{ov}) \right] \] (1.248)

\[ I_{Gov_0} = I_{Gov}(V_{GS}, V_{ov_0}) \] (1.249)

\[ I_{Gov_L} = I_{Gov}(V_{GS} - V_{DS}, V_{ov_L}) \] (1.250)

The gate tunnelling current in inversion, including quantum-mechanical barrier lowering \( \Delta \chi_B \):

\[ \Delta \chi_B = QM_{\psi} \cdot \left[ (\overline{V}_{GT}/3 + V_{ox} - \overline{V}_{GT})^2 + V_{\text{limit}}^2 \right]^{1/3} \] (1.254)

\[ \chi_{B_{\text{eff}}} = 0.7 \cdot \chi_{B_{\text{inv}}} + \text{hyp}_1(0.3 \cdot \chi_{B_{\text{inv}}} - \Delta \chi_B; \varepsilon_5) \] (1.255)

\[ B_{\text{eff}} = B_{\text{inv}} \cdot \left( \chi_{B_{\text{eff}}} / \chi_{B_{\text{inv}}} \right)^{3/2} \] (1.256)

\[ P_{\text{inv}} = P_{\text{tun}}(V_{ox} ; \chi_{B_{\text{eff}}} ; B_{\text{eff}}) \] (1.257)

\[ B_{\text{inv}}^* = \frac{3}{8} \cdot \chi_{B_{\text{eff}}}^{-2} \cdot B_{\text{eff}} \cdot \partial V_{ox} \] (1.258)
The total intrinsic gate current $I_{GC}$:

$$I_{GC} = \bar{I}_{GC} \cdot \bar{V}_{inv} \cdot P_{GC}$$  \hspace{1cm} (1.264)$$

$$P_{GS} = \left[ B_{inv}^* + \partial V_{ox}^* \right] \cdot \frac{\Delta \psi}{12} + \left[ (B_{inv}^*)^2 \cdot (B_{inv}^* + 5 \cdot \xi^* + 3 \cdot \partial V_{ox}^*) + 2 \cdot \xi^{*2} \cdot (B_{inv}^* - \xi^* + \partial V_{ox}^*) + 10 \cdot B_{inv}^* \cdot \xi^* \cdot \partial V_{ox}^* \right] \cdot \frac{\Delta \psi^3}{480}$$  \hspace{1cm} (1.265)$$

$$\xi^* = \frac{\xi^*}{\phi_T \cdot \bar{V}_{Gr}}$$  \hspace{1cm} (1.259)$$

$$\partial V_{ox}^* = \frac{\partial V_{ox}}{\sqrt{V_{ox}^{2} + V_{\text{limit}}^{2}}}$$  \hspace{1cm} (1.260)$$

$$P_{GC} = 1 + \frac{\left[ (B_{inv}^*)^2 + 4 \cdot B_{inv}^* \cdot \xi^* + 2 \cdot B_{inv}^* \cdot \partial V_{ox}^* + 2 \cdot \xi^{*2} + 4 \cdot \partial V_{ox}^* \cdot \xi^* \right] \cdot \Delta \psi^2}{24}$$  \hspace{1cm} (1.261)$$

$$\bar{I}_{GC} = I_{GINV} \cdot G_{\Delta L} \cdot \left( V_{GS} - \frac{1}{2} \cdot V_{DS} \right) \cdot P_{inv}$$  \hspace{1cm} (1.262)$$

$$\bar{V}_{inv} = \frac{V_{inv_0} + V_{inv_1}}{2}$$  \hspace{1cm} (1.263)$$
\[ I_{GS} = \frac{1}{2} \cdot I_{GC} + \left( P_{GS} \cdot \bar{V}_{inv} + \frac{V_{inv0} - V_{invL}}{12} \right) \cdot I_{GC} + I_{Gov0} \]  

(1.266)

\[ I_{GD} = I_{GC} - I_{GS} + I_{Gov0} + I_{GovL} \]  

(1.267)

Extended Charge Equations

Bias-Dependent Overlap Capacitance:

\[ Q_{ov0} = C_{GSO} \cdot V_{ov0} \]  

(1.268)

\[ Q_{ovL} = C_{GDO} \cdot V_{ovL} \]  

(1.269)

Intrinsic Charges:

\[ C_{ox,eff} = \frac{C_{ox}}{1 + QM_{t_{ox}} \cdot \left[ \left( \frac{V_{eff}}{\eta_{mob}} \right)^2 + (20 \cdot \phi_T)^2 \right]^{-1/6}} \]  

(1.270)

\[ \Delta V_{GT} = \frac{V_{GT0} - V_{GT_L}}{2 \cdot \left( 1 + \theta_R \cdot \frac{\bar{V}_{G_T}}{G_{tot}} \right)} \]  

(1.271)

\[ F_j = \frac{\Delta V_{GT}}{\bar{V}_{G_T}} \]  

(1.272)

\[ Q_S = \frac{C_{ox,eff}}{2} \cdot \left[ \bar{V}_{G_T}^* + \frac{\Delta V_{G_T}}{3} \cdot \left( F_j - \frac{F_j^2}{5} + 1 \right) - \xi \right] \]  

(1.273)
Extended Noise Equations

In these equations \( f \) represents the operation frequency of the transistor.

\[
Q_D = -\frac{C_{ox, eff}}{2} \cdot \left[ \overline{V}^*_{G_T} + \frac{\Delta V_{G_T}}{3} \cdot \left( F\delta + \frac{F^2\delta}{5} - 1 \right) - \xi \right] \tag{1.274}
\]

\[
Q_B = -C_{ox, eff} \cdot [V_{ox} - \overline{V}^*_{G_T} + \xi] \tag{1.275}
\]

\[
Q_G = -[Q_S + Q_D + Q_B] \tag{1.276}
\]

\[
g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \tag{1.277}
\]

\[
T_{sat} = \begin{cases} 
\frac{\theta_{sat}^2}{\sqrt{1 + \theta_{sat}^2 \cdot \Delta\psi^2}} & \text{for PMOS} \\
\theta_{sat}^2 & \text{for NMOS}
\end{cases} \tag{1.278}
\]

\[
R_{ideal} = \frac{\beta_T \cdot G_{vsat}^2}{G_{tot}} \cdot \left[ \frac{V_{inv_0} + V_{inv_l}}{2} + \frac{(V_{inv_0} - V_{inv_l})^2}{12 \cdot \left( \frac{V_{inv_0} + V_{inv_l}}{2} + \xi \right)} \right] \tag{1.279}
\]
\[ S_{th} = \begin{cases} 0 \\ \frac{N_T}{G_{mob}} \cdot (R_{ideal} - T_{sat} \cdot I_{DS} \cdot \Delta \psi) & \quad R_{ideal} \leq T_{sat} \cdot I_{DS} \cdot \Delta \psi \\ \frac{N_T}{G_{mob}} \cdot (R_{ideal} - T_{sat} \cdot I_{DS} \cdot \Delta \psi) & \quad R_{ideal} > T_{sat} \cdot I_{DS} \cdot \Delta \psi \end{cases} \] (1.280)

\[ N_0 = \frac{\varepsilon_{ox}}{q t_{ox}} \cdot V_{inv_0} \] (1.281)

\[ N_L = \frac{\varepsilon_{ox}}{q t_{ox}} \cdot V_{inv_L} \] (1.282)

\[ N^* = \frac{\varepsilon_{ox}}{q t_{ox}} \cdot \xi \] (1.283)

\[ S_{fl} = \frac{q \cdot \phi_T^2 \cdot t_{ox} \cdot \beta \cdot I_{DS}}{f \cdot \varepsilon_{ox} \cdot G_{vsat} \cdot N^*_0} \cdot \left[ (N_{FA} - N^* \cdot N_{FB} + N^{*2} \cdot N_{FC}) \cdot \ln \frac{N_0 + N^*}{N_L + N^*} + (N_{FB} - N^* \cdot N_{FC}) \cdot (N_0 - N_L) + \frac{N_{FC}}{2} \cdot (N_0^2 - N_L^2) \right] + \frac{\phi_T \cdot I_{DS}^2}{f} \cdot (1 - G_{\Delta L}) \cdot \left[ \frac{N_{FA} + N_{FB} \cdot N_L + N_{FC} \cdot N_L^2}{(N_L + N^*_L)^2} \right] \] (1.284)
1.5.2 Numerical adaptations

The implemented electrical equations of MOS Model 11 are essentially based on the physical description given in section 1.2 on page 5. The following numerical adaptations have been made in order to obtain smooth transitions and prevent numerical problems, leading to the equations given in section 1.5 on page 71:

- The piece-wise eqs. (1.11) and (1.19) for \( V_{GB_{eff}} \), (1.14) for \( D_{sf} \), (1.15) for \( D \), (1.22) for \( V_{DSAT_{long}} \), (1.25) for \( V_{DSAT} \), (1.27), (1.33) and (1.65) for different functions \( f_1 \), (1.62) for \( V_{GX_{eff}} \) and (1.77) for \( I_{GB} \) have been replaced by smooth \( C_{\infty} \)-continuous functions based on hyp-functions.

- Expression (1.13), describing the drain-induced barrier lowering effect, has no numerical solution for \( V_{SB} + \phi_B < 0 \). In order to solve this problem the expression \( V_{SB} + \phi_B \) is clipped at a minimum value of \( 0.1 \cdot \phi_B \) using eq. (1.180). In order to maintain symmetry (with respect to source and drain), the same method must be applied to the drain side, this is done in eq. (1.196).

- The effective voltage \( V_{eff} \) given by eq. (1.214) becomes negative in the accumulation region, which leads to strange behaviour in the mobility reduction expression (1.47). In order to prevent \( V_{eff} \) from becoming negative, a hyp-smoothing function is used in the actual implementation, see eq. (1.217).
• The theoretical velocity saturation expression (1.49) results in zero divided by zero for \( V_{DS} = 0 \). This numerical problem has been circumvented by replacing this expression by a third-order Taylor polynomial for small values of \( V_{DS} \), see eq. (1.220).

• The theoretical channel length modulation expression (1.50) can become negative for high values of \( \alpha \) and \( V_{DS} \). This corresponds to a negative effective channel length, which is not physical. In order to prevent \( G_{\Delta L} \) from becoming negative, a hyp-smoothing function is used in the actual implementation, see eq. (1.221).

• The term in the square root of eq. (1.53) can become negative for very high values of parameter \( \theta_R \), which would result in numerical errors. This has been prevented in the actual implementation (1.224) by using a hyp-smoothing function.

• The term \( \psi_{\text{kin}} + \Delta_{\text{acc}} \) in expression (1.54) may become negative in accumulation for certain parameter values. Since a square root is taken of this term, it has to be prevented that the above term becomes negative; this has been done using a hyp-smoothing function (1.225) in eq. (1.226). The same type of problem occurs in eq. (1.45) for variable \( \xi \), it has been circumvented in the same way, see eq. (1.215).

• Theoretically, in subthreshold, the drift current given by eq. (1.57) is much smaller than the diffusion current, due to the term \( \Delta \psi \) which rapidly approaches zero for decreasing gate bias. Owing to the approximations made in the calculation of surface potential in MOS Model 11, for certain conditions \( \Delta \psi \) may not go to zero rapidly enough. As a result the drift current is forced to very small values in subthreshold by making use of eqs. (1.229) to (1.232).

• The exponent in the tunnelling probability \( P_{\text{tun}} \), given by eq. (1.61), results in zero divided by zero for \( V_{ox} = 0 \). By simply rewriting the exponent, this problem can be circumvented as has been done in eq. (1.236).

• The expression of effective oxide barrier lowering \( \Delta \chi_B \), given by eq. (1.78), can become equal to zero (at \( V_{GB} = V_{FB} \)), resulting in numerical errors in the first-order derivatives of \( \Delta \chi_B \) to the terminal voltages. In order to prevent \( \Delta \chi_B \) from becoming zero, eq. (1.254) has been used.

• For very high gate bias values, which could occur during the iteration process of the circuit simulator, the expression of effective oxide barrier \( \chi_{B,\text{eff}} \), given by eq. (1.79), can
become zero or negative resulting in numerical errors. In order to prevent this problem $\chi_{B_{eff}}$ is clipped at a minimum (arbitrary) value of $0.7 \cdot \chi_{B_{inv}}$ using a hyp-smoothing function, see eq. (1.255).

- The expression of $\partial V_{ox}^*$, given by eq. (1.84), gives numerical problems when the oxide voltage $V_{ox}$ is equal to zero. This problem has been circumvented by replacing $V_{ox}$ by $\sqrt{V_{ox}^2 + V_{limit}^2}$, see eq. (1.260).

- The expression of effective oxide capacitance (1.94) due to quantum-mechanical effects gives erroneous results for $V_{eff} = 0$ (i.e. $V_{GB} = V_{FB}$). This can be prevented by replacing $V_{eff}/\eta_{mob}$ by $\sqrt{(V_{eff}/\eta_{mob})^2 + (20 \cdot \phi_T)^2}$, where the value of $20 \cdot \phi_T$ is rather arbitrary but it nevertheless ensures a smooth transition from accumulation to depletion/inversion.

- The effective gate bias $V_{GT}$ may become negative in deep cubthreshold, resulting in inaccurate results in expression (12.103) for $R_{ideal}$. In order to prevent this, $R_{ideal}$ is clipped to zero in these cases, see eq. ***(11.279)***.

- The thermal noise spectral density $S_{th}$ given by eq. (12.104) can become negative for very high values of parameter $\theta_{sat}$, which is not physical. In order to prevent this, $S_{th}$ is clipped to zero in these cases, see eq. ***(11.280)***.
1.6 DC Operating point

The DC operating point output facility gives information on the state of a device at its operation point. Besides terminal currents and voltages, the magnitudes of linearized internal elements are given. In some cases meaningful quantities can be derived which are then also given (e.g. $f_T$). The objective of the DC operating-facility is twofold:

- Calculate small-signal equivalent circuit element values.
- Open a window on the internal bias conditions of the device and its basic capabilities.

Below the printed items are described. $C_{xy}$ indicates the derivate of the charge $Q$ at terminal $x$ to the voltage at terminal $y$, when all other terminals remain constant. When the parameter

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Program Name</th>
<th>Units</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DS}$</td>
<td>IDS</td>
<td>A</td>
<td>Drain current, excl. avalanche and tunnel currents.</td>
</tr>
<tr>
<td>$I_{avl}$</td>
<td>IAVL</td>
<td>A</td>
<td>Substrate current due to weak-avalanche</td>
</tr>
<tr>
<td>$I_{GS}$</td>
<td>IGS</td>
<td>A</td>
<td>Gate-to-source current due to direct tunnelling</td>
</tr>
<tr>
<td>$I_{GD}$</td>
<td>IGD</td>
<td>A</td>
<td>Gate-to-drain current due to direct tunnelling</td>
</tr>
<tr>
<td>$I_{GB}$</td>
<td>IGB</td>
<td>A</td>
<td>Gate-to-bulk current due to direct tunnelling</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>VDS</td>
<td>V</td>
<td>Drain-Source voltage</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>VGS</td>
<td>V</td>
<td>Gate-Source voltage</td>
</tr>
<tr>
<td>$V_{SB}$</td>
<td>VSB</td>
<td>V</td>
<td>Source-Bulk voltage</td>
</tr>
<tr>
<td>$V_{TO}$</td>
<td>VTO</td>
<td>V</td>
<td>Zero-bias threshold voltage: $V_{TO} = V_{FB} + P_D \cdot (\phi_B + 2 \cdot \phi_T) + k_0 \cdot \sqrt[2]{\phi_B + 2 \cdot \phi_T}$</td>
</tr>
<tr>
<td>$V_{TS}$</td>
<td>VTS</td>
<td>V</td>
<td>Threshold voltage including back-bias effects: $V_{TS} = V_{FB} + P_D \cdot (V_{SB} + 2 \cdot \phi_T) - (V_{SB} - \phi_B) + k_0 \cdot \sqrt[2]{V_{SB} + 2 \cdot \phi_T}$</td>
</tr>
<tr>
<td>Symbol</td>
<td>Program Name</td>
<td>Units</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>--------------</td>
<td>-------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>VTH</td>
<td>V</td>
<td>Threshold voltage including back-bias and drain-bias effects: $V_{TH} = V_{FB} + P_D \cdot (V_{SB} + 2 \cdot \phi_T) - (V_{SB} - \phi_B) + k_0 \cdot \sqrt{V_{SB} + 2 \cdot \phi_T - \Delta V_G}$</td>
</tr>
<tr>
<td>$V_{GT}$</td>
<td>VGT</td>
<td>V</td>
<td>Effective gate drive including back-bias and drain voltage effects: $V_{GT} = V_{inv_{o}}$</td>
</tr>
<tr>
<td>$V_{DSAT}$</td>
<td>VDSS</td>
<td>V</td>
<td>Drain saturation voltage at actual bias</td>
</tr>
<tr>
<td>$V_{DS_{eff}}$</td>
<td>VSAT</td>
<td>V</td>
<td>Saturation limit: $V_{DS_{eff}} = V_{DS} - V_{DSAT}$</td>
</tr>
<tr>
<td>$g_m$</td>
<td>GM</td>
<td>A/V</td>
<td>Transconductance (assumed $V_{DS&gt;0}$): $g_m = \partial I_{DS}/\partial V_{GS}$</td>
</tr>
<tr>
<td>$g_{mb}$</td>
<td>GMB</td>
<td>A/V</td>
<td>Substrate-transconductance (assumed $V_{DS&gt;0}$): $g_{mb} = \partial I_{DS}/\partial V_{BS}$</td>
</tr>
<tr>
<td>$g_{ds}$</td>
<td>GDS</td>
<td>A/V</td>
<td>Output conductance: $g_{ds} = \partial I_{DS}/\partial V_{DS}$</td>
</tr>
<tr>
<td>$C_{D(D)}$</td>
<td>CDD</td>
<td>F</td>
<td>$C_{D(D)} = \partial Q_D/\partial V_{DS}$</td>
</tr>
<tr>
<td>$C_{D(G)}$</td>
<td>CDG</td>
<td>F</td>
<td>$C_{D(G)} = -\partial Q_D/\partial V_{GS}$</td>
</tr>
<tr>
<td>$C_{D(S)}$</td>
<td>CDS</td>
<td>F</td>
<td>$C_{D(S)} = C_{D(D)} - C_{D(G)} - C_{D(B)}$</td>
</tr>
<tr>
<td>$C_{D(B)}$</td>
<td>CDB</td>
<td>F</td>
<td>$C_{D(B)} = \partial Q_D/\partial V_{SB}$</td>
</tr>
<tr>
<td>$C_{G(D)}$</td>
<td>CGD</td>
<td>F</td>
<td>$C_{G(D)} = -\partial Q_G/\partial V_{DS}$</td>
</tr>
<tr>
<td>$C_{G(G)}$</td>
<td>CGG</td>
<td>F</td>
<td>$C_{G(G)} = \partial Q_G/\partial V_{GS}$</td>
</tr>
<tr>
<td>$C_{D(S)}$</td>
<td>CGS</td>
<td>F</td>
<td>$C_{G(S)} = C_{G(G)} - C_{G(D)} - C_{G(B)}$</td>
</tr>
<tr>
<td>$C_{G(B)}$</td>
<td>CGB</td>
<td>F</td>
<td>$C_{G(B)} = \partial Q_G/\partial V_{SB}$</td>
</tr>
<tr>
<td>$C_{S(D)}$</td>
<td>CSD</td>
<td>F</td>
<td>$C_{S(D)} = -\partial Q_S/\partial V_{DS}$</td>
</tr>
<tr>
<td>$C_{S(G)}$</td>
<td>CSG</td>
<td>F</td>
<td>$C_{S(G)} = -\partial Q_S/\partial V_{GS}$</td>
</tr>
</tbody>
</table>
### Symbol | Program Name | Units | Description
--- | --- | --- | ---
$C_{S(S)}$ | CSS | F | $C_{S(S)} = C_{S(G)} + C_{S(D)} + C_{S(B)}$
$C_{S(B)}$ | CSB | F | $C_{S(B)} = \frac{\partial Q_S}{\partial V_{SB}}$
$C_{B(D)}$ | CBD | F | $C_{B(D)} = -\frac{\partial Q_B}{\partial V_{DS}}$
$C_{B(G)}$ | CBG | F | $C_{B(G)} = -\frac{\partial Q_B}{\partial V_{GS}}$
$C_{B(S)}$ | CBS | F | $C_{B(S)} = C_{B(B)} - C_{B(D)} - C_{B(G)}$
$C_{B(B)}$ | CBB | F | $C_{B(B)} = -\frac{\partial Q_B}{\partial V_{SB}}$
$C_{GD_{ov}}$ | CGDOL | F | Gate-drain overlap capacitance of the actual transistor: $C_{GD_{ov}} = \frac{\partial Q_{OV_L}}{\partial V_{DS}}$
$C_{GS_{ov}}$ | CGSOL | F | Gate-source overlap capacitance of the actual transistor: $C_{GS_{ov}} = \frac{\partial Q_{OV_o}}{\partial V_{GS}}$
$W_E$ | WE | m | Effective channel width for geometrical models
$L_E$ | LE | m | Effective channel length for geometrical models
$u$ | U | - | Transistor gain: $u = g_m / g_{ds}$
$R_{out}$ | ROUT | $\Omega$ | Small-signal output resistance: $R_{out} = 1 / g_{ds}$
$V_{Early}$ | VEARLY | V | Equivalent Early voltage: $V_{Early} = |V_{DS}| / g_{ds}$
$k_{eff}$ | KEFF | $\sqrt{V}$ | Body effect parameter: $k_{eff} = k_0$
$\beta_{eff}$ | BEFF | $A / V^2$ | Gain factor: $2 \cdot \frac{|V_{DS}|}{V_{inv_o}}^2$
$f_T$ | FUG | Hz | Unity gain frequency at actual bias: $f_T = \frac{g_m}{2\pi(C_{G(G)} + C_{GS_{ov}} + C_{GD_{ov}})}$
$\sqrt{\frac{S_{V_{Gib}}}{q}}$ | SQRTSFW | $V_{\sqrt{Hz}}$ | Input-referred RMS white noise voltage density: $\sqrt{\frac{S_{V_{Gib}}}{q}} = \sqrt{S_{th}} / g_m$
When the parameter PRINTSCALED is set to 1, the device parameter set after geometrical and temperature scaling is added to the OP output:

### Symbol | Program Name | Units | Description
--- | --- | --- | ---
$\sqrt[n]{S_{V_{Gf}}}$ | SQRTSFF | $V/\sqrt{Hz}$ | Input-referred RMS white noise voltage density at 1 kHz: $\sqrt[n]{S_{V_{Gf}}}/S_{fl(1kHz)}/g_m$
$f_{knee}$ | FKNEE | Hz | Cross-over frequency above which white noise is dominant: $f_{knee} = \frac{1Hz \cdot S_{fl(1Hz)}}{S_{th}}$

### Quantity | Description
--- | ---
$VFB$ | Flat-band voltage for the actual transistor
$KO$ | Body-effect factor
$KPINV$ | Inverse of body-effect factor of the poly-silicon gate
$PHIB$ | Surface potential at the onset of strong inversion
$BET$ | Gain factor
$THESR$ | Mobility degradation parameter due to surface roughness scattering
$THEPH$ | Mobility degradation parameter due to phonon scattering
$ETAMOB$ | Effective field parameter for dependence on depletion charge
$NU$ | Exponent of field dependence of mobility model
$THER$ | Coefficient of series resistance
$THER1$ | Numerator of gate voltage dependent part of series resistance
$THER2$ | Denominator of gate voltage dependent part of series resistance
$THESAT$ | Velocity saturation parameter due to optical/acoustic phonon scattering
$THETH$ | Coefficient of self-heating
$SDIBL$ | Drain-induced barrier lowering parameter
$MO$ | Parameter for (short-channel) subthreshold slope
$SSF$ | Static-feedback parameter
$ALP$ | Factor of channel length modulation
$VP$ | Characteristic voltage of channel-length modulation
$MEXP$ | Smoothing factor
$PHIT$ | Thermal voltage at the actual temperature
<table>
<thead>
<tr>
<th>Quantity</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_1$</td>
<td>Factor of the weak-avalanche current</td>
</tr>
<tr>
<td>$A_2$</td>
<td>Exponent of the weak-avalanche current</td>
</tr>
<tr>
<td>$A_3$</td>
<td>Factor of the drain-source voltage above which weak-avalanche occurs</td>
</tr>
<tr>
<td>$IGINV$</td>
<td>Gain factor for intrinsic gate tunnelling current in inversion</td>
</tr>
<tr>
<td>$BINV$</td>
<td>Probability factor for intrinsic gate tunnelling current in inversion</td>
</tr>
<tr>
<td>$IGACC$</td>
<td>Gain factor for intrinsic gate tunnelling current in accumulation</td>
</tr>
<tr>
<td>$BACC$</td>
<td>Probability factor for intrinsic gate tunnelling current in accumulation</td>
</tr>
<tr>
<td>$VFBOV$</td>
<td>Flat-band voltage for the Source/Drain overlap extensions</td>
</tr>
<tr>
<td>$KOV$</td>
<td>Body-effect factor for the Source/Drain overlap extensions</td>
</tr>
<tr>
<td>$IGOV$</td>
<td>Gain factor for Source/Drain overlap tunnelling current</td>
</tr>
<tr>
<td>$COX$</td>
<td>Oxide capacitance for the intrinsic channel</td>
</tr>
<tr>
<td>$CGDO$</td>
<td>Oxide capacitance for the gate-drain overlap</td>
</tr>
<tr>
<td>$CGSO$</td>
<td>Oxide capacitance for the gate-source overlap</td>
</tr>
<tr>
<td>$GATENOISE$</td>
<td>Flag for in/exclusion of induced gate thermal noise</td>
</tr>
<tr>
<td>$NT$</td>
<td>Thermal noise coefficient</td>
</tr>
<tr>
<td>$NFA$</td>
<td>First coefficient of the flicker noise</td>
</tr>
<tr>
<td>$NFB$</td>
<td>Second coefficient of the flicker noise</td>
</tr>
<tr>
<td>$NFC$</td>
<td>Third coefficient of the flicker noise</td>
</tr>
<tr>
<td>$TOX$</td>
<td>Thickness of gate oxide layer</td>
</tr>
</tbody>
</table>
Remarks:

- When $V_{ds} < 0$, $g_m$ and $g_{mb}$ are calculated with drain and source terminals interchanged. The terminal voltages and $I_{DS}$ keep their sign.

- The signs of $V_{TO}$ and $V_{TS}$ follow the conventions of the model parameter set. The parameter set is always assumed to correspond to an n-channel device.

- $W$ and $L$ are not available for the electrical MOS models.

- $MULT$ is a scaling parameter that multiplies all currents and charges by the value of $MULT$. This is equivalent to putting $MULT$ (a number) MOS transistors in parallel. And as a consequence $MULT$ effects the operating point output.

A non-existent conductance, $G_{min}$, is connected between the nodes $D$ and $S$. This conductance $G_{min}$ does not influence the DC-operating point.

- Zero-bias threshold voltage:
  
  $$V_{TO} = V_{FB} + P_D \cdot (\phi_B + 2 \cdot \phi_T) + k_0 \cdot \sqrt{\phi_B + 2 \cdot \phi_T}$$

- Threshold voltage including back-bias effects:
  
  $$V_{TS} = V_{FB} + P_D \cdot (V_{SB_t} + 2 \cdot \phi_T) - (V_{SB_t} - \phi_B) + k_0 \cdot \sqrt{V_{SB_t} + 2 \cdot \phi_T}$$

- Threshold voltage including back-bias and drain-bias effects:
  
  $$V_{TH} = V_{FB} + P_D \cdot (V_{SB_t} + 2 \cdot \phi_T) - (V_{SB_t} - \phi_B) + k_0 \cdot \sqrt{V_{SB_t} + 2 \cdot \phi_T} - \Delta V_G$$
1.7 Embedding

1.7.1 Model embedding in a circuit simulator

In CMOS technologies both n- and p-channel MOS transistors are supported. It is convenient to use one model for both type of transistors instead of two separate models. This is accomplished by mapping a p-channel device with its bias conditions and parameter set onto an equivalent n-channel device with appropriately changed bias conditions (i.e. currents, voltages and charges) and parameters. In this way both type of transistors can be treated as an n-channel transistor. Nevertheless, the electrical behaviour of electrons and holes is not exactly the same (e.g. the mobility and tunnelling behaviour), and consequently slightly different equations have to be used in case of n- or p-type transistors, see section 1.2.2 on page 19.

As said earlier, any circuit simulator internally identifies the terminals of a MOS transistor by a number. However, designers are used to the standard terminology of source, drain, gate and bulk. Therefore, in the context of a circuit simulator it is traditionally possible to address, say, the drain of MOST number 17, even if in reality the corresponding source is at a higher potential (n channel case). More strongly, most circuit simulators provide for model evaluation a so called $V_{DS}$, $V_{GS}$, and $V_{SB}$ based on an a priori assignment of source, drain and bulk that is independent of the actual bias conditions. Since MOS Model 11 assumes saturation occurs at the drain side of the MOSFET, the basic model cannot cope with bias conditions that correspond to $V_{DS} < 0$. Again a transformation of the bias conditions is necessary.

In this case, the transformation corresponds to internally reassigning source and drain, applying the standard electrical model, and then reassigning the currents and charges to the original terminals. In MOS Model 11 care has been taken to preserve symmetry with respect to drain and source at $V_{DS} = 0$. In other words no non-singularities will occur in the higher-order derivatives at $V_{DS} = 0$.

In detail, in order to embed MOS Model 11 correctly into a circuit simulator, the following procedure, illustrated in figure 6 should be followed. We have assumed that indeed the simulator provides the nodal potentials $V^e_D$, $V^e_G$, $V^e_S$ and $V^e_B$ based on an a priori assignment of drain, gate, source and bulk.
Step 1 Calculate the voltages $V_{DS}''$, $V_{GS}''$, and $V_{SB}''$, and the additional voltages $V_{DG}''$ and $V_{SG}''$. The latter are used for calculating the charges associated with overlap capacitances.

Step 2 Based on n- or p-channel devices, calculate the modified voltages $V_{DS}'$, $V_{GS}'$, and $V_{SB}'$. From here onwards only n-channel behaviour needs to be considered.

Step 3 Based on a positive or negative $V'_{DS}$, calculate the internal nodal voltages. At this level, the voltages - and the parameters, see below - comply to all the requirements for input quantities of MOS Model 11.

Step 4 Evaluate all the internal output quantities - channel current, weak avalanche current, gate current, nodal charges, and noise-power spectral densities - using the standard MOS Model 11 equations and the internal voltages.

Step 5 Correct the internal output quantities for a possible source-drain interchange. In fact, this directly establishes the external noise power spectral densities.

Step 6 Correct for a possible p-channel transformation.

Step 7 Change from branch current to nodal currents, establishing the external current output quantities. Calculate the overlap charges that are related to the physical regions and add them to the nodal charges, thus forming the external charge output quantities.
\[ V^e_D, V^e_G, V^e_S, V^e_B \]

\[ V^e_{DS} = V^e_D - V^e_S \]
\[ V^e_{GS} = V^e_G - V^e_S \]
\[ V^e_{SB} = V^e_S - V^e_B \]
\[ V^e_{DG} = V^e_D - V^e_G \]
\[ V^e_{SG} = V^e_S - V^e_G \]

**n-channel**
\[ V^e_{DS} = V^e_{DS} \]
\[ V^e_{GS} = V^e_{GS} \]
\[ V^e_{SB} = V^e_{SB} \]

**p-channel**
\[ V^e_{DS} = -V^e_{DS} \]
\[ V^e_{GS} = -V^e_{GS} \]
\[ V^e_{SB} = -V^e_{SB} \]

**Channel type**

\[ V^e_{DS} \geq 0 \]

**yes**
\[ V^e_{DS} = V^e_{DS} \]
\[ V^e_{GS} = V^e_{GS} \]
\[ V^e_{SB} = V^e_{SB} \]

**no**
\[ V^e_{DS} = -V^e_{DS} \]
\[ V^e_{GS} = V^e_{GS} - V^e_D \]
\[ V^e_{SB} = V^e_{SB} + V^e_D \]

\[ I_{DS} = I_{DS}(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ I_{AVL} = I_{AVL}(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ I_{GS} = I_{GS}(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ I_{GD} = I_{GD}(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ I_{GB} = I_{GB}(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ Q_D = Q_D(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ Q_S = Q_S(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ Q_B = Q_B(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ s^r_s = S^r_s(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ s^f_s = S^f_s(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ s^r_l = S^r_l(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ s^l = S^l(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ s^l_s = S^l_s(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ s^l_l = S^l_l(V^e_{DS}, V^e_{GS}, V^e_{SB}) \]
\[ V_{DS} \geq 0 \]

\[ I_{DS} = I_{DS} \quad I_{GS} = I_{GS} \quad Q_D = Q_D \]
\[ I_{DB} = I_{AVL} \quad I_{GD} = I_{GD} \quad Q_G = Q_G \]
\[ I_{SB} = 0 \quad I_{GB} = I_{GB} \quad Q_S = Q_S \]
\[ Q_B = Q_B \]
\[ Q_{ov0} = Q_{ov0} \]
\[ Q_{ovl} = Q_{ovl} \]

\[ S_D = S_{th} + S_f \]
\[ S_G = S_{ig} \]
\[ S_S = S_{th} + S_f + S_{ig} \]
\[ S_{DG} = S_{igth} \]
\[ S_{GS} = -S_{ig} - S_{igth} \]
\[ S_{SD} = -S_{igth} - S_{th} - S_f \]

\[ I_{DS} = -I_{DS} \quad I_{GS} = I_{GD} \quad Q_D = Q_S \]
\[ I_{DB} = 0 \quad I_{GD} = I_{GS} \quad Q_G = Q_G \]
\[ I_{SB} = I_{AVL} \quad I_{GB} = I_{GB} \quad Q_S = Q_D \]
\[ Q_B = Q_B \]
\[ Q_{ov0} = Q_{ovl} \]
\[ Q_{ovl} = Q_{ovl} \]

\[ S_D = S_{th} + S_f + S_{ig} \]
\[ +2R_e\{S_{igth}\} \]
\[ S_G = S_{ig} \]
\[ S_S = S_{th} + S_f \]
\[ S_{DG} = -S_{ig} - S_{igth} \]
\[ S_{GS} = S_{igth} \]
\[ S_{SD} = -S_{igth} - S_{th} - S_f \]
It is customary to have separate user models in the circuit simulators for n- and p-channel transistors. In that manner it is easy to use a different set of reference and scaling parameters for the two channel types. As a consequence, the changes in the parameter values necessary for a p-channel type transistor are normally already included in the parameter sets on file. The changes should not be included in the simulator.
1.8 Simulator specific items

1.8.1 Pstar syntax

n channel electrical model: mne_n(d,g,s,b) level=1100, <parameters>
p channel electrical model: mpe_n(d,g,s,b) level=1100, <parameters>
n channel geometrical model: mn_n(d,g,s,b) level=1100, <parameters>
p channel geometrical model: mp_n(d,g,s,b) level=1100, <parameters>

n : occurrence indicator
<parameters> : list of model parameters
d, g, s and b are drain, gate, source and bulk terminals respectively.

1.8.2 Spectre syntax

n channel electrical model: model modelname mos1100e type=n <modpar>
componentname d g s b modelname <inpar>
p channel electrical model: model modelname mos1100e type=p <modpar>
componentname d g s b modelname <inpar>
n channel geometrical model: model modelname mos1100 type=n <modpar>
componentname d g s b modelname <inpar>
p channel geometrical model: model modelname mos1100 type=p <modpar>
componentname d g s b modelname <inpar>

modelname : name of model, user-defined
componentname : occurrence indicator
<modpar> : list of model parameters
<inpar> : list of instance parameters
d, g, s and b are drain, gate, source and bulk terminals respectively.

3 Note

Warning! In Spectre, use only the parameter statements type=n or type=p. Using any other string and/or numbers will result in unpredictable and possibly erroneous results.
1.8.3 ADS syntax

n channel electrical model : model modelname mos1100e gender=1 <modpar>
modelname:componentname d g s b <instpar>

p channel electrical model : model modelname mos1100e gender=0 <modpar>
modelname:componentname d g s b <instpar>

n channel geometrical model : model modelname mos1100 gender=1 <modpar>
modelname:componentname d g s b <instpar>

p channel geometrical model : model modelname mos1100 gender=0 <modpar>
modelname:componentname d g s b <instpar>

modelname : name of model, user-defined
componentname : occurrence indicator
<modpar> : list of model parameters
<instpar> : list of instance parameters
d, g, s and b are drain, gate, source and bulk terminals respectively.

1.8.4 The ON/OFF condition for Pstar

The solution for a circuit involves a process of successive calculations. The calculations are
started from a set of ‘initial guesses’ for the electrical quantities of the nonlinear elements. A
simplified DCAPPROX mechanism for devices using ON/OFF keywords is mentioned in [9].
By default the devices start in the default state.

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<th>p-channel</th>
</tr>
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<tbody>
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<td></td>
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</tr>
<tr>
<td>$V_{GS}$</td>
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<tr>
<td>$V_{SB}$</td>
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1.8.5 The ON/OFF condition for Spectre

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### 1.8.6 The ON/OFF condition for ADS

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<td>$V_{SB}$</td>
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<tr>
<td>$V_{GS}$</td>
<td>0</td>
</tr>
<tr>
<td>$V_{SB}$</td>
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</thead>
<tbody>
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<tr>
<td>$V_{GS}$</td>
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</tr>
<tr>
<td>$V_{SB}$</td>
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</tr>
</tbody>
</table>
1.9 Parameter extraction

The parameter extraction for MOS Model 11 using an optimization method is described step by step in the scheme below. The equations used for the parameter extraction are the basic equations of 1.2.2. It should be noticed that for the p-channel MOSFET all voltage and current values have to change sign upon entering the optimization program as a p-MOST is treated as an equivalent n-MOST. The bias conditions to be used for the measurements are dependent on the supply voltage of the process. Of course it is advisable to restrict the range of voltages to this supply voltage $V_{sup}$. Otherwise physical effects, atypical for normal transistor operation and therefore less well described by MOS Model 11, may dominate the characteristics.

The simultaneous determination of all parameters is not advisable, because the value of some parameters can be wrong due to correlation and suboptimisation. Therefore it is more practical to split the parameters into several groups, and, for each group, to measure the dc-characteristics according to the indicated conditions and to determine the specific parameters. Although the poly-depletion effect affects the dc-behaviour of a MOSFET, the poly-depletion parameter $KPINV$ can only be determined accurately from $C-V$-measurements. If the (physical) oxide thickness $t_{ox}$ and the polysilicon impurity concentration $N_p$ are known, the parameter $KPINV \, (= 1/k_p)$ can be calculated from:

$$k_p = \frac{t_{ox} \cdot \sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_p}}{\varepsilon_{ox}}$$  \hspace{1cm} (1.288)

If the polysilicon impurity concentration $N_p$ is not known, as a good first-order estimate one can use $N_p = 1 \cdot 10^{26} \text{ m}^{-3}$ for $n^+$-polysilicon gates and $N_p = 5 \cdot 10^{25} \text{ m}^{-3}$ for $p^+$-polysilicon gates. In the latter case, a measured $C_{GG} - V_{GS}$-characteristic for a long-channel transistor is essential for an accurate determination of $KPINV$.

Before the optimization is started a parameter set has to be determined which contains a first estimation of the parameters to be extracted and the parameters which remain constant. The value of $\phi_T$ is calculated from the device temperature $T_{KD}$ according to eq. (1.161). The value of smoothing factor $m$ is calculated from the device length $L$ and from the minimum feature size of the technology $L_{min}$ using eq. (1.136). The above equation is rounded off to an integer value.
The parameter set used as a first-order estimation of the parameters to be extracted is given in Table 2. With this parameter set a first optimization following the scheme below, is performed. After this the new parameter set serves as an estimation for the second optimization, which is performed following the same scheme. This method yields a proper set of parameters after the second optimization. Experiments with transistors of different processes show that the parameter set does not change very much after a third optimization.

**Measurements:**

The parameter extraction routine consists of five different dc-measurements and one (optional) capacitance measurement:

- **Measurement I:** $I_D/g_m/I_G-V_{GS}$ - characteristics in linear region:

  - n-channel: $V_{GS} = 0 \ldots V_{sup}$ (with steps of maximum 50 mV).  
    $V_{DS} = 50$ mV  
    $V_{BS} = 0 \ldots -V_{sup}$
  
  - p-channel: $V_{GS} = 0 \ldots -V_{sup}$ (with steps of maximum 50 mV).  
    $V_{DS} = -50$ mV  
    $V_{BS} = 0 \ldots V_{sup}$

- **Measurement II:** Subthreshold $I_D-V_{GS}$ - characteristics:

  - n-channel: $V_{GS} = V_T - 0.6$ V $\ldots V_T + 0.3$ V  
    $V_{DS} = 3$ values starting from 100 mV to $V_{sup}$  
    $V_{BS} = 0 \ldots -V_{sup}$
  
  - p-channel: $V_{GS} = V_T + 0.6$ V $\ldots V_T - 0.3$ V  
    $V_{DS} = 3$ values starting from -100 mV to $-V_{sup}$  
    $V_{BS} = 0 \ldots V_{sup}$
• **Measurement III:** $I_D/g_{DS}/g_{DS}-V_{DS}$ characteristics:

  - n-channel: $V_{DS} = 0 \ldots V_{sup}$ (with steps of maximum 50 mV).
    
    $V_{GS} = 4$ values starting from $V_T + 0.1$ V, not above $V_{sup}$
    
    $V_{BS} = 3$ values starting from 0 V to $-V_{sup}$

  - p-channel: $V_{DS} = 0 \ldots -V_{sup}$ (with steps of maximum 50 mV).
    
    $V_{GS} = 4$ values starting from $V_T + 0.1$ V, not below $-V_{sup}$
    
    $V_{BS} = 3$ values starting from 0 V to $V_{sup}$

• **Measurement IV:** $I_D/I_S/I_G/I_B-V_{GS}$ characteristics in all operation regions:

  - n-channel: $V_{GS} = -V_{sup} \ldots V_{sup}$ (with steps of maximum 50 mV).
    
    $V_{DS} = 4$ values starting from 0 V to $V_{sup}$
    
    $V_{BS} = 0$ V

  - p-channel: $V_{GS} = -V_{sup} \ldots -V_{sup}$ (with steps of maximum 50 mV).
    
    $V_{DS} = 4$ values starting from 0 V to $-V_{sup}$
    
    $V_{BS} = 0$ V

• **Measurement V:** $I_B-V_{GS}$ characteristics:

  - n-channel: $V_{GS} = 0 \ldots V_{sup}$ (with steps of maximum 50 mV).
    
    $V_{DS} = 3$ values not above $V_{sup}$
    
    $V_{BS} = 0$ V

  - p-channel: $V_{GS} = 0 \ldots -V_{sup}$ (with steps of maximum 50 mV).
    
    $V_{DS} = 3$ values not below $-V_{sup}$
    
    $V_{BS} = 0$ V

• **Measurement VI:** $C_{gg}-V_{GS}$ characteristics (optional):

  - n/p-channel: $V_{GS} = -V_{sup} \ldots V_{sup}$ (with steps of maximum 50 mV).
    
    $V_{DS} = 0$ V
    
    $V_{BS} = 0$ V
<table>
<thead>
<tr>
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<tr>
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Table 2: Starting miniset parameter values for parameter extraction of a typical MOS transistor with channel length \( L \) (m), channel width \( W \) (m), oxide thickness \( t_{ox} \) (m) and polysilicon impurity concentration \( N_p \) \( \text{m}^{-3} \) at room temperature. If the polysilicon concentration \( N_p \) is not known, one can use \( N_p = 1 \cdot 10^{26} \text{m}^{-3} \) or \( 5 \cdot 10^{25} \text{m}^{-3} \) for \( n^+ \)-resp. \( p^+ \)-polysilicon gates. Parameters \( C_{ox} \), \( C_{GSO} \) and \( C_{GDO} \) are only important for the charge model, and do not affect the dc-model; they have to be extracted from \( C-V \)-characteristics. In order to determine the geometry-scaling of parameters, the last column indicates for which conditions the parameters have to be extracted: \( L \)=long-channel device (fixed for short-channel devices), \( S \)=short-channel devices, \( A \)=all devices and \( F \)=fixed parameter.

<table>
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<tr>
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<th>( n )</th>
<th>( p )</th>
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<tr>
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<td>( V_{\text{FBov}} )</td>
<td>VFBOV</td>
<td>0.1</td>
<td>0.1</td>
<td>L</td>
</tr>
<tr>
<td>( k_{ov} )</td>
<td>KOV</td>
<td>( 9.3 \cdot 10^8 \cdot t_{ox} )</td>
<td>( 3.8 \cdot 10^8 \cdot t_{ox} )</td>
<td>L</td>
</tr>
<tr>
<td>( I_{\text{GOV}} )</td>
<td>IGOV</td>
<td>( 5.0 \cdot 10^{-13} \cdot W/t_{ox}^2 )</td>
<td>( 5.0 \cdot 10^{-12} \cdot W/t_{ox}^2 )</td>
<td>A</td>
</tr>
<tr>
<td>( C_{ox} )</td>
<td>COX</td>
<td>( \varepsilon_{ox}/t_{ox} \cdot W \cdot L )</td>
<td>( \varepsilon_{ox}/t_{ox} \cdot W \cdot L )</td>
<td>-</td>
</tr>
<tr>
<td>( C_{GDO} )</td>
<td>CGDO</td>
<td>( 3.0 \cdot 10^{-10} \cdot W )</td>
<td>( 3.0 \cdot 10^{-10} \cdot W )</td>
<td>-</td>
</tr>
<tr>
<td>( C_{GSO} )</td>
<td>CGSO</td>
<td>( 3.0 \cdot 10^{-10} \cdot W )</td>
<td>( 3.0 \cdot 10^{-10} \cdot W )</td>
<td>-</td>
</tr>
</tbody>
</table>
The values of transconductance $g_m$ and output conductance $g_{DS}$ are extracted from the $I-V$-characteristics by calculating in a numerical way the derivative of $I_D$ to $V_{GS}$ and $V_{DS}$, respectively. In the subthreshold measurements, use is made of threshold voltage $V_T$, which has to be determined for all the used bulk-source bias values $V_{BS}$. The determination of $V_T$ is rather arbitrary, and it can be either determined using the linear extrapolation method or the constant current criterion.

For an accurate extraction of parameter values, the parameter set for a long-channel transistor has to be determined first. In the long-channel case the poly-depletion parameter $1/k_p$, the flat-band voltage $V_{FB}$, the carrier mobility (i.e. $\theta_{sr}$, $\theta_{ph}$ and $\eta_{mob}$) and the gate tunnelling probability factors ($B_{inv}$ and $B_{acc}$) can be determined, and they can subsequently be fixed for the short and narrow-channel devices, see Table 2.

In Table 3 the extraction procedure for long-channel transistors is given. Since the value of body-factor $k_0$ may change much over geometry and over technology, the first-order estimate in Table 2 is very crude and a more accurate, preliminary value is obtained using Step 1. In Step 2 (optional) more accurate values of the poly-depletion parameter $1/k_p$ and the flat-band voltage $V_{FB}$ (which determines the onset of accumulation), are extracted. Next the subthreshold parameters $\phi_B$, $k_0$ and $m_0$ are optimized in Step 3, neglecting short-channel effects such as drain-induced barrier-lowering (DIBL). After that the mobility parameters are optimized using Steps 4 and 5, neglecting the influence of series-resistance. In Step 6 a preliminary value of the velocity saturation parameter is obtained, and subsequently the conductance parameters $\sigma_{sf}$, $\alpha$ and $\theta_{th}$ are determined in Step 7. A more accurate value of $\theta_{sat}$ can now be obtained using Step 8. The gate current parameters are determined in Steps 9 and 10. Finally, the weak-avalanche parameters are optimized in Step 11. For short-channel devices the values of the poly-depletion parameter $1/k_p$, flat-band voltage $V_{FB}$, the carrier mobility parameters ($\theta_{sr}$, $\theta_{ph}$ and $\eta_{mob}$) and the gate tunnelling probability factors ($B_{inv}$ and $B_{acc}$) of the long-channel device are copied, and next the extraction procedure as given in Table 4 is executed. In contrast to the long-channel case, the extraction procedure for short-channel devices also optimizes the parameters for series-resistance\(^1\) and DIBL.

---

1. Note that in Table parameters $\theta_{R1}$ and $\theta_{R2}$ are not included, which implies that the series-resistance is assumed to be voltage-independent. This holds true for modern CMOS technologies, where no use is made of LDD-structures.
Table 3: DC-parameter extraction procedure for an n-type long-channel MOS transistor, where Steps 2 and 12 are optional. For p-type transistors all voltages and currents have to be multiplied by -1. The optimization is either performed on the absolute or relative deviation between model and measurements. Parameter \( I_{tst} \) is 2.5 \( \mu A \) for NMOS and 0.8 \( \mu A \) for PMOS. The parameter is only determined for temperatures unequal to room temperature. For n-type MOS transistors \( B_{adv} = B_{inv} \), and as a result \( B_{adv} \) does not have to be extracted. For p-type MOS transistors this is not the case, see Table 1.
Table 4: DC-Parameter extraction procedure for an n-type short-channel MOS transistor. For p-type transistors all voltages and currents have to be multiplied by -1. Parameters $1/k_p$, $V_{FB}$, $\theta_{sr}$, $\theta_{ph}$, $\eta_{mob}$, $B_{inv}$, $B_{acc}$ and $k_{ov}$ are taken from the long-channel case. The optimization is either performed on the absolute or relative deviation between model and measurements.

**AC-parameters:** The AC-parameters $C_{ox}$, $C_{GSO}$, $C_{GDO}$, $k_{ov}$ and $V_{FBov}$ cannot be (accurately) determined from DC-characteristics, and as a consequence they have to be determined from $C-V$ characteristics. Since normal MOS transistors are symmetrical devices, one can assume that the oxide capacitance of the source and drain extension are identical, which implies that $C_{GSO} = C_{GDO}$. The oxide capacitance of the intrinsic MOSFET $C_{ox}$ can be extracted from Measurement VI. For an accurate determination of the bias-dependent overlap capacitances $C_{GSO}(= C_{GDO})$, $k_{ov}$ and $V_{FBov}$, the following $C-V$-measurements have to be done:

<table>
<thead>
<tr>
<th>Step</th>
<th>Optimized Parameters</th>
<th>Measurement</th>
<th>Fitted On</th>
<th>Absolute/Relative</th>
<th>Specific Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$\phi_R$, $k_0$, $\beta$, $\theta_R$</td>
<td>I</td>
<td>$I_D$</td>
<td>Absolute</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>$\phi_B$, $k_0$, $m_0$, $\sigma_{dibl}$</td>
<td>II</td>
<td>$I_D$</td>
<td>Relative</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>$\beta$, $\theta_R$</td>
<td>I</td>
<td>$I_D/g_m$</td>
<td>Relative</td>
<td>$V_{SB} = 0\text{V}$ $V_{GS} &gt; V_T + 0.3\text{V}$</td>
</tr>
<tr>
<td>4</td>
<td>$\theta_{sat}$</td>
<td>III</td>
<td>$I_D$</td>
<td>Absolute</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>$\sigma_{sf}$, $\alpha$, $\theta_{Th}$, $\sigma_{dibl}$</td>
<td>III</td>
<td>$g_{DS}$</td>
<td>Relative</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>$\theta_{sat}$</td>
<td>III</td>
<td>$I_D$</td>
<td>Absolute</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>$I_{GINV}$, $I_{GOV}$, $I_{GACC}$</td>
<td>IV</td>
<td>$I_G$</td>
<td>Absolute</td>
<td>-</td>
</tr>
<tr>
<td>8</td>
<td>$a_1$, $a_2$, $a_3$</td>
<td>V</td>
<td>$I_B$</td>
<td>Absolute</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>Repeat steps 2, 3, 4, 5, 7 and 8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
• **Measurement VII:** $C_{dg} - V_{GS}$ - characteristics:

- **n-channel:** $V_{GS} = -V_{sup} \ldots 0$ (with steps of maximum 50 mV).
  - $V_{DS} = 0 \text{ V}$
  - $V_{SB} = 0 \text{ V}$

- **p-channel:** $V_{GS} = 0 \ldots V_{sup}$ (with steps of maximum 50 mV).
  - $V_{DS} = 0 \text{ V}$
  - $V_{SB} = 0 \text{ V}$

• **Measurement VIII:** $C_{gd} - V_{DS}$ - characteristics (optional):

- **n-channel:** $V_{GB} = 0 \text{ V}$
  - $V_{DS} = 0 \text{ V}$
  - $V_{SB} = 0 \ldots V_{sup}$ (with steps of maximum 50 mV).

- **p-channel:** $V_{GB} = 0 \text{ V}$
  - $V_{DS} = 0 \text{ V}$
  - $V_{SB} = -V_{sup} \ldots 0$ (with steps of maximum 50 mV).

In Table 5 the extraction procedure for the AC-parameters is given.

<table>
<thead>
<tr>
<th>Step</th>
<th>Optimised Parameters</th>
<th>Measurement</th>
<th>Fitted On</th>
<th>Absolute/Relative Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$k_{ov}, C_{GSO}$</td>
<td>VII / VII</td>
<td>$C_{gd}/C_{dg}$</td>
<td>Relative -</td>
</tr>
<tr>
<td>2</td>
<td>$C_{ox}$</td>
<td>VI</td>
<td>$C_{gg}$</td>
<td>Relative -</td>
</tr>
<tr>
<td>3</td>
<td>Repeat steps 1 and 2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Table 5:* **AC-parameter extraction procedure for a MOS transistor.** Here it is assumed that $C_{GSO} = C_{GDO}$. In the first instance flat-band voltage $V_{FBov}$ is not optimised, although it may be optimised during Step 1 in order to obtain more accurate results. The optimization is either performed on the absolute or relative deviation between model and measurements.
Scaling of Parameters

Using the scaling relations of section 1.4 on page 62 it is possible to calculate a parameter set for a process, given the parameter set of typical transistors of this process. To accomplish this, transistors of different lengths, widths and at different temperatures have to be measured. With the results of these measurements the sensitivities of the parameters on length, width and temperature can be found. For the determination of a geometry-scaled parameter set a three-step procedure is recommended:

1. Determine minisets \((\phi_B, k_0, \beta, \ldots)\) for all measured devices, as explained in section 1.9 on page 105.

2. The width and length sensitivity coefficients are optimized by fitting the appropriate geometry scaling rules to these miniset parameters.

3. Finally, the width and length sensitivity coefficients are optimized by fitting the result of the scaling rules and current equations to the measured currents of all devices simultaneously.

An important part of the above-described parameter extraction is the determination of \(\Delta L\) and \(\Delta W\), see eqs. (1.112) and (1.113), since it affects both the DC- and the AC-model. Traditionally \(\Delta W\) can be determined from the extrapolated zero-crossing in the \(\beta\) versus mask width \(W\) characteristic. In a similar way \(\Delta L\) can be determined from the \(1/\beta\) versus mask length \(L\) characteristic. For modern MOS devices with pocket implants, however, it has been found that the above \(\Delta L\) extraction method is no longer valid [18]. Another, more accurate method is to measure the gate-to-bulk capacitance \(C_{GB}\) in accumulation for different channel lengths [19]. In this case the extrapolated zero-crossing in the \(C_{GB}\) versus mask length \(L\) curve will give \(\Delta L\).

For the determination of a temperature-scaled parameter set a three-step procedure is recommended:

1. Determine minisets at various temperature values (at least three) for the corner devices, i.e. the long/broad, the long/narrow, the short/broad and the short/narrow channel transistor.

2. The temperature sensitivity coefficients are optimized by fitting the appropriate temperature scaling rules to these miniset parameters.

3. Finally, the temperature sensitivity coefficients are optimized by fitting the result of the scaling rules and current equations to the measured currents of the corner devices simultaneously.
Parameter sets have been determined for several processes using this parameter extraction strategy and taking care of not exceeding the supply voltage. For all processes good results have been obtained.
1.10 References


A
Hyp functions
Figure 7: \( \text{hyp}_1(x; \varepsilon) = \frac{1}{2} \cdot (x + \sqrt{x^2 + 4 \cdot \varepsilon^2}) \)

Figure 8: \( \text{hyp}_2(x; x_0; \varepsilon) = x - \text{hyp}_1(x - x_0; \varepsilon) \)
Figure 9: \( hyp_3(x;x_0;\varepsilon) = hyp_2(x;x_0;\varepsilon) - hyp_2(0;x_0;\varepsilon) \) for \( \varepsilon = \varepsilon(x_0) \)

Figure 10: \( hyp_4(x;x_0;\varepsilon) = hyp_1(x - x_0;\varepsilon) - hyp_1(-x_0;\varepsilon) \)
Figure 11: \( \text{hyp}_5(x;x_0;\varepsilon) = x_0 - \text{hyp}_1\left(x_0 - x - \frac{\varepsilon^2}{x_0}\right) \) for \( \varepsilon = \varepsilon(x_0) \)

The hypm-function:

\[
\text{hypm}[x,y;m] = \frac{x \cdot y}{(x^{2 \cdot m} + y^{2 \cdot m})^{1/(2 \cdot m)}}
\]  

(1.289)
B

Spectre Specific Information
Imax, Imelt, Jmelt parameters

Introduction

Imax, Imelt and Jmelt are Spectre-specific parameters used to help convergence and to prevent numerical problems. We refer in this text only to the use of Imax model parameter in Spectre with SiMKit devices since the other two parameters, Imelt and Jmelt, are not part of the SiMKit code. For information on Imelt and Jmelt refer to Cadence documentation.

Imax model parameter

Imax is a model parameter present in the following SiMKit models:
– juncap and juncap2
– psp and pspnqs (since they contain juncap models)

In Mextram 504 (bjt504) and Modella (bjt500) SiMKit models, Imax is an internal parameter and its value is set through the adapter via the Spectre-specific parameter Imax.
The default value of the Imax model parameter is 1000A. Imax should be set to a value which is large enough so it does not affect the extraction procedure.

In models that contain junctions, the junction current can be expressed as:

$$I = I_s \exp\left(\frac{V}{N \cdot \phi_{TD}} - 1\right)$$

(1.290)

The exponential formula is used until the junction current reaches a maximum (explosion) current Imax.

$$I_{max} = I_s \exp\left(\frac{V_{exp}}{N \cdot \phi_{TD}} - 1\right)$$

(1.291)

The corresponding voltage for which this happens is called Vexp (explosion voltage). The voltage explosion expression can be derived from (1):

$$V_{exp} = N \cdot \phi_{TD} \log\left(\frac{I_{max}}{I_s}\right) + 1$$

(1.292)

For $V > V_{exp}$, the following linear expression is used for the junction current:
Region parameter

Region is an Spectre-specific model parameter used as a convergence aid and gives an estimated DC operating region. The possible values of region depend on the model:

– For Bipolar models:
  – subth: Cut-off or sub-threshold mode
  – fwd: Forward
  – rev: Reverse
  – sat: Saturation.
  – off

– For MOS models:
  – subth: Cut-off or sub-threshold mode;
  – triode: Triode or linear region;
  – sat: Saturation
  – off

For PSP and PSPNQS all regions are allowed, as the PSP(NQS) models both have a MOS part and a juncap (diode). Not all regions are valid for each part, but when e.g. region=forward is set, the initial guesses for the MOS will be set to zero. The same holds for setting a region that is not valid for the JUNCAP.

– For diode models:
  – fwd: Forward
  – rev: Reverse
  – brk: Breakdown
  – off

Model parameters for device reference temperature in Spectre

This text describes the use of the tnom, tref and tr model parameters in Spectre with SiMKit devices to set the device reference temperature.

\[ I = I_{\text{max}} + (V - V_{\text{exp1}}) \frac{I_s}{N \cdot \phi_{TD}} \exp\left( \frac{V_{\text{exp1}}}{N \cdot \phi_{TD}} \right) \] (1.293)
A Simkit device in Spectre has three model parameter aliases for the model reference temperature, \( t_{\text{nom}} \), \( t_{\text{ref}} \) and \( t_r \). These three parameters can only be used in a model definition, not as instance parameters.

There is no difference in setting \( t_{\text{nom}} \), \( t_{\text{ref}} \) or \( t_r \). All three parameters have exactly the same effect. The following three lines are therefore completely equivalent:

\[
\begin{align*}
\text{model nmos11020 mos11020 type=n tnom=30} \\
\text{model nmos11020 mos11020 type=n tref=30} \\
\text{model nmos11020 mos11020 type=n tr=30}
\end{align*}
\]

All three lines set the reference temperature for the mos11020 device to 30 C.

Specifying combinations of \( t_{\text{nom}} \), \( t_{\text{ref}} \) and \( t_r \) in the model definition has no use, only the value of the last parameter in the model definition will be used. E.g.:

\[
\text{model nmos11020 mos11020 type=n tnom=30 tref=34}
\]

will result in the reference temperature for the mos11020 device being set to 34 C, \( t_{\text{nom}}=30 \) will be overridden by \( t_{\text{ref}}=34 \) which comes after it.

When there is no reference temperature set in the model definition (so no \( t_{\text{nom}} \), \( t_{\text{ref}} \) or \( t_r \) is set), the reference temperature of the model will be set to the value of \( t_{\text{nom}} \) in the options statement in the Spectre input file. So setting:

\[
\begin{align*}
\text{options1 options tnom=23 gmin=1e-15 reltol=1e-12} \\
\text{vabstol=1e-12 iabstol=1e-16} \\
\text{model nmos11020 mos11020 type=n}
\end{align*}
\]

will set the reference temperature of the mos11020 device to 23 C.

When no \( t_{\text{nom}} \) is specified in the options statement and no reference temperature is set in the model definition, the default reference temperature is set to 27 C.

So the lines:

\[
\begin{align*}
\text{options1 options gmin=1e-15 reltol=1e-12 vabstol=1e-12} \\
\text{iabstol=1e-16} \\
\text{model nmos11020 mos11020 type=n}
\end{align*}
\]

will set the reference temperature of the mos11020 device to 27 C.
The default reference temperature set in the SiMKit device itself is in the Spectre simulator never used. It will always be overwritten by either the default "options tnom", an explicitly set option tnom or by a tnom, tref or tr parameter in the model definition.
Overvoltage warnings in SiMKit

Introduction
Overvoltage flagging is signalling that a (terminal) voltage is outside a specified safe range. A warning will be given when the conditions for giving a warning are fulfilled.

Simple checks for overvoltage have been added to the following models: mos903, mos1100, mos1101, mos1102, mos2002, mos2003, mos3100, mos4000, psp102, psp103. The checks are done on terminal voltages of the models.

There are many ways to define overvoltage. For a general overvoltage flagging solution Verilog-A should be used.

Extra parameters for overvoltage flagging
A set of extra parameters has been added to the mos models mos903, mos1100, mos1101, mos1102, mos2002, mos2003, mos3100, mos4000, psp102, psp103.

Table 6:

<table>
<thead>
<tr>
<th>Name</th>
<th>Unit</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBOX</td>
<td>V</td>
<td>0.0</td>
<td>Oxide breakdown voltage. Checking will be done if $VBOX &gt; 0$</td>
</tr>
<tr>
<td>VBDS</td>
<td>V</td>
<td>0.0</td>
<td>Drain-source breakdown voltage Checking will be done if $VBDS &gt; 0$</td>
</tr>
<tr>
<td>TMIN</td>
<td>s</td>
<td>0.0</td>
<td>Ovcheck tmin value</td>
</tr>
</tbody>
</table>

For mos models the safe region is:

$|V_{gs}| < VBOX$ and $|V_{gd}| < VBOX$ and $|V_{ds}| < VBDS$
Ovcheck: two terminal dummy model

A (dummy) two-terminal model ovcheck has been implemented that can be used to check if the voltage between the two terminals is within or without a so called safe region. The model parameters are:

<table>
<thead>
<tr>
<th>Name</th>
<th>Unit</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VLOW</td>
<td>V</td>
<td>0.0</td>
<td>Lower bound of safe region</td>
</tr>
<tr>
<td>VHIGH</td>
<td>V</td>
<td>0.0</td>
<td>Upper bound of safe region</td>
</tr>
<tr>
<td>TMIN</td>
<td>s</td>
<td>0.0</td>
<td>Ovcheck tmin value</td>
</tr>
</tbody>
</table>

Checking will be done when $VLOW \leq V_{t1} - V_{t2} \leq VHIGH$, where $t1$ is the first and $t2$ is the second terminal.

For the ovcheck model the safe region is:

Functionality

In Spectre and Pstar

At the end of a DC analysis or in a transient analysis after each time step a check will be done if the device is inside or outside the safe region. A warning is given whenever the device enters or leaves the safe region.
**In Spectre only**

To prevent too many warnings in a Spectre transient analysis the model parameter TMIN has been introduced. If the time between leaving and entering the safe region is less than the TMIN value no warning is given. Because of the TMIN parameter a warning cannot be issued when leaving the safe region. A warning is given when the device enters the safe region again. This warning includes the time and the voltage when the safe region was exited. At the end of the transient warnings are given for devices that are still out of the safe range.

In Pstar TMIN may be specified as a model parameter, but it will be ignored.
D

Parameter PARAMCHK
Parameter PARAMCHK

Introduction

All models have the parameter PARAMCHK. It is not related to the model behavior, but has been introduced control the clip warning messages. Various situations may call for various levels of warnings. This is made possible by setting this parameter.

PARAMCHK model parameter

This model parameter has been added to control the amount of clip warnings.

<table>
<thead>
<tr>
<th>PARAMCHK</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 0</td>
<td>No clip warnings</td>
<td></td>
</tr>
<tr>
<td>≥ 0</td>
<td>Clip warnings for instance parameters (default)</td>
<td></td>
</tr>
<tr>
<td>≥ 1</td>
<td>Clip warnings for model parameters</td>
<td></td>
</tr>
<tr>
<td>≥ 2</td>
<td>Clip warnings for electrical parameters at initialisation</td>
<td></td>
</tr>
<tr>
<td>≥ 3</td>
<td>Clip warnings for electrical parameters during evaluation. This highest level is of interest only for selfheating jobs, where electrical parameters may change dependent on temperature.</td>
<td></td>
</tr>
</tbody>
</table>
Bibliography


[22] Ir. C. Kortekaas, *Description and users guide of the MOS interconnect capacitance extractor; MICE 2.0*, Nat. Lab Technical note 1988


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[66] V. Palankovski R. Schultheis and S. Selberherr, *Modelling of power heterojunction bipolar transistor on gallium arsenide*, IEEE Trans. Elec. Dev., vol 48, pp. 1264-1269, 2001. Note: the paper uses \( \alpha = 1.65 \) for Si, but \( \alpha = 1.3 \) gives a better fit: also, \( k_{300} \) for GaAs is closer to 40 than to the published value of 46 (Palankovski, personal communication).

[67] JUNCAP: http://www.semiconductors.philips.com/Philips_Models/


[70] MOSModel 9:
http://www.nxp.com/models/